Micromachined Acoustic Programmable Tunable
Finite Impulse Response (FIR) Filters for
Microwave Applications

by

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ABSTRACT
This dissertation proposes a miniature FIR filter that works at microwave frequencies, whose filter response can ideally be digitally programmed. Such a frequency agile device can find applications in cellular communications and wireless networking. The basic concept of the FIR filter utilizes a low loss acoustic waveguide of appropriate geometry that acts as a traveling wave tapped-delay line. The input RF signal is applied by an array of capacitive transducers at various locations on the acoustic waveguide at one end that excites waves of a propagating acoustic mode with varying spatial delays and amplitudes which interfere as they propagate. The output RF signal is picked up at the other end of the waveguide by another array of capacitive transducers. Tuning of the FIR filter coefficients is realized by controlling the DC voltage profile applied to the individual transducers which essentially shapes the overall filter response. Equivalent circuit modeling of the capacitive transducer, acoustic waveguide and transducer-line coupling is presented in this dissertation. A theoretical model for the filter is developed from a general theory of an array of transducers exciting a waveguide and is used to obtain a set of filter design equations. A MATLAB based circuit simulator is developed to simulate the filter responses. Design parameters and simulation results obtained for an example waveguide structure are presented and compared to the values estimated by the theoretical model. A waveguide structure utilizing the Rayleigh-like mode of a ridge is then introduced. A semi-analytical method to obtain propagating elastic modes of such a ridge waveguide etched in an anisotropic crystal is presented. Microfabrication of a filter based on ridges etched in single crystal Silicon is discussed along with details of the challenges faced. Finally, future work and a few alternative designs are presented that can have a better chance of success. Analysis and modeling work to this point has given a good understanding of the working principles, performance tradeoffs and fabrication pitfalls of the proposed device. With the appropriate acoustic waveguide structure, the proposed device could make it possible to realize miniature programmable FIR filters in the GHz range.
To my loving parents Shekhar and Jyotsna
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Chapter 1

INTRODUCTION

This project aims to develop an RF MEMS filter that can be digitally tuned to various frequencies in the microwave range and whose frequency response can be shaped to some extent. Such a highly versatile frequency hopping device is useful in spread spectrum cellular communications and defense applications. In general, filters are an integral part of radio transceivers. They must be adaptable to different standards, modulation schemes, and frequency bands. High-speed ultra-selective tunable filters are essential for spectral sensing and channel traffic assessment in cognitive radio applications. The required degree of filter tunability in some applications can exceed several frequency decades. The device proposed here exploits the voltage-controlled transduction coefficient of capacitive transducers to achieve a programmable function. The FIR filtering scheme offers a large degree of control over the filter characteristics through direct synthesis of the impulse response. The ability to program a filter response digitally has the benefit of a faster tuning rate that can be useful for covert OFDM-type communications and most radar systems. An adjustable frequency response can be used for realizing equalizers, suppressing interferers by adaptively adding transmission zeros, or opting for multiple simultaneous channels in fast frequency-hopping systems.

In the past, various groups have tried to fabricate tunable or switchable RF MEMS filters. A brief overview of the recent developments in this area of research is presented here.

In a paper published in 2008 [1], Chandrahlim et al. of Cornell University report a digitally tunable filter using coupled arrays of dielectrically transduced square-extensional mode resonators that works at 500 MHz. The filter can only be tuned between 2 bands with the appropriate DC bias. The required DC bias voltages are very high and the size of each resonator is approximately 100 um by 100 um. A more recent paper by the same group
[2] reports a switchable filter bank based on 2 contour mode resonator filters and monolithically integrate PZT switches. The minimum insertion loss achieved is around -17 dB and the center frequency cannot be tuned over a wide range. Poorkamali et al. of Georgia Institute of Technology [3][4] have also made a coupled resonator based bandpass filter with tunable bandwidth. All the test structures reported in these papers have a center frequency of less than 1 MHz and the size of each resonator is greater than 100 um by 10 um. Also the range over which the center frequency can be tuned is not very large. A multiple frequency bandpass filter using rectangular plate or ring shaped piezoelectric resonators has been demonstrated by Piazza et al. [5]. The filter cannot be digitally tuned to different frequencies. The dimensions of the resonators are also more than 100 um by 100 um. Perez et al. of University of Pennsylvania [6] report an attempt to control the bandwidth of acoustically coupled AlN contour mode filters by exciting higher order modes in resonators using multiple electrodes with appropriate spacing. The insertion loss is in the range of -15 dB to -20 dB and increases as the bandwidth is widened because of decoupling between the modes of the resonators. A super high frequency AlN piezoelectric channel-select filter using resonators employing thickness field excitation inside AlN nano plates operating at 1.96 GHz has been built by the same group [7]. The insertion loss is greater than 10 dB and these filters cannot be tuned very easily. A older work by Ark-Chew et al. of The University of Michigan [8] have reports a filter cum mixer from interlinked micromechanical resonators to operate at 37 MHz. Large DC biases are required for substantial tuning capability. Various designs employing SAW waves have also been built, but they generally suffer from large insertion loss and the filter response cannot be shaped easily. To summarize, reconfigurable tunable passive electromagnetic filters that use varactors, transmission line segments, inductors, capacitors and resonators switched by MEMS switches, suffer from the following drawbacks –
• Moderate Q’s (<300) BW=1-20%
• Modest filter selectivity
• High insertion-loss
• Tuning range is typically less than an octave
• Filter structures are large
• Fabrication technology is not compatible with CMOS
• Reliability issues with MEMS switches

It is evident from this brief survey that the state of the art is still not mature enough and no one has so far claimed to have built a miniature digitally programmable Finite Impulse Response (FIR) microwave filter in the GHz range. It should be mentioned here that the device proposed in this dissertation is currently a theoretical concept and no working device has ever been built. It is up to the reader to conceive a practical filter design based on the theory outlined here, that would rival the performance of the devices cited in the above literature survey.

In this chapter, the basic concept of the filter is discussed in Section 1.1. A simplified model of the idealized filter is presented in Section 1.2. A simplified equation of the FIR filter transfer function is also derived in that section. An explanation of the basic electrical connections of the DC bias and input and output RF signals is presented in Section 1.3. Finally, Section 1.4 discusses the basic outline of the entire dissertation.
1.1 Basic Concept

The device proposed in this project utilizes a traveling wave tapped-delay line and capacitive transducers to realize an FIR filter whose response can ideally be programmed to change its center frequency, bandwidth, and response shape. Figure 1.1 shows an illustration of the basic principle behind the proposed concept. By using a low loss acoustic waveguide of appropriate geometry, a miniature device with acceptable impedance can be fabricated. This filter can be programmed with a switching time on the order of microseconds. The input RF signal is applied at various locations on the acoustic waveguide at one end that excites waves of a propagating acoustic mode with varying spatial delays and amplitudes which interfere as they propagate. The output RF signal is picked up at various locations along the propagating structure at the other end, resulting in a tapped delay line that is essential to the construction of an FIR filter.

Figure 1.1 Illustration of the basic principle behind the tapped-delay line based acoustic finite impulse response filter showing the main components, namely, the acoustic waveguide and the capacitive transducer arrays. The input array excites the acoustic mode in the waveguide, thereby converting the signal from the electrical domain into the mechanical domain, while the output array picks up the partially filtered signal and converts it back to the electrical domain.
The basic principle used for tuning in this design is that the frequency response of the input and output transducer arrays can be shaped by controlling the DC voltage profile applied to the individual transducer fingers in each of these arrays. Individual waves launched by each input transducer finger propagate with a relative time delay that is dictated by the distance between the fingers and acoustic phase velocity in the acoustic waveguide. The resultant stress wave generated in the waveguide, hence, can be represented by a finite weighted series of time delayed copies of the input voltage waveform, where the weights are proportional to the DC voltages applied to the fingers. The corresponding frequency response from the input voltage to the resultant stress components will then be that of an FIR filter. Assuming a traveling wave regime, the deformation sensed by the individual output transducer fingers and component currents generated by these fingers can be similarly expressed as a weighted sum of time delayed replica of the relevant strain component waveform and the frequency response the output sense current generated by the transducer array can be expressed as a second FIR filter. The frequency response from the output current to input voltage then can be expressed as the product of these two FIR frequency responses.

An advantage of using acoustic waves is that their wavelengths are on the order of microns at microwave frequencies, making it possible to miniaturize the filter structures. Usually a parallel set of acoustic waveguides are excited by another parallel set of electrodes perpendicular to the waveguides. A set of parallel waveguides has two advantages over a single continuous waveguide structure. Firstly, it increases the overall area of the transducer and its effective transduction ratio, thereby decreasing the input/output electrical impedance of the filter to the practical range of \(<200\) Ohms. Secondly, the structural isolation of thinner waveguides inherently helps to guide the acoustic waves by reducing the spread and avoids excitation of higher order modes in
the waveguide ensuring single moded operation. The intersection points of this grid of waveguides and electrodes define an array of capacitive transducers that generate controlled acoustic excitations in a mechanical structure with varying spatial delays. An advantage of using electrostatic transduction is that, by superposing appropriate DC bias voltages across the air gap capacitors, the amplitude of the induced mechanical vibrations can be linearly controlled [10]. This property will be evident in a later section where the equations of the capacitive transducer are derived. A similar piezoelectric transducer can also be realized in which a piezoelectric crystal sits in the air gap. A disadvantage of using a piezoelectric crystal is that its mechanical properties also need to be accounted for, whereas in the electrostatic case the beams are free to move in the air gap. Secondly, the amplitude of the induced mechanical vibration cannot be controlled by applying a DC bias voltage as can be done for the capacitive transducer. With the capacitive transducers, the ability to control the amplitude of excitation of the acoustic waves makes it possible to realize an FIR filter whose coefficients can be digitally programmed. DC bias voltages applied on the electrodes act as the filter coefficients of the FIR filter.

If an ideal acoustic FIR filter is successfully realized based on the concepts described in this section, it can have the following advantages –

- Fully programmable impulse response
- Adjustable input and output impedance levels
- Elimination of piezoelectric materials desirable for CMOS integration
- Bandwidth control
- High selectivity and low loss due to micromechanical structures
• High speed switching
• Tuning range of an octave with proper matching
• Miniature device
• All Chip area utilized in all modes of operation

To successfully realize the FIR filter concept, an appropriate acoustic waveguide must be chosen. In order to build a practically useful microwave filter with a sharp response, wider tuning range or matching bandwidth, low insertion loss, fast switching times and low voltage operation, certain physical characteristics of the acoustic waveguide are desired. Namely, an ideal acoustic waveguide structure should have the following mechanical properties –

• Low loss or high Q material
• Isolated uncoupled modes for single moded operation
• High mode propagation velocity to avoid aliasing at high frequencies
• Low RF spring constant (low acoustic input impedance leading to low electrical input impedance)
• High DC spring constant (high pull-in voltage)
• Negligible loading effect from anchoring structures
• Negligible leakage through the anchors into the substrate (low substrate loss)
• Mostly resistive input impedance (low electrode reactance)
• Low mechanical coupling with electrodes and anchors (unless they are part of the guiding structure)
• Easy to fabricate
In general, the overall design of the device should also have the following electrical properties –

- Good input-output electrical isolation
- Small electrical parasitics
- Low DC leakage
- No dielectric breakdown
- No field emission in airgap

In general, acoustic waveguides can support many different elastic modes. From the point of view of transduction, the mode which yields a better coupling and high mechanical input impedance is more desirable. In general, shear modes are better in this respect compared to longitudinal modes. Hence, the mode of operation chosen for the proposed embodiment to be discussed later in this dissertation is one that operates predominantly in the shear mode.
1.2 Simplified Filter Model

A simplified model of the capacitive transducer is presented here. It is then used to derive the filter response of the idealized FIR filter. A more detailed model of a capacitive transducer exciting an acoustic waveguide shown in Figure 3.2 is derived in later sections. Consider a capacitive transducer whose electrodes are separated by a distance $X_0$, has capacitance $C_0$ and across which a DC bias voltage of $V_{dc}$ is applied. The AC voltage across the transducer and the AC current flowing through the transducer is denoted by the phasors $V$ and $I$, respectively. The relative AC velocity between the electrodes of the transducer is denoted by the phasor $U$ and the AC force between them is denoted by the phasor $F$. For a transducer exciting a waveguide, if the transducer-line coupling can be neglected and the transducers do not load the line, then the transducer model can be represented by (1.1) after the transducer shunt capacitance has been cancelled out by a matching inductor.

\[
\begin{bmatrix}
V \\
I
\end{bmatrix} = \begin{bmatrix}
0 & 1/J \\
J & 0
\end{bmatrix} \begin{bmatrix}
U \\
F
\end{bmatrix}, \quad J = \frac{C_0 V_{dc}}{X_0}
\]

(1.1)

Now consider the schematic of the complete FIR filter shown in Figure 1.2. An array of $N$ capacitive transducers (input array) with pitch $d$ excites one end of an acoustic waveguide with the input RF signal $V_{in}$. The RF source has an internal system impedance $Z_0$. At the other end of the waveguide, a mirrored array of $N$ capacitive transducers (output array) picks up the filtered output signal $V_{out}$ across a load impedance $Z_L$. The matching inductor used to cancel out the total capacitance of the transducer arrays is shown by $L_{mat}$. This inductor can either be connected in series or in
parallel with $Z_0$ and $Z_L$ (here it is shown connected in series). The spacing between the two arrays is $d_c$ and the distance between the arrays the ends of the waveguide is $d_t$, as shown. The acoustic waveguide has a characteristic impedance $Z_{m0}$ and the working mode has a phase constant of $\beta$ at the operating frequency $\omega$. The characteristic impedance, which is described in more detail in later sections, is the ratio of the forward velocity wave to the forward force wave at any given location. In practice, both ends of the waveguide are either clamped or left free to reflect the backward going acoustic waves such that they add in-phase with the forward going waves at the operating frequency. $U_\Sigma$ and $F_\Sigma$ represent the phase delayed superposition of the partial acoustic waves, $U_n$ and $F_n$, generated by the transducers at the locations shown in the figure. $V_{dc}^n$ are the DC bias voltages across the capacitive transducers.
Figure 1.2 Schematic of the complete FIR filter showing the acoustic waveguide and the input and output capacitive transducer arrays. (Note: figure rotated anti-clockwise by 90 degrees)
From (1.1) and Figure 1.2, the relations shown in (1.2) can be written for the various physical quantities. Here, \( J_n = C_0 V_{dc}^n / X_0 \) and \( J_m = C_0 V_{dc}^m / X_0 \).

\[
F_n = J_n V_{in}
\]
\[
F_Z = \sum_{n=0}^{N-1} F_n e^{-j\beta m d}
\]
\[
U_Z = Z_{m0} F_Z e^{-j\beta d_c}
\]
\[
U_m = U_Z e^{-j\beta m d}
\]
\[
I_m = J_m U_m
\]
\[
I_{out} = \sum_{m=0}^{N-1} I_m
\]
\[
V_{out} = -Z_L I_{out}
\]

These relations can be used to obtain the following simplified overall filter response \( H(\omega) \) of the idealized FIR filter. Here, \( v_p \) is the phase velocity of the working mode.

\[
V_{out}(\omega) = H(\omega)V_{in}(\omega)
\]

\[
H(\omega) = -Z_L Z_{m0} \frac{C_0^2}{X_0^2} e^{-j\beta d_c} \sum_{n=0}^{N-1} V_{dc}^n e^{-j\beta m d} \sum_{m=0}^{N-1} V_{dc}^m e^{-j\beta m d}. \quad \beta = \omega / v_p
\]
1.3 Electrical Connections

An illustration showing how the DC bias voltages and the RF input and output signals are electrically connected to the filter, is shown in Figure 1.3. For better clarity, only \( N = 2 \) transducers are shown in both the input and output arrays, exciting a single acoustic waveguide (\( M = 1 \)). Each transducer has its own independently tunable DC bias source, shown by \( V^{1}_{dc} \) and \( V^{2}_{dc} \) in the figure. Resistors used to isolate the RF signals from the DC path are shown by \( R_{block} \). These resistors can be on-chip or off-chip. Since there is no DC current in the circuit, all the DC voltage appears across the transducers. RF chokes can be used instead of the resistors if they can be fabricated with a small footprint. The DC bypass capacitors used to block the DC voltages are shown by \( C_{RF} \), and are usually implemented as metal-insulator-metal (MIM) on-chip capacitors. They have to be designed appropriately so that they offer very little impedance to the RF signal. \( C_{ox} \) represents the capacitance of a thermal oxide layer that is usually added in series inside the capacitive transducers to prevent the DC paths from shorting should the transducers experience pull-in. Although, if \( R_{block} \) is high enough, then this capacitance may not be required. Again, it should be ensured that this capacitance offers negligible impedance to the RF signals. The DC air-gap capacitance of the capacitive transducers is denoted by \( C_{0} \). The input RF signal source is shown by \( V_{in} \) and has an internal source impedance \( Z_{0} \). The output RF signal denoted by \( V_{out} \) is measured across a load impedance \( Z_{L} \). \( L_{match} \) is the on-chip or off-chip matching inductor used to cancel out the total DC shunt capacitance of the transducer arrays. It can either be connected in series or in parallel with \( Z_{0} \) and \( Z_{L} \) (here it is shown connected in series).
Figure 1.3 Illustration showing the electrical connections of the DC bias voltages and the RF input and output signals to the capacitive transducers.

1.4 Thesis Overview

In Chapter 0, the basic concept behind the proposed programmable acoustic filter was discussed along with a simplified model of the idealized filter. The proposed device is composed of an input array of capacitive transducers, an acoustic waveguide and an output array of capacitive transducers. Chapter 2 discusses the equivalent circuit modeling of the capacitive transducers, the acoustic waveguide, and the interface between the transducers and the waveguide. An example waveguide structure is introduced to aid in this discussion. In Chapter 3, a general theory of an array of transducers exciting a waveguide, like the one encountered in this filter design, is discussed and its application is demonstrated for an example waveguide structure. This general theory is applied to the models developed in Chapter 2 to derive a set of design equations that will guide the filter design process. A circuit simulator developed to simulate the entire filter response is discussed in Chapter 4. Chapter 5 presents an
example filter design with parameters optimized using the design equations of Chapter 3. Simulation results, including filter responses, obtained using the circuit simulator for this filter design are also presented and compared to the filter performance estimated by the design equations in order to verify those equations. A process flow for fabricating a filter structure similar to the example structure is briefly presented along with a brief discussion of electrical parasitic effects. It should be mentioned that the actual historical timeline of the project was different than the order in which the work has been presented in this dissertation. Due to the limited time frame of this project, a filter design based on the ridge waveguide was finalized for fabrication in the earlier phases of the project. Its analysis was done using some preliminary techniques that were developed earlier in the project. These techniques and a few of the filter geometries that were studied, especially, the tethered beam waveguide and the ridge waveguide are briefly discussed in Chapter 6. Unfortunately, due to fabrication difficulties, the ridge based design was not successful, and due to monetary constraints, other designs could not be fabricated and tested. Consequently, the research efforts were diverted towards analyzing and modeling the filter in more detail. The outcome of that later research is what has been presented in the chapters before Chapter 6. Chapter 7 discusses a semi-analytical method to obtain propagating elastic modes of a ridge waveguide etched in an anisotropic crystal. Chapter 8 explains in detail the microfabrication process flow that was followed in order to fabricate a filter based on the ridge waveguide. It also talks about the layout generation and the challenges faced during the fabrication. Finally, Chapter 9 discusses some of the future work and possible ways to improve the design of the filter.
In this chapter, the electromechanical model of a capacitive transducer exciting an acoustic waveguide is discussed in detail. The same model also holds for the capacitive transducers that sense the wave propagating through the acoustic waveguide. In Section 2.1, the standard Mason’s model of the transducer is derived from basic principles. Section 2.2 discusses the equivalent circuit modeling of the acoustic waveguide and transducer-line coupling using a simple example waveguide structure.

2.1 Capacitive Transducer

To derive the equivalent circuit model of a capacitive transducer, we assume the transducer can be represented as the two electrodes of an air-filled parallel plate capacitor with the area \( A \) and electrode separation \( x_{cap} \). If a voltage \( v \) is applied across the electrodes, then an attractive force of magnitude \( f \propto v^2 \) is experienced by the electrodes. Depending on the dynamical conditions of the electrodes, this force can lead to changes in the plate separation \( x \) between the electrodes. The current induced in the capacitor can be shown by \( i \) and corresponds to the variations in the capacitor charge resulting from the changes in the voltage as well as the capacitance. Assuming that voltage consists of a DC component \( V_{dc} \) and an sinusoidal (AC) component \( v_{ac} \), the force, displacement and current, each will contain components at DC as well as the fundamental and generally harmonic frequency of the applied AC voltage. Under small signal conditions \( v_{ac} \ll V_{dc} \), higher order harmonic terms in these quantities can be neglected leaving the DC components \( F_{dc} \), \( X_{dc} \), and AC component phasors \( F_{ac} \), \( X_{ac} \) and \( I_{ac} \). It is clear that the capacitor current cannot have a DC component. The DC
component of displacement can also be neglected in the first order approximation under small signal conditions. A capacitive transducer and related parameters are illustrated in Figure 2.1.

![Figure 2.1 A basic diagram illustrating the capacitive transducer and associated physical quantities.](image)

The DC capacitance $C_0 = \varepsilon_0 A_e / X_0$ and the DC electric field magnitude $E_{dc} = V_{dc} / X_0$ can be used to define two quantities, $J = C_0 E_{dc}$ and $B = \omega C_0$, which will be used later to simplify the model equations. Here, $\omega$ is the angular frequency of the AC components.

The relative velocity of the electrode plates will be represented by $u = dx/dt$ with the AC component $U_{ac} = j\omega X_{ac}$. It is noted that like current, the velocity does not have a DC component. If $x$ is the instantaneous plate separation and $C$ is the instantaneous capacitance of the transducer, then the instantaneous charge $q$ of the capacitor can be written as:
\[ q = Cv \]
\[ = \frac{\varepsilon_0 A_e}{x} V \]
\[ \approx \frac{\varepsilon_0 A_e}{(X_0 - x_{ac})}(V_{dc} + v_{ac}) \]
\[ \approx \frac{\varepsilon_0 A_e V_{dc}}{X_0} \left(1 + \frac{v_{ac}}{V_{dc}} \right) \left(1 + \frac{x_{ac}}{X_0} \right) \]
\[ = \frac{\varepsilon_0 A_e V_{dc}}{X_0} + \frac{\varepsilon_0 A_c}{X_0} v_{ac} + \frac{\varepsilon_0 A_e V_{dc}}{X_0^2} x_{ac} \]
\[ = C_0 V_{dc} + \text{Re} \left[ (C_0 V_{ac} + C_0 E_{dc} X_{ac}) e^{j\omega} \right] \] (2.1)

The current \( i \) can then be obtained by taking the time derivative of \( q \) as follows:

\[ i = \text{Re} \left[ j\omega (C_0 V_{ac} + C_0 E_{dc} X_{ac}) e^{j\omega} \right] \] (2.2)

A more useful representation of this current can be given in frequency domain as:

\[ I_{ac} = j\omega C_0 V_{ac} + C_0 E_{dc} U_{ac} \] (2.3)

The current does not have any DC component, as expected, due to the transducer capacitance. Thus, even though the transducer often requires large DC voltages to operate, it does not consume any DC power. If \( E \) is the magnitude of the total electric field, then the contribution to the electric field by only one electrode will be \( E/2 \) due to symmetry. Hence, the magnitude of the instantaneous electric force \( f \) between the electrode plates can be derived as shown below.
\[ f = \frac{qE}{2} \]
\[ = \frac{Cv^2}{2x} \]
\[ = \frac{\varepsilon_0A\varepsilon}{2x^2} \]
\[ \approx \frac{\varepsilon_0A_\varepsilon}{2x^2} \left( V_{dc} + v_{ac} \right)^2 \]
\[ \approx \frac{\varepsilon_0A_{dc}}{2X_0^2} \left( 1 + 2 \frac{v_{ac}}{V_{dc}} \right) \left( 1 + 2 \frac{x_{ac}}{X_0} \right) \]
\[ = \frac{C_0V_{dc}^2}{2X_0} \left( 1 + 2 \frac{v_{ac}}{V_{dc}} + 2 \frac{x_{ac}}{X_0} \right) \]
\[ = \frac{C_0V_{dc}^2}{2X_0} + C_0E_{dc}v_{ac} + C_0E_{dc}^2x_{ac} \]

In the expression for total force, the first term is recognized as the magnitude of the DC component of the force, \( F_{dc} = C_0V_{ac}^2/2X_0 \), while the rest represents the AC force. The expression for current in (2.3) and the magnitude of the AC component of force \( F_{ac} \) in (2.4) can be written in terms of \( J \) and \( B \) as follows:

\[
I_{ac} = jBV_{ac} + JU_{ac} \\
F_{ac} = JV_{ac} + J^2 U_{ac} = J \left( V_{ac} - \frac{I_{ac} - jBV_{ac}}{-jB} \right)
\]

where \( X_{ac} \) has been replaced by \( U_{ac}/j\omega \). The equations in (2.5) constitute the first-order linear model of a capacitive transducer. This model essentially relates the electrical quantities \( V_{ac} \) and \( I_{ac} \) to the mechanical quantities \( U_{ac} \) and \( F_{ac} \). It can be shown that these equations correspond to the equivalent circuit model of Figure 2.2,
where the block element represents the electromechanical transmission equations between the electrical and mechanical domains:

\[
\begin{bmatrix}
V_{ac}' \\
I_{ac}'
\end{bmatrix}
= T^{EM}
\begin{bmatrix}
U_{ac} \\
F_{ac}
\end{bmatrix}
\tag{2.6}
\]

where primed quantities refer to the electrical voltage and current at the input of the block and \( T^{EM} \) is the electromechanical transmission matrix given by:

\[
T^{EM} = \begin{bmatrix}
0 & 1/J \\
J & 0
\end{bmatrix}
\tag{2.7}
\]

**Note:** In this dissertation, the symbol \( T \) with subscripts or superscripts usually represents the 2-port transmission matrices, unless mentioned otherwise, as in Chapter 4 and Chapter 7.

![Figure 2.2 Circuit model of the capacitive transducer with two capacitors and an impedance inverter.](image)

Positive directions of the current and voltage in the electrical port (left) follow to the convention that the voltage-current product must yield the power entering the port. On the other hand, with the above definitions of attraction force and velocity, the product of these quantities yields power delivered from the mechanical port to an external load. The
annotated direction of the force arrow on the right side of Figure 2.2 simply refers to the fact that a positive product corresponds to an output power flow.

In terminology of electrical networks, an electrical two-port with the transmission matrix of (2.7) can be recognized as an admittance inverter, with $J$ being the inversion ratio. The most important characteristic of an inverter is that its input admittance $Y_{in}$ is equal to the inverse of the load admittance $Y_L$ times $J^2$. Treating the AC velocity as a mechanical analog of voltage and AC force as the mechanical analog of current, and defining a mechanical admittance $Y^M$ as the ratio $\frac{F_{ac}}{U_{ac}}$, the electromechanical admittance, an electromechanical impedance inversion equations can be obtained for the present case as follows:

$$Y_{in} = \frac{J^2}{Y_L^M} \quad (2.8)$$

where the subscript $L$ refers to the load. Notably, (2.6) and (2.7) guarantee that the sum of the electrical and mechanical powers entering the element is zero. This is an important observation, because it indicates that in spite the DC bias the transducer cannot be used as to amplify or attenuate the signal. One must also note that the concept of reciprocity cannot be directly applied between the two domains. As a result, although the transducer is passive and made of reciprocal elements, the electromechanical transmission matrix does not have a unity determinant as predicted by circuit theory. The standard circuit model of Figure 2.2 involves two capacitors and an admittance inverter. The overall transmission matrix of this circuit can be written as:
\[
T_{\text{trans}} = \begin{bmatrix}
1 & 0 & 1 & j/B & 0 & 1/J \\
0 & 1 & jB & 0 & j/B & 0 \\
J & 0 & 0 & 1 & 0 & 0
\end{bmatrix}
\] (2.9)

By adding and subtracting a series capacitor on the electrical side, two other forms of the circuit model involving another inverter and a transformer can be obtained as shown in Figure 2.3 and Figure 2.4.

\[
T_{\text{trans}} = \begin{bmatrix}
1 & 1/jB & 0 & j/B & 0 & 1/J \\
0 & 1 & jB & 0 & j/B & 0 \\
J & 0 & 0 & 1 & 0 & 0
\end{bmatrix}
\] (2.10)

![Figure 2.3](image)

Figure 2.3 Circuit model of the capacitive transducer with one capacitor and two impedance inverters.

\[
T_{\text{trans}} = \begin{bmatrix}
1 & 1/jB & 0 & jE_{\text{dc}}/\omega & 0 \\
0 & 1 & jB & 0 & j\omega/E_{\text{dc}} \\
\end{bmatrix}
\] (2.11)

![Figure 2.4](image)

Figure 2.4 Circuit model of the capacitive transducer with a capacitor, transformer and a 90 degree phase shifter.
2.1.1 Electrically Large Electrodes

In a practical structure, the electrode plates in general will not be parallel to each other if the electrode dimensions are comparable to the wavelength of the acoustic mode at the frequency of operation. If the curvature of the surfaces is small then the electrode can be treated as a composite of several infinitesimal electrodes in parallel and, $E_{dc}$ and $X_0$ can be assumed to be constant over the area of the electrode. Also, $V_{ac}$ is constant over the area of the electrode. If the velocity distribution and the AC pressure over the area of the electrode are represented, as a function of lateral coordinates $y$ and $z$, by $U_e(y, z)$ and $P_e(y, z)$, respectively, then the equations for a transducer of infinitesimal area can be derived from (2.5) as:

\[
V_{ac} dA_e = \frac{jE_{dc}}{\omega} U_e(y, z) dA_e + \frac{X_0}{j\omega\varepsilon_0} dI_{ac}
\]

\[
dI_{ac} = \frac{j\omega}{E_{dc}} P_e(y, z) dA_e
\]

(2.12)

where $dA_e$ is the incremental electrode area. Integrating these equations over the area of the entire capacitive region with area $A_e$ leads to:

\[
V_{ac} = \frac{jE_{dc}}{\omega} \frac{1}{A_e} \int U_e(y, z) dA_e + \frac{1}{j\omega\varepsilon_0} I_{ac}
\]

\[
I_{ac} = \frac{j\omega}{E_{dc}} \int P_e(y, z) dA_e
\]

(2.13)
(2.13) indicates that the circuit model of (2.5), and subsequently any of its equivalent forms, can be used in the general case as long as the velocity and force are interpreted as the following:

\begin{align*}
U_{ac} &= \frac{1}{A_e} \int U_e(y, z) dA_e \\
F_{ac} &= \int P_e(y, z) dA_e
\end{align*}

(2.14)

In other words, in the transducer model, \( U_{ac} \) represents the average velocity and \( F_{ac} \) stands for the total AC force, both over the area of the electrodes. These equations will be used later to define the field quantities for a mechanical transmission line. From here onwards, the ‘ac’ subscript in \( V_{ac} \), \( I_{ac} \), \( U_{ac} \) and \( F_{ac} \) will be dropped and unsubscripted symbols will be used to refer to the AC components of those physical quantities.
2.2 Mechanical Transmission Line

In this section, the process of modeling the equivalent circuit of the mechanical interface and the acoustic transmission line will be illustrated with the help of a simple waveguide structure. A cross sectional view of a block of this waveguide structure is shown in Figure 2.5.

It consists of a strip of single crystal Silicon of width $y_{\text{elec}}$ and thickness $x_{\text{wg}}$, separated from the substrate by a small air gap $x_{\text{cap}}$. The propagation takes place along the $z$-axis and, the transducer electrodes of width $y_{\text{elec}}$ and length $z_{\text{elec}}$ are placed at several locations along that direction to excite a propagating wave. It should be noted that the figure only shows a quarter section of one transducer and the arrows depicting the
symmetric boundary conditions are in reference to an analysis that will be discussed later. The capacitive transducer is formed by the conductive electrode surfaces on the lower face of the waveguide and the upper face of the substrate. The attraction between these electrodes bends the Silicon strip and this disturbance propagates along the waveguide. This structure will be referred to as the *Strip waveguide*.

### 2.2.1 Modal Analysis

Once the general structure of the waveguide is conceptualized, the next step is to identify the propagating modes and determine the dimensions of the waveguide based on the desired operating bandwidth. To that effect, a Modal analysis is performed on a small section of the waveguide that acts as a resonator, as shown in Figure 2.6, using the commercial finite element simulation software ANSYS. The block has a length of $z_{res}$, a width of $y_{res}$ and a thickness of $x_{res}$. Boundary conditions on the nodal velocities $v_x$, $v_y$ and $v_z$ enforced on the various faces of this block are shown in (2.15). Since the actual acoustic delay line in the proposed filter will utilize a large number of parallel waveguides expected to achieve practical impedance values, periodic boundary conditions can be used along $y$, which in this case reduce to a symmetry condition at the $y = y_{res}$ plane. The boundaries not mentioned in (2.15) are ‘free’, which means that the traction components obtained as the dot product of the stress field and the surface normal are zero. The Modal analysis essentially yields the various resonant modes of the block and their resonant frequencies. The boundary conditions are set in such a way that the length of the block, $z_{res}$, will correspond to half the wavelength of the propagating modes.
Figure 2.6 Cross-sectional view of a small section of the waveguide that is used in the ANSYS modal analysis.

\[ v_x = v_y = v_z = 0 \text{ at } x = -x_{res} \]
\[ v_y = 0 \text{ at } y = 0, y_{res} \]
\[ v_z = 0 \text{ at } z = 0, z_{res} \]  

(2.15)

A block of size \( x_{res} = 2 \text{ um} \) and \( y_{res} = 4.5 \text{ um} \) is meshed with the element SOLID185 to determine the first and second lowest resonant frequencies. As block length \( z_{res} \) becomes one half of a wavelength at each of these frequencies at the corresponding resonant mode, the phase constant along \( z \) can be calculated as \( \pi/z_{res} \). The dispersion curves for the first and second modes can be generated by repeating this analysis for different values of \( z_{res} \) in the range of 2 um to 30 um and plotting phase constant vs. modal resonant frequencies. Figure 2.7 shows the solution for the first two modes for waveguide with dimensions \( x_{wg} = 0.5 \text{ um} \) and \( y_{elec} = 3 \text{ um} \) and with a block.
length of $z_{res} = 2.5$ um. Corresponding resonant frequencies were found as 516 MHz and 1343 MHz.

Noting that neither of these modes can exist at DC, the single moded band of operation of the waveguide will be a bandpass region marked by the cutoff frequencies of the first and second propagating modes. These cutoff frequencies correspond to a zero phase constant along $z$ and can be found by eigen mode analysis of the block structure with $z_{res}$ approaching infinity. For the above dimensions, the single moded band of operation spans approximately from 325 MHz to 1200 MHz. In practice, one must avoid operation close the two extremes, due to the large group delay near the lower end and reactive loading by the second mode near the upper end of the band. In the present case, a practical operational band of 500-1000 MHz will guarantee single moded behavior with some margin left on both ends.

Figure 2.7 ANSYS Modal analysis showing the first two resonant modes for a block of waveguide with dimensions: $x_{res} = 2$ um, $y_{res} = 4.5$ um, $z_{res} = 2.5$ um, $x_{wg} = 0.5$ um and $y_{elec} = 3$ um. For a block of this length, mode 1 (left) has a resonant frequency of 516 MHz and mode 2 (right) has a resonant frequency of 1343 MHz. The color shows the nodal displacement in the $x$ direction. Green corresponds to zero displacement in the $x$ direction.
2.2.2 Harmonic Analysis

The eigenvalue analysis of the waveguide determines its basic modal characteristics and dispersion properties that can help choose the waveguide dimensions for the desired operating band. However, the resonant model is over simplified, in the sense that it does not include the effect of loss mechanisms such as substrate leakage, and that it imposes certain desired modal characteristics through boundary conditions that may not necessary represent the reality of the situation. Also, this model does not provide any information about the coupling between the transducers and the waveguide.

To model this fundamental mode in the propagating regime and work out the waveguide model parameters as a transmission line and also determine possible mechanical
parasitic elements in the equivalent circuit for the coupling between the waveguide and individual transducer electrodes, an analysis can be used. This is done by conducting a Harmonic analysis in ANSYS on a long waveguide section terminated on both ends by matched loads and excited using a force applied to a rectangular region representing the electrodes of a single transducer and repeating the analysis for adequate number of frequency points within the band of interest. The matched loads are emulated by perfectly matched layers (PML’s) which consist of layered structures with gradually increasing damping ratios. Computations can be simplified by simulating only a quarter section of the waveguide and the transducer by exploiting the symmetry of the structure. Also, as discussed earlier, an additional symmetry condition can be applied at the $y = y_{har}$ plane [See Figure 2.5] since a large number of parallel waveguides are utilized to achieve practical impedance values. Ideally, $y_{har}$ should be set equal to $y_{res}$ in order to obtain a modal field distribution that is close to the one obtained in the modal analysis.

The simplified structure used in the Harmonic analysis is shown in Figure 2.9 and the applied symmetry boundary conditions are given as:
The length of the force region that corresponds to the $z$ dimensions of a single electrode is related to the spacing between adjacent electrodes. Digital filter theory provides that to avoid formation of spurious pass-bands within the frequency range of operation, time samples of the FIR impulse response must be not be smaller than the Nyquist rate. This requires that the separation between adjacent fingers in the input and output transducer arrays is kept to less than one half of the wavelength at the highest frequency of interest. According to Figure 2.8, for an upper band frequency of 1000 MHz, this results in a maximum finger spacing of 1.4 um. Allowing for some spacing between the transducer electrodes, we chose the practical value of $z_{elec} = 1$ um for the electrodes.
In the Harmonic analysis, a constant pressure of 1 Pa is applied on the surfaces of both the electrodes of the transducer located within $0 < z < z_{elec}/2$ and $0 < y < y_{elec}/2$ and the simulation is run over the operating bandwidth. The graphic representation of the $x$ directed nodal displacement calculated for the frequency point of 750 MHz is shown in Figure 2.10.

![Image](image.png)

Figure 2.10 Result of the ANSYS Harmonic analysis at 750 MHz showing the fundamental mode 1 propagating along the waveguide. The applied pressure on the transducer is 1 Pa. The color shows the nodal displacement in the $x$ direction which has been amplified by a factor of $3 \times 10^{10}$ for better visualization. Green corresponds to zero displacement in the $x$ direction.

In order to model the waveguide mode as a mechanical transmission line, field quantities need to be defined in a way that is consistent with the transducer model. Motivated by the definition in (2.14), the *mechanical voltage* along the line, $U(z)$, is defined in (2.17) as the average surface velocity of the waveguide computed by a moving average filter working over an area equal to the area of electrode $A_e = y_{elec} z_{elec}$.
The mechanical characteristic impedance or acoustic characteristic impedance of the line can be defined based on the power flowing in the waveguide. The complex mechanical power flowing in the waveguide, \( P_f(z) \), is obtained by integrating the complex pointing vector, derived in [11], over the cross section of the waveguide as,

\[
P_f(z) = \int_{-z_{wg}}^{0} \int_{-z_{elec}}^{z_{elec}} \left(-\vec{V}^* \cdot \hat{T}\right) \cdot \hat{z} \, dx dy
\]  

(2.18)

where \( \vec{V} \) is the particle velocity vector. Theoretically, for a propagating mode the mechanical characteristic impedance \( Z_{m0} \) can be found by calculating the ratio \( \frac{|U|^2}{P_f} \) at any given cross section of the line. In reality, however, due to the approximate nature of the PML and the presence of evanescent modes near the excitation region, this ratio exhibits some dependence on \( z \). To minimize the effect of evanescent modes and modeling errors, we will use the average impedance defined by (2.19), computed over the interval \([z_i, z_i + z_{len}]\), where \( z_i \) is chosen a few wavelengths away from the transducer to minimize the reactive effect of evanescent modes.

\[
Z_{m0} = \frac{1}{z_{len}} \int_{z_i}^{z_i + z_{len}} \frac{|U(z)|^2}{\text{Re} \left[ P_f(z) \right]} \, dz = \left\langle \frac{|U(z)|^2}{\text{Re} \left[ P_f(z) \right]} \right\rangle
\]  

(2.19)
Ideally, if the mode is terminated in a matched load, $P_f(z)$ should be purely real. If there are any reflections and reactive effects, it can have a small imaginary component. Here we neglect these imaginary components and use only the real part of power for calculating the mechanical impedance. Finally, the *mechanical current* along the line, $F(z)$, which has the units of force, is defined as,

$$ F(z) = \frac{U(z)}{Z_{m0}} $$

(2.20)

The characteristic impedance computed for the waveguide structure of Figure 2.5 is plotted vs. frequency in Figure 2.11. The frequency behavior of this impedance is similar to that of TE modes in electromagnetic waveguides.

Figure 2.11 Mechanical characteristic impedance of the fundamental mode of the waveguide as a function of frequency within the operating bandwidth obtained from the ANSYS Harmonic analysis.
The results of the Harmonic analysis can also be used to compute the wavelength. This can be done by estimating the spatial frequency of the wave flowing along the waveguide. Intuitively, the obvious choice is to use the FFT to obtain the spatial frequency. Unfortunately, for the same meshing resolution, the number of data points in one wavelength becomes less at higher frequencies and hence, the spatial frequency cannot be estimated accurately. A better method is to use an optimization technique, wherein, the phase factor along a certain length of the wave is de-embedded to a fixed point using various trial values for the wavelength (or phase constant). As can be expected, the value of the wavelength that gives the least standard deviation in the de-embedded phase factors is the wavelength of the wave. Mathematically, estimate $\beta$ such that $f(\beta)$ in (2.21) is minimized.

$$f(\beta) = \sigma_z \left( \frac{V_x(-x_{wg},0,z) e^{j\beta z}}{V_x(-x_{wg},0,z)} \right)$$

(2.21)

where $\sigma_z$ is the standard deviation taken over several mesh nodes along the $z$ direction.

As frequency sweep is built into the Harmonic analysis this approach allows for the dispersion curves to be generated from a single simulation, as opposed to the method explained earlier in this section which requires repetitive execution of Modal analysis. The wavelength obtained from the Harmonic analysis using this method is plotted in Figure 2.12 along with the result of the Modal analysis. Clearly, the two curves closely follow each other.
2.2.3 Transducer-Line Coupling Model

In addition to the transmission line characteristic impedance $Z_{m0}$ and propagation constant $\beta$, the Harmonic analysis can be used to derive an equivalent circuit for the coupling between the transducer and waveguide. A generic model for the coupling can be considered as the combination of a series mechanical impedance $Z_m$ and a parallel mechanical admittance $Y_m$. The simulation set up of Figure 2.9 then can be equivalent to the circuit model of Figure 2.13, with PML’s replaced with matched terminations on both sides of the transmission line. It is assumed that the line is lossless. The mechanical voltages and currents shown in this circuit model are defined in (2.22).
The mechanical voltage $U_1$ on the input side represents the average relative velocity between the electrodes of the transducer, and is essentially (2.17) evaluated at the location of the transducer subtracted by the average velocity of the other electrode surface which is not on the waveguide. The mechanical current source $F_1$ represents the applied input force in the simulation and acts as the excitation source. The mechanical voltage $U_2$ on the output side of the mechanical transmission matrix $T^M$, is the velocity in (2.17) calculated at a certain distance from the transducer divided by the appropriate phase factor so as to obtain its value at the location of the transducer. Again, to minimize the effect of the approximate nature of the PML and the presence of evanescent modes near the excitation region, the average value computed over the interval $[z_1, z_1 + z_{\text{len}}]$, is
used. Finally, the mechanical current $F_2$, on the output side is found from the impedance offered by the doubly matched line, $Z_m/2$. Figure 2.14 shows the values of these field quantities computed from the output of the Harmonic analysis. It is seen that the imaginary parts of $U_2$ and $F_2$ are nearly zero. The slight fluctuations can be attributed to simulation errors. Hence, these imaginary parts will be ignored in subsequent calculations. As per the circuit model of Figure 2.13, the values of $Z_m$ and $Y_m$ calculated from $U_1$, $F_1$, $U_2$ and $F_2$ as follows:

$$Z_m = \frac{U_1 - U_2}{F_1}$$

$$Y_m = \frac{F_1 - F_2}{U_2}$$

The values of $Z_m$ and $Y_m$ for the previous example are shown in Figure 2.15. It is observed that the real part of $Z_m$ is nearly zero, thus it will be ignored in subsequent calculations. Since, the imaginary part of $Z_m$ is negative, it is modeled by a frequency dependent capacitor $C_m$. Also, the imaginary part of $Y_m$ is identically zero. Thus, $Y_m$ can be effectively modeled by a frequency dependent resistor $R_m$. The values of these circuit elements are calculated from (2.24).

$$C_m = \frac{-1}{\omega \text{Im}[Z_m]}$$

$$R_m = \frac{1}{\text{Re}[Y_m]}$$

(2.24)
Figure 2.16 shows the computed values for $C_m$ and $R_m$ found in this way. The fluctuations in these values can be attributed to simulation errors and smoothed out using a polynomial curve fitting, as shown in the plots.

Figure 2.14 Values of the mechanical voltages and currents, depicted in Figure 2.13, computed from the output of the ANSYS Harmonic analysis.
Figure 2.15 Values of the transducer-line coupling elements, $Z_m$ and $Y_m$, shown in Figure 2.13, computed from the output of the ANSYS Harmonic analysis.
Figure 2.16 Values of the frequency dependent parasitic capacitor $C_m$, and the frequency dependent parasitic resistor $R_m$, computed from the output of the ANSYS Harmonic analysis.
The described circuit model of the transducer-line coupling interface provides some physical insight into working of the capacitive transducer. The capacitor \( C_m \) can be thought of as the reactance of the transducer electrode, while the resistor \( R_m \) can be thought of as the loss into the substrate. As will be seen later, this substrate loss plays an important role in the performance of the filter. To summarize, the circuit model of the mechanical transmission matrix is shown in Figure 2.17 and the corresponding equations are shown in (2.25). Even though this circuit model was developed using the waveguide structure shown in Figure 2.5, it is expected to be descriptive of any general acoustic waveguide structure and transducer electrodes spanning over a finite length of the waveguide.

![Figure 2.17](image)

Figure 2.17 Circuit model of the mechanical transmission matrix obtained from the ANSYS Harmonic analysis.

\[
\begin{align*}
\begin{bmatrix}
U_1 \\
F_1
\end{bmatrix}
&= T^m \begin{bmatrix}
U_2 \\
F_2
\end{bmatrix} \\
T^m &= \begin{bmatrix}
1 + Y_m Z_m & Z_m \\
Y_m & 1
\end{bmatrix} \\
&= \begin{bmatrix}
1 + \frac{1}{j \omega R_m C_m} & \frac{1}{j \omega C_m} \\
\frac{1}{R_m} & 1
\end{bmatrix}
\end{align*}
\]
2.2.4 Static Analysis

When designing an acoustic waveguide excited by a capacitive transducer, an important consideration is the pull-in voltage $V_p$. The pull-in voltage is a function of the transducer dimensions as well as the effective spring constant $k_{\text{eff}}$ (38). To determine $k_{\text{eff}}$, a Static analysis is performed in ANSYS by applying a uniform DC pressure $P_e$ on the transducer electrodes. The visualization of the $x$ directed nodal displacement obtained using such an analysis for an applied DC pressure of 1 Pa is shown in Figure 2.18. $k_{\text{eff}}$ can be calculated from the ratio of the total force to the average of the relative $x$-directed nodal displacement distribution of the electrode surfaces $\delta_x$, as given by (2.26).

The pull-in voltage can then be calculated from (2.26).

![Figure 2.18 Result of the ANSYS Static analysis. The applied DC pressure on the transducer is 1 Pa. The color shows the nodal displacement in the $x$ direction which has been amplified by a factor of $1 \times 10^{10}$ for better visualization. Blue corresponds to zero displacement in the $x$ direction.](image)

$$k_{\text{eff}} = \frac{F_{dc}}{X_{dc}} = \frac{\int \int \int P_e (-x_{wg}, y, z) dy dz}{\int \int \int \frac{1}{y_{elec}} \delta_x (-x_{wg}, y, z) dy dz}$$

$$V_p = \sqrt{\frac{8k_{\text{eff}} x_{cap}^3}{27 \varepsilon_0 A_e}}$$
Chapter 3
ARRAY OF CAPACITIVE TRANSDUCERS

In this chapter, a theoretical model for an array of capacitive transducers exciting an acoustic waveguide is discussed. General equations for a transducer array are developed in Section 3.1. Section 3.2 then applies those equations to a specific model of the capacitive transducer exciting an acoustic waveguide, developed in the previous section, to obtain a set of design equations that aid in the filter design process.

3.1 General Theory

In Section 2.1, the transmission matrix of a single capacitive transducer was derived. In this section, a general approximate transmission matrix of an array of transducers exciting a waveguide or transmission line is discussed. This will be helpful in understanding some important properties of such an array. In general, the equations governing the properties of a general array of transducers are quite involved and cannot be derived analytically. The properties of a general array can only be computed numerically using circuit simulators if the appropriate equivalent circuit model is available. Here, a special case of an array of transducers will be considered whose properties can be derived analytically. As shown in Figure 3.1, consider an array of \( N \) transducers periodically located on a transmission line with characteristic impedance \( Z_m \) and propagation constant \( \beta \). It will be assumed that the transmission line is lossless and is terminated in a matched load at both ends. All transducers are separated by a constant pitch distance \( d \).
Figure 3.1 Schematic diagram of an array of $N$ generalized transducers exciting a transmission line terminated in a matched load at both ends.

In addition to a phase factor, the transducers are assumed to have a generalized transmission matrix $T$, expressed in (3.1), that relates the electrical and mechanical domains.

$$T = \begin{bmatrix} T_A & T_B \\ T_C & T_D \end{bmatrix}, \quad \Delta = -1$$  \hspace{1cm} (3.1)$$

The phasing of the transducer coefficients is usually designed so that the partial waves launched by individual transducers add in phase at frequency $\omega_0$ while propagating along the transmission line in the direction of interest. To accomplish this, if $\beta_0$ is the phase constant at $\omega_0$, then the transmission matrix of the $n^{th}$ transducer must be set to the value shown in (3.2).

$$T^n = T e^{j\beta_0 nd}, \quad n = 0, 1, \ldots, N - 1$$  \hspace{1cm} (3.2)$$
The electrical inputs of all transducers are connected and raised to a potential $V$ which draws a total current $I$ from the source. The Nyquist theorem dictates that $\beta_0 d \leq \pi$ in order to avoid aliasing. When $\beta_0 = \pi/d$, the input current $I$ is divided between the $N$ transducers equally, as depicted in Figure 3.1. This condition has been verified with circuit simulators. If $-C_0$ in Figure 2.2 is large and the transducer-line coupling can be neglected, it can be intuitively seen that this condition is indeed satisfied. In such a case, it can be shown that in the absence of RF voltage, transducers present a negligible loading effect to the transmission line. As a result, superposition can be used by considering one transducer at a time to compute the total force induced in the line. Since the RF voltage is the same, the force generated by transducers is proportional to their applied bias voltages. Thus, when $\beta_0 = \pi/d$, the current is equally divided between all transducers. For frequencies close to the center frequency, this condition can be approximately assumed to hold true. In summary, when the condition in (3.3) is satisfied ($\beta$ is the phase constant at the test frequency), the input current to all $N$ transducers is approximately equal and the transducer phase factors are approximately an alternating sequence of $+1$ and $-1$. All the results derived in this section are valid only when this condition is satisfied.

$$\beta \sim \beta_0 \sim \pi/d$$  \hspace{1cm} (3.3)

From Figure 3.1, the physical quantities related to the transducer can be written as,

$$\begin{bmatrix} V \\ I/N \end{bmatrix} = T^n \begin{bmatrix} U_n \\ F_n \end{bmatrix}$$  \hspace{1cm} (3.4)
It should be mentioned here that, in practice it is not possible to control the complex phase factors of the transmission matrix in (3.2). Thus, the transducers are biased so as to launch partial waves in both the forward and backward directions, which relates the physical quantities as,

\[
\begin{bmatrix}
U_n \\
F_n
\end{bmatrix} = T^{-1} \left( \frac{e^{-j\beta_{nd}} + e^{j\beta_{nd}}}{2} \right) \begin{bmatrix}
V \\
I/N
\end{bmatrix}
\] (3.5)

It is readily seen that the transducer transmission matrices can now be expressed using a real scaling factor as shown in (3.6) which can be easily controlled with the appropriate biasing. In general, this real scaling factor is discretized to a finite number of levels to reduce the required number of bias levels.

\[
T^n = T/\cos(\beta_{nd}) \quad , \quad n = 0, 1, ..., N - 1
\] (3.6)

To simplify the analysis, we will continue using the transmission matrix in (3.2), without loss of generality. Thus, (3.4) can be expanded using (3.1) and (3.2) as,

\[
\begin{aligned}
U_n &= \left( -T_D V + T_B \frac{I}{N} \right) e^{-j\beta_{nd}} \\
F_n &= \left( T_C V - T_A \frac{I}{N} \right) e^{-j\beta_{nd}}
\end{aligned}
\] (3.7)
As shown in Figure 3.1, $U_0$ and $U_{N-1}$ are the mechanical voltages at either end of the line and, $F_Σ$ and $F'_Σ$ are the total mechanical currents at either end of the line. Since the line is matched at both ends, the following condition is satisfied,

$$Z_{m0} = \frac{U_0}{F_Σ} = \frac{U_{N-1}}{F'_Σ} \quad (3.8)$$

The mechanical current $F_n$ is divided equally in both directions when it is injected into the line. From (3.7), the expressions for the mechanical voltages and currents at either end of the line at some test frequency can be written as shown in (3.9) and (3.10). It can be seen here how (3.3) with its resulting condition of current dividing equally between all transducers, was instrumental in simplifying the expressions.

$$U_0 = \left( -T_D V + T_B \frac{I}{N} \right)$$

$$F_Σ = \sum_{n=0}^{N-1} \frac{F_n}{2} e^{j\beta nd}$$

$$= \left( T_C V - T_A \frac{I}{N} \right) \frac{\Sigma}{2} \quad (3.9)$$

$$U_{N-1} = \left( -T_D V + T_B \frac{I}{N} \right) e^{-j\beta(N-1)d} \begin{cases} U_{N-1} = U_0 e^{-j\beta(N-1)d} \\ F'_Σ = F_Σ e^{-j\beta(N-1)d} \end{cases}$$

$$F'_Σ = \sum_{n=0}^{N-1} \frac{F_n}{2} e^{-j\beta(N-1)d} \quad (3.10)$$
The parameter $\Sigma$ in (3.9) is defined in (3.11), along with its various possible first-order linear approximations as $\theta \to 0$. These approximate expressions will be helpful in later analysis.

$$
\Sigma = \sum_{n=0}^{N-1} e^{j(\beta - \beta_0)n d}
$$

$$
= \frac{e^{jN\theta}}{e^{j\theta}} \frac{\sin(N\theta)}{\sin(\theta)} ; \quad \theta \triangleq (\beta - \beta_0) \frac{d}{2}
$$

$$
= N \text{sinc}(N\theta) e^{jN\theta}, \quad (\theta \text{ small})
$$

$$
= N (1 + jN\theta), \quad (N\theta \text{ small})
$$

$$
= N, \quad (\theta = 0)
$$

(3.11)

The equations in (3.9) and (3.10) can be rearranged to a matrix form as shown in (3.12) and (3.13). At $\beta = \beta_0$, these two matrix forms are identical except for a phase factor $e^{j\beta_0(N-1)d}$.

$$
\begin{bmatrix}
V \\
I
\end{bmatrix} =
\begin{bmatrix}
T_A & 2T_B/\Sigma \\
T_c N & 2T_d N/\Sigma
\end{bmatrix}
\begin{bmatrix}
U_0 \\
F_x
\end{bmatrix}
$$

(3.12)

$$
\begin{bmatrix}
V \\
I
\end{bmatrix} =
\begin{bmatrix}
(T_A) e^{j\beta_0(N-1)d} & (2T_B/\Sigma)e^{j\beta(N-1)d} \\
(T_c N) e^{j\beta_0(N-1)d} & (2T_d N/\Sigma)e^{j\beta(N-1)d}
\end{bmatrix}
\begin{bmatrix}
U_{N-1} \\
F_{x,}'
\end{bmatrix}
$$

(3.13)

In a practical implementation, in order to achieve practical impedance values, parallel arrays of transducers operating on parallel waveguides must be used. If there are $M$ identical parallel transducer arrays and waveguides, then the total electrical current fed to each array is simply $I/M$. Consequently, the matrix in (3.12) can be generalized to the form in (3.14):
\[
\begin{bmatrix}
V \\
I
\end{bmatrix}
= \begin{bmatrix}
T_A & 2T_B / \Sigma \\
T_NM & 2T_D / \Sigma
\end{bmatrix}
\begin{bmatrix}
U_0 \\
F_\Sigma
\end{bmatrix}
\] (3.14)

The matrix in (3.14) can be thought of as the generalized transducer transmission matrix for \( M \) parallel arrays of \( N \) transducers each, exciting waveguides that are terminated in a matched load at both ends. From this matrix and (3.8), a general expression for the electrical input impedance \( Z_{in} = \frac{V}{I} \) can be obtained as shown in (3.15):

\[
Z_{in} = \frac{1}{NM} \left( \frac{T_A Z_{m0} \Sigma + 2T_B}{T_C Z_{m0} \Sigma + 2T_D} \right)
\] (3.15)
3.2 Filter Design Equations

In this section, the general theory developed in Section 3.1 for an array of transducers satisfying (3.3) is applied to the capacitive transducer and the example waveguide structure described in Section 2.2. As derived in that section, the complete electromechanical model of the transducer consists of a cascade of the transducer transmission matrix and the mechanical transmission matrix. Thus, the generalized transmission matrix in (3.1) can be obtained as the product of (2.9) and (2.25) and is shown in (3.16). The corresponding equivalent circuit model of the capacitive transducer and the transducer-line coupling is shown in Figure 3.2.

\[
T = (T^E) \cdot T^{trans} \cdot T^M
\]

\[
= \begin{bmatrix}
 j \frac{B}{J} + \left(1 - a_{cm} \right) \frac{J}{JR_m} \\
 j \frac{B}{JR_m} & j \frac{B}{J}
\end{bmatrix}
\]  

(3.16)

Figure 3.2 Cascaded equivalent circuits of the capacitive transducer and the transducer-line coupling model.

In the above product of transmission matrices, the \textit{electrical transmission matrix} \( T^E \), representing the effect of electrical parasitic elements is also included for the sake of completeness. The exact expression for the electrical transmission matrix depends on
the specific design and layout of the filter. Here, it is assumed to be a 2x2 identity matrix.

The factor $a_{cm}$ defined in (3.17), represents the effect of the electrode reactance and is always a negative number. Another useful factor, $a_{rm}$, also defined in (3.17), represents the effect of the substrate leakage loss and will be used in later expressions. When the electrode does not exhibit any reactive effects and there is no substrate loss, $a_{cm} = a_{rm} = 0$.

$$a_{cm} = \frac{j^2}{(j\omega C_0)(j\omega C_m)}$$

$$a_{rm} = \frac{Z_{m0}}{2R_m}$$

From (3.16), the electrical input impedance in (3.15) and the corresponding admittance can be written as,

$$Z_{in}(\omega) = \frac{Z_{m0}}{2(1 + a_{rm}\Sigma)} \frac{J^2 \Sigma}{B^2NM} - \frac{j(1 - a_{cm})}{BNM}$$

$$Y_{in}(\omega) = \frac{1}{Z_{in}(\omega)} = \frac{Z_{m0}}{2(1 + a_{rm}\Sigma)} \frac{J^2\Sigma NM}{(1 - a_{cm})^2} + \frac{BNM}{(1 - a_{cm})}$$

The approximated expression for the input admittance is accurate only when the condition on $K^2$ defined in (3.19), is satisfied. For most practical structures, this condition is indeed satisfied, since the total susceptance of the capacitive transducer array dominates the effective input admittance of the array, similar to the one in (2.8).
\[ K^2 = \left( \frac{Z_{m0}}{2(1+a_m \Sigma)(1-a_{cm}^2) B} \right)^2 \ll 1 \quad (3.19) \]

After close inspection, the expressions in (3.18) can be rearranged to the form shown in (3.20) which lends itself to the conception of a possible circuit model for the input electrical impedance and admittance. The terms in (3.20) are defined in Table 3.1.

\[
\begin{align*}
Z_{in}^s(\omega) &= \frac{1}{G_{in,m}^s(\omega) + G_{in}^p(\omega) + jB_{in}^p(\omega)} - j \frac{1}{B_C} \\
Y_{in}^p(\omega) &= \frac{1}{R_{in,m}^p(\omega) + R_{in}^p(\omega) + jX_{in}^p(\omega)} + jB_C
\end{align*}
\quad (3.20)
\]

<table>
<thead>
<tr>
<th>Series model</th>
<th>Parallel model</th>
</tr>
</thead>
<tbody>
<tr>
<td>( G_{in,m}^s(\omega) = \frac{a_{m N}}{R^s} )</td>
<td>( R_{in,m}^p(\omega) = R^p a_{m N} )</td>
</tr>
<tr>
<td>( G_{in}^s(\omega) = \frac{1}{R^s} \text{Re} \left( \frac{N}{\Sigma} \right) )</td>
<td>( R_{in}^p(\omega) = R^p \text{Re} \left( \frac{N}{\Sigma} \right) )</td>
</tr>
<tr>
<td>( B_{in}^s(\omega) = \frac{1}{R^s} \text{Im} \left( \frac{N}{\Sigma} \right) )</td>
<td>( X_{in}^p(\omega) = R^p \text{Im} \left( \frac{N}{\Sigma} \right) )</td>
</tr>
<tr>
<td>( R^s = \frac{Z_{m0} J^2}{2 B^2 M} )</td>
<td>( R^p = \frac{2(1-a_{cm}^2)}{Z_{m0} J^2 N^2 M} )</td>
</tr>
<tr>
<td>( B_C = \frac{B M}{(1-a_{cm})} )</td>
<td>( B_C = \frac{B M}{(1-a_{cm})} )</td>
</tr>
</tbody>
</table>

Table 3.1 Expressions for the terms appearing in (3.20).

In the filter, there are two identical mirrored arrays, one at the input port and the other at the output port. When the conditions outlined in Section 3.1 are satisfied, the filter input impedance or admittance seen from the input port and the filter output impedance or admittance seen from output port is the same. The equivalent filter circuit model for this
situation developed based on the expressions in (3.20), as seen from both the input port and the output port, is shown in Figure 3.3 and Figure 3.4. The circuit model in Figure 3.3 can be thought of as the *series model* because the total DC capacitance of the transducers, \( C_{dc,NM/(1 - a_{cm})} \), appears in series with the rest of the circuit at the input port. Similarly, the circuit model in Figure 3.4 can be thought of as the *parallel model* because the total DC capacitance of the transducers appears in parallel with the rest of the circuit at the input port. The simplest matching network consists of a single inductor \( L_{mat} \), as shown in red on the left side of the vertical dashed line in the circuit diagrams. The inductor is designed to cancel out the total DC capacitance at some frequency which is typically the mean frequency of the entire operation band of the tunable filter. If it is feasible, a switchable bank of inductors can be used instead of one fixed inductor for better matching across the operation band. The input ports are fed by the filter input signal source \( V_{in} \), having an internal source impedance \( Z_0 \). Load impedance \( Z_L \) is connected at the output ports, the voltage across which constitutes the output signal of the filter.
Figure 3.3 The series circuit model for the electrical impedance of the filter seen from the input port and the output port when both the ports are matched and the mechanical transmission line is matched at both ends. The matching inductor, source impedance and the load impedance are also shown.

Figure 3.4 The parallel circuit model for the electrical admittance of the filter seen from the input port and the output port when both the ports are matched and the mechanical transmission line is matched at both ends. The matching inductor, source impedance and the load impedance are also shown.
If the ports are designed to be matched at the center frequency $\omega_0$, the matching conditions can be written as,

$$\begin{aligned}
Z_0 + j\omega_0 L_{\text{mat}} &= Z_{in}^*(\omega_0) = Z_L + j\omega_0 L_{\text{mat}} \quad \text{(series)} \\
\frac{1}{Z_0} + \frac{1}{j\omega_0 L_{\text{mat}}} &= Y_{in}^*(\omega_0) = \frac{1}{Z_L} + \frac{1}{j\omega_0 L_{\text{mat}}} \quad \text{(parallel)}
\end{aligned}$$

(3.21)

Firstly, (3.21) dictates that $Z_L = Z_0$. In most practical systems, the source impedance is purely real. Furthermore, from Table 3.1 and (3.11), it is evident that $B_{in}^*(\omega_0) = X_{in}^*(\omega_0) = 0$. Hence (3.21) can be simplified as follows:

$$\begin{aligned}
\text{Re}\left[Z_{in}(\omega_0)\right] &= Z_0 \quad \text{(series)} \\
\text{Re}\left[Y_{in}^*(\omega_0)\right] &= \frac{1}{Z_0} \quad \text{(parallel)} \\
\omega_0 L_{\text{mat}} &= 1/B_C
\end{aligned}$$

(3.22)

The expressions for the real part of the input impedance and admittance at the center frequency, obtained from (3.18) or (3.20) and Section 2.1, are shown in (3.23) and (3.24). When designing the filter, the various design parameters appearing in the boxed expressions of these two equations are tweaked so as to satisfy (3.22). Depending on how the matching inductor is connected at the ports, either the series model or the parallel model is used.
From the above equations, it can be seen that in the absence of substrate loss, the real part of the input impedance obtained from the series model is independent of $N$ at the center frequency, while the real part of the input admittance obtained from the parallel model is directly proportional to $N^2$ at the center frequency. This fact can also be easily derived from the simplified models of (2.11) and (2.9) and neglecting the transducer-line coupling. After neglecting the large negative series capacitor, the input impedance and admittance at the center frequency for an array with $M = 1$ can be obtained from (3.15) and (3.20), as shown in (3.25).

\[
\begin{align*}
\text{Re}[Z_{in}(\omega_0)] &= \frac{1}{G^{s}_{in}(\omega_0) + G^{s}_{in,m}(\omega_0)} \\
&= \frac{R^s}{(1 + a_{am}N)} \\
&= \frac{Z_{m0}}{2(1 + a_{am}N)M} \left( \frac{V_{dc}}{\omega_0 x_0} \right)^2
\end{align*}
\]

\[
\begin{align*}
\text{Re}[Y_{in}(\omega_0)] &= \frac{1}{R^{p}_{in}(\omega_0) + R^{p}_{in,m}(\omega_0)} \\
&= R^p \left( 1 + a_{am}N \right) \\
&= \frac{2(1 + a_{am}N)}{Z_{m0}M} \left( x_0^2 \left( 1 - a_{cm} \right) \right)^2
\end{align*}
\]

\[
\begin{align*}
Z_{in}(\omega_0) + j/B_c &= \frac{1}{G^{s}_{in}(\omega_0)} = \left( \frac{E_{dc}^2}{2\omega_0^2} \right) Z_{m0} \quad \text{(series)} \\
Y_{in}(\omega_0) - jB_c &= \frac{1}{R^{p}_{in}(\omega_0)} = \left( \frac{J^2}{2} \right) Z_{m0}N^2 \quad \text{(parallel)}
\end{align*}
\]
The value of the matching inductor at the center frequency can be calculated from the design parameters as,

\[
L_{\text{mat}} = \frac{(1 - a_{cm})}{\omega_0 B NM} \left[ \frac{x_0 (1 - a_{cm})}{\varepsilon_0 A_0 A_{\text{rc}}^2 \omega_0^2 N M} \right]
\]  

(3.26)

This matching scheme clearly comes with its own bandwidth limitation. The matching bandwidth is inversely proportional to the loaded quality factor of the tank circuit \(Q_{\text{mat}}\) under the assumption that input impedance/admittance satisfy (3.21) within the matching bandwidth, and can be written as (3.27). \(Q_{\text{mat}}\) corresponds to the overall filter Q if the bandwidth was limited by the matching rather than the filter itself, and its inverse represents the fractional bandwidth in which the real filter can be tuned without changing the matching inductance. It is, hence, desirable to minimize \(Q_{\text{mat}}\) by tweaking the parameters in the boxed expression of (3.27).

\[
Q_{\text{mat}}(\omega_0) = \frac{\left| \text{Im} \left[ Z_{\text{in}}(\omega_0) \right] \right|}{2 \text{Re} \left[ Z_{\text{in}}(\omega_0) \right]} = \frac{\left| \text{Im} \left[ Y_{\text{in}}(\omega_0) \right] \right|}{2 \text{Re} \left[ Y_{\text{in}}(\omega_0) \right]}
\]

\[
= \frac{(1 + a_{rm} N) B (1 - a_{cm})}{Z_{m0} J^2 N} = \frac{(1 + a_{rm} N) A_0 x_0^3 (1 - a_{cm})}{Z_{m0} \varepsilon_0 A_{\text{rc}} V_{\text{dc}}^2 N}
\]  

(3.27)
From Figure 3.3 or Figure 3.4 and (3.20), it is seen that the conductance \( G'_{\text{in}}(\omega_0) = j/\omega_0 \) and the resistance \( R_{\text{in}}(\omega_0) = R_p \) represent the characteristic resistance or conductance of the waveguide at the center frequency, while the conductance \( G'_{\text{in,m}} \) and the resistance \( R_{\text{in,m}} \) represent the loss into the substrate. Hence, the fraction of the power flowing into the waveguide, \( p_{\text{wg}} \), can be obtained at the center frequency as shown in (3.28). For an ideal design with no substrate loss, \( p_{\text{wg}}(\omega_0) = 1 \).

\[
p_{\text{wg}}(\omega_0) = \begin{cases} \frac{|V|^2 G'_{\text{in}}(\omega_0)}{|V|^2 \left( G'_{\text{in}}(\omega_0) + G'_{\text{in,m}}(\omega_0) \right)} \\ \frac{|I|^2 R_{\text{in}}(\omega_0)}{|I|^2 \left( R_{\text{in}}(\omega_0) + R_{\text{in,m}}(\omega_0) \right)} \end{cases}
\]

\[
= \frac{1}{1 + a_{\text{in}} N} \tag{3.28}
\]

The total insertion loss of the filter in dB, \( IL \), at the center frequency can be obtained from (3.28) as shown in (3.29). This expression is valid subject to the conditions of the derivation in Section 3.1 where it is assumed that the waveguide is terminated in a matched load at both ends. For such a waveguide, half the input power is lost at the input port and half of the remaining half is lost at the output port, causing an additional 6 dB loss as shown in (3.29).

\[
IL(\omega_0) = 10 \log_{10} \left( \frac{1}{1 + a_{\text{in}} N} \right)^2 - 6 \quad \text{(dB)} \tag{3.29}
\]
A derivation of the Q-factor of the filter response, $Q_{\text{filter}}$, at the center frequency, is presented next. A simple expression will be derived in the absence of substrate loss and then it will be used to estimate a possible formula for the Q-factor in the presence of substrate loss. Since the FIR response is characterized by transmission zeros in the rejection band, let us define the filter bandwidth as the interval confined between the close in transmission zeros in the lower and upper rejection bands. In the absence of substrate loss ($a_{rm} = 0$), the filter bandwidth and the Q-factor can be obtained by finding the frequency at which the frequency dependent load resistance presented by the waveguide drops to zero. This derivation is shown in (3.30), where the definition for $\theta$ given in (3.11) and the condition $\beta_0 = \pi/d$ from (3.3), is used to simplify the expression.

\[
\begin{align*}
G_m^\prime(\omega) = 0 \\
R_m^\prime(\omega) = 0
\end{align*}
\Rightarrow \text{Re}\left[\frac{N}{\Sigma}\right] = N\theta \cot(N\theta) = 0
\Rightarrow \theta = \frac{\pi}{2N}
\Rightarrow Q_{\text{filter}}(\omega_0) = \frac{\beta_0}{2(\beta - \beta_0)} = \frac{N}{2}
\] (3.30)

The Q-factor at resonance is typically defined as the ratio of the imaginary part of the impedance or admittance to the real part of the impedance or admittance. With this definition in mind, a potential hidden susceptance $B_m^\prime$ and a reactance $X_m^\prime$ are defined at the center frequency using (3.30), as shown in (3.31). $B_m^\prime$ appears in parallel with $G_m^\prime$, while $X_m^\prime$ appears in series with $R_m^\prime$. It is assumed that these arbitrary components get cancelled out at resonance to give a net zero susceptance or reactance, as discussed earlier. They are also assumed to be independent of the substrate loss.
\[
B_i^\prime(\omega_0) = \frac{N}{2} \left( G_{in}^\prime(\omega_0) + 1/Z_0 \right) \\
= NG_{in}^\prime(\omega_0)
\]
\[
X_{in}^{p'}(\omega_0) = \frac{N}{2} \left( R_{in}^p(\omega_0) + Z_0 \right) \\
= NR_{in}^p(\omega_0)
\]

(3.31)

With this formulation, the loaded Q-factor of the filter response at the center frequency in the presence of substrate loss \((a_{rm} \neq 0)\) can be expressed as,

\[
Q_{\text{filter}}(\omega_0) = \begin{cases} 
\frac{B_i^\prime(\omega_0)}{2\left( G_{in}^\prime(\omega_0) + G_{in,m}^\prime(\omega_0) \right)} \\
\frac{X_{in}^{p'}(\omega_0)}{2\left( R_{in}^p(\omega_0) + R_{in,m}^p(\omega_0) \right)}
\end{cases}
\]

(3.32)

This is clearly less than the Q-factor of \(N/2\) in (3.30). As can be expected, due to the presence of resistive substrate losses, the filter response is not as sharp. In a filter with no substrate loss, the filter response can be made arbitrarily narrow by increasing \(N\). For a filter with substrate loss, there is a limit on how narrow the filter response can be made. This limit, \(Q_{\text{loss}}\), expressed in (3.33), dictates that the Q-factor of the filter cannot exceed \(1/(2a_{rm})\).

\[
Q_{\text{loss}} = \lim_{N \to \infty} \left[ Q_{\text{filter}}(\omega_0) \right] = \frac{1}{2a_{rm}}
\]

(3.33)
It can be seen that the equations for the input impedance and input admittance of an array, as well as the matching Q-factor, are in agreement with the results obtained in [37]. Finally, it should be emphasized that although the equations derived in this section are only valid when (3.3) is satisfied, these equations serve as helpful guidelines during the overall filter design process to examine performance trade-offs.
Chapter 4

CIRCUIT SIMULATOR

A circuit simulator developed to analyze the filter is described in this chapter. This simulator is a computer program which is written in a modular fashion using several functions. In general, if the mechanical circuit models are known, the program can be quite versatile. It can simulate a wide variety of filter structures, including structures that use transducers with arbitrary transmission matrices, complex waveguide structures that are periodically loaded or designs that exploit multiple modes of a multi-moded waveguide.

Figure 4.1 shows the complete schematic block diagram of the filter circuit that the simulator solves for. Except for the transducers, each circuit block is represented by its impedance matrix \( Z \), followed by a subscript, that is contained within the block. In some cases, the T-matrix \( T \) (described later) representing the block is also shown. The impedance matrix of the entire filter is denoted by \( Z_{FIL} \). There are two arrays of \( N \) transducers each, one on the input side and one on the output side, denoted by the impedance matrices \( Z_{CAS} \) and \( Z'_{CAS} \), respectively. The transducer arrays are simulated as a cascade of \( N \) unit cells with their electrical ports connected together. As explained later, the input impedance of one transducer array, \( Z_{in} \), independent of the rest of the filter circuit, can also be computed to help in analyzing the design. The structure connecting the input and output array is simulated by the connecting impedance matrix \( Z_{CON} \). Structures in which the arrays are terminated are simulated by the terminal impedance matrixes \( Z_{TER} \) and \( Z'_{TER} \). Each unit cell in the transducer array is denoted by the impedance matrix \( Z''_U \). It is simulated as a combination of a constant mechanical
part denoted by the $Z_{FL}$ and the transducer with the generalized transmission matrix $T_{ABCD}$

Adjacent transducers are separated by the pitch distance $d$. It should be noted that the schematic in Figure 4.1 is drawn only for one waveguide. In general, there can be $M$ such waveguides excited electrically parallel to each other. In such a situation, the total impedance matrix of the filter and the total input impedance of one transducer array, are simply obtained by dividing $Z_{FL}$ and $Z_{in}$, by $M$, respectively.
Figure 4.1 Schematic block diagram of the general filter circuit that is solved by the circuit simulator. (Note: figure rotated anti-clockwise by 90 degrees)

Next, the general equations outlining the simulation steps to solve the circuit of Figure 4.1 are presented. All the functions that appear here, denoted by the script $\mathfrak{F}$ followed
by a subscript, are defined in Section 4.3. The impedance matrices $Z_U^n$, are computed as,

$$Z_U^n = S_{ABCD} Z_{TL} \left( T_{ABC}^n \right)$$  \hspace{1cm} (4.1)

These are cascaded to obtain $Z_{CAS}$ as shown in (4.2). Typically, the excitation of the output transducer array is a mirror image of the excitation of the input transducer array. Hence, $Z_{CAS}'$ can also be computed from $Z_U^n$, as shown in (4.2).

$$Z_{CAS} = S_{ZaZb} \left( \ldots S_{ZaZb} \left( S_{ZaZb} \left( Z_U^n , Z_U^2 \right), Z_U^1 \right) , \ldots , Z_U^N \right)$$

$$Z_{CAS}' = S_{ZaZb} \left( \ldots S_{ZaZb} \left( S_{ZaZb} \left( Z_U^N , Z_U^{N-1} \right), Z_U^{N-2} \right) , \ldots , Z_U^1 \right)$$  \hspace{1cm} (4.2)

Finally, $Z_{FIL}$, is computed as shown in (4.3). This impedance matrix can be converted to the corresponding S-parameter matrix $S_{FIL}$, for the given $Z_0$. The filter response in dB can then be computed as, $20 \log_{10} \left( \left| S_{FIL,21} \right| \right)$.

$$Z_{FIL} = S_{filter} \left( Z_{CAS}, Z_{CAS}' , Z_{CON} , Z_{TER} , Z_{TER}' \right)$$  \hspace{1cm} (4.3)

*Image* impedances of a 2-port network are defined as the load impedances for which both the ports are simultaneously matched. For a symmetric 2-port, the image impedances at both ports are equal. Typically, $Z_{FIL}$ is a symmetric matrix and the image impedance is computed as shown in (4.4). The conjugate of the image impedance, $Z_i^*$, gives an idea of the port impedances looking into the ports, and therefore, the values of
the system and load impedances, and matching inductors, that would result in perfect impedance matching. If the filter is properly designed, then $\text{Re}[Z_i(\omega_i)] = Z_0$. From (4.4), the image admittance can also be calculated as, $Y_i = 1/Z_i$.

$$Z_i = \Imag(Z_{\text{FIL}})$$

(4.4)

### 4.1 Example Case

In Figure 4.1, the internal structures of some of the blocks are also shown. These structures correspond to a simple filter design consisting of an acoustic waveguide operated in the single moded bandwidth. This example design is considered to illustrate the computation of some of the blocks in the circuit schematic. The waveguide mode is simulated as a transmission line of characteristic impedance $Z_{m0}$, and a propagation constant $\beta$. Each unit cell thus features a T-junction, as shown in Figure 4.1, made of two transmission lines of length $d/2$, connected to a transducer. Consequently, $Z_{TL}$, is computed as shown in (4.5) and the generalized transducer transmission matrix $T_{ABCD}^n$ is computed from (3.16) and (3.2).

$$Z_{TL} = -j \frac{Z_{m0}}{2} \begin{bmatrix} \cot \phi & \csc \phi & \csc \phi \\ \csc \phi & 2 \cot \phi & 2 \csc \phi 2 \phi \\ \csc \phi & 2 \csc \phi & 2 \cot \phi \end{bmatrix}, \quad \phi = \frac{\beta d}{2} \quad (4.5)$$

Once $Z_{CAS}$ is computed from (4.2), it is worthwhile to compare the simulation results with the expected theoretical model parameters obtained using the filter design equations of
Section 3.2. Accordingly, the input impedance of one transducer array, $Z_{in}$, independent of the rest of the filter circuit, is computed as shown in (4.6). Here, the array is simulated as terminated in the mechanical loads $Z_{ml,1}$ and $Z_{ml,2}$, at either end. For the equations of Section 3.2 to hold true, $Z_{ml,1} = Z_{ml,2} = Z_{m0}$.

$$Z_{in} = Z_{CAS,11} + Z_{CAS,12} \frac{x_1}{x_3} + Z_{CAS,13} \frac{x_2}{x_3}$$

where,

$$x_1 = Z_{CAS,31}Z_{CAS,23} - Z_{CAS,21}(Z_{CAS,33} + Z_{ml,2})$$

$$x_2 = Z_{CAS,21}Z_{CAS,32} - Z_{CAS,31}(Z_{CAS,22} + Z_{ml,1})$$

$$x_3 = (Z_{CAS,22} + Z_{ml,1})(Z_{CAS,33} + Z_{ml,2}) - Z_{CAS,23}Z_{CAS,32}$$

(4.6)

The connecting structure is just a transmission line section of length $d_c$, so $Z_{CON}$ is computed as,

$$Z_{CON} = -j \frac{Z_{m0}}{\sin \phi_c} \begin{bmatrix} \cos \phi_c & 1 \\ 1 & \cos \phi_c \end{bmatrix}, \quad \phi_c = \beta d_c$$

(4.7)

The transducer arrays are terminated at either end in a mechanical load $Z_{ml}$, connected at the end of a transmission line section of length $d_f$, as shown in Figure 4.1. Thus, the terminal impedance is computed as shown in (4.8). For the equations of Section 3.2 to hold true, $Z_{ml} = Z_{m0}$.

$$Z_{TER} = Z'_{TER} = Z_{TER} = Z_{m0} \frac{Z_{ml} + jZ_{m0} \tan \phi_f}{Z_{m0} + jZ_{ml} \tan \phi_f}, \quad \phi_f = \beta d_f$$

(4.8)
4.2 T-matrix Method

A **T-matrix** is defined for a multiport network with *odd* number of ports to speed the circuit simulation. This T-matrix should not be confused with the 2-port transmission matrices which are discussed in all the other chapters. Although, the motivation for the definition of the T-matrix comes from the way in which transmission matrixes are defined, relating the input ports to the output ports of a multiport network. In order to distinguish them from the T-matrix discussed here, the 2-port transmission matrices are denoted by $T_{ABCD}$ only in this chapter. In all the other chapters, the subscript ‘ABCD’ is dropped for the 2-port transmission matrices. If an $N$ port network has an impedance matrix $Z$, with port voltages $\overline{V}$ and currents $\overline{I}$, then $\overline{V} = Z \overline{I}$. The corresponding T-matrix $T$, for this network can be defined as shown in (4.9).

\[
\begin{bmatrix}
V_1 \\
T_{in}
\end{bmatrix} = T
\begin{bmatrix}
I_1 \\
T_{out}
\end{bmatrix}, \quad \text{where} \quad \begin{bmatrix}
\overline{T}_{in} \\
\overline{T}_{out}
\end{bmatrix} = \begin{bmatrix}
V_2 & I_2 & V_4 & I_4 & \ldots & V_{N-1} & I_{N-1}
\end{bmatrix}^T
\]

(4.9)

General equations to simulate the filter circuit using the T-matrices are discussed next. The T-matrices of the unit cells, $T_{U}^{n}$, are computed as,

\[
T_{U}^{n} = S_{Z2T} \left(Z_{U}^{n}\right)
\]

(4.10)

T-matrices of the input and output array of transducers, $T_{CAS}$ and $T_{CAS}'$, respectively, are computed as,
\[ T_{CAS} = \mathcal{S}_{TaTb} \left( \ldots \mathcal{S}_{TaTb} \left( \mathcal{S}_{TaTb} \left( T_U^1, T_U^2 \right), T_U^3 \right), \ldots , T_U^N \right) \]
\[ T'_{CAS} = \mathcal{S}_{TaTb} \left( \ldots \mathcal{S}_{TaTb} \left( \mathcal{S}_{TaTb} \left( T_U^N, T_U^{N-1} \right), T_U^{N-2} \right), \ldots , T_U^1 \right) \]  
(4.11)

The T-matrix of the connecting segment \( T_{CON} \), is computed from \( Z_{CON} \) after zero-padding as,
\[ T_{CON} = \mathcal{S}_{Z2T} \left( \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix}^T \begin{bmatrix} 0 & 0 \\ 0 & 0 \end{bmatrix} \right) \]  
(4.12)

Finally, the impedance matrix of the entire filter is computed as,
\[ Z_{FIL} = \mathcal{S}_{filter-T} \left( T_{CAS}, T'_{CAS}, T_{CON}, Z_{TER}, Z'_{TER} \right) \]  
(4.13)

The T-matrix method can provide slight improvement in the computational speed for certain designs.

4.3 Functions

To simplify the equations that appear in the description of the functions in the tables presented below, a special notation is used here to represent subsets of components of a vector or elements of a matrix. Instead of using an arrow on top or a bold letter to describe these subsets, an intuitive subscript notation is used, as shown in the example of (4.14). In this example, a subset of components of a vector \( \bar{A} \) and a subset of elements of a matrix \( B \) are denoted in the subscript notation using the indices \( m \) and \( n \) .
Also, in the diagrams that are shown in the description of each function, a special convention is followed to make them easier to read. Instead of showing every port of a multiport network, appropriate subsets of ports are grouped together and represented by a single bold arrow, as shown in Figure 4.2. In this example, ports with numbers denoted by the index $n$ are grouped together in the modified diagram.

\[
\begin{align*}
A_n &= \begin{bmatrix} A_1 & A_3 & A_7 \end{bmatrix}^T \\
\Rightarrow B_{mn} &= \begin{bmatrix} B_{21} & B_{23} & B_{27} \\
B_{41} & B_{43} & B_{47} \end{bmatrix}
\end{align*}
\] (4.14)

Figure 4.2 Illustration of the convention used in the diagrams to represent subsets of ports using a bold arrow.

The reader should also be reminded that the 2-port transmission matrices in this Appendix are denoted with the subscript ‘ABCD’ as $T_{ABCD}$. 
**Function:**

\[ Z' = \mathcal{S}_{ABCD}(Z, T_{ABCD}) \]

**Diagram:**

\[
\begin{array}{ccc}
V'_1 & \rightarrow & T_{ABCD} \\
\downarrow & & \downarrow \\
\rightarrow & & \rightarrow \\
V_1 & \rightarrow & Z
\end{array}
\]

\[ I_1 \rightarrow I_n \rightarrow V_n \]

**Indices:**

\[ n = 2, 3, \ldots, N \]

**Given:**

\[
\begin{bmatrix} V_1 \\ V_n \end{bmatrix} = \begin{bmatrix} Z_{i_1} & Z_{i_n} \\ Z_{n_1} & Z_{nn} \end{bmatrix} \begin{bmatrix} I_1 \\ I_n \end{bmatrix}
\]

\[
\begin{bmatrix} V'_1 \\ I'_1 \end{bmatrix} = \begin{bmatrix} T_A & T_B \\ T_C & T_D \end{bmatrix} \begin{bmatrix} V_1 \\ I_1 \end{bmatrix}
\]

**Find:**

\[
\begin{bmatrix} V'_1 \\ V_n \end{bmatrix} = \begin{bmatrix} Z'_{i_1} & Z'_{i_n} \\ Z'_{n_1} & Z'_{nn} \end{bmatrix} \begin{bmatrix} I'_1 \\ I_n \end{bmatrix}
\]

**Solution:**

\[
\begin{bmatrix} Z'_{i_1} \\ Z'_{n_1} \\ Z'_{i_n} \\ Z'_{nn} \end{bmatrix} = \frac{1}{x} \begin{bmatrix} (T_A Z_{i_1} + T_B) & Z_{i_1} (T_AT_D - T_BT_C) \\ Z_{n_1} & Z_{nn} - Z_{i_1} Z_{i_n} T_C \end{bmatrix}
\]

where, \( x = T_C Z_{i_1} + T_D \)

**Comments:**

Table 4.1 Circuit simulator function.

---

**Function:**

\[ \begin{bmatrix} Z_{i_1} & Z_{i_2} \end{bmatrix} = \mathcal{S}_{image}(Z) \]

**Diagram:**

\[
\begin{array}{ccc}
Z_{i_1} & \rightarrow & Z \\
\downarrow & & \downarrow \\
\rightarrow & & \rightarrow \\
Z_{i_2} & \rightarrow & Z_{i_2}
\end{array}
\]

\[ \text{positive roots of} \]

\[ \text{Re} \left[ T_D T_C^* \right] Z_{i_1}^2 + j \text{Im} \left[ T_B T_C^* + T_A T_D^* \right] Z_{i_1} - \text{Re} \left[ T_A T_B^* \right] = 0 \]

\[ \text{Solution:} \]

\[ \text{Re} \left[ T_A T_C^* \right] Z_{i_2}^2 + j \text{Im} \left[ T_B T_C^* + T_D T_A^* \right] Z_{i_2} - \text{Re} \left[ T_D T_B^* \right] = 0 \]

where, \( \begin{bmatrix} T_A & T_B \\ T_C & T_D \end{bmatrix} = \frac{1}{Z_{21}} \begin{bmatrix} Z_{i_1} & Z_{i_1} Z_{22} - Z_{i_2} Z_{21} \\ 1 & Z_{22} \end{bmatrix} \)

**Comments:**

symmetric \( Z \Rightarrow T_A = T_D \Rightarrow Z_{i_1} = Z_{i_2} = Z_i \)

Table 4.2 Circuit simulator function.
**Function:** \( Z = 3_{ZaZb} (Za, Zb) \)

**Diagram:**

![Diagram](image)

**Indices:**

- \( e = 2, 4, \ldots, N-1 \)
- \( o = 3, 5, \ldots, N \)
- \( p = 1, 2, \ldots, \frac{N-1}{2} \)

**Given:**

\[
\begin{align*}
V_1 & = \begin{bmatrix} Z_{a11} & Z_{a1e} & Z_{a1o} \\ Z_{a1e} & Z_{aee} & Z_{aeo} \\ Z_{a1o} & Z_{aoe} & Z_{aoa} \end{bmatrix}\begin{bmatrix} I_{a1} \\ I_{ae} \\ I_{ao} \end{bmatrix} \\
V_e & = \begin{bmatrix} Z_{be1} & Z_{bee} & Z_{beo} \\ Z_{bee} & Z_{beeo} & Z_{beoo} \\ Z_{beo} & Z_{beoe} & Z_{beoo} \end{bmatrix}\begin{bmatrix} I_{be1} \\ I_{beee} \\ I_{beeo} \end{bmatrix} \\
V_0 & = \begin{bmatrix} Z_{b11} & Z_{b1e} & Z_{b1o} \\ Z_{b1e} & Z_{bbe} & Z_{bbo} \\ Z_{b1o} & Z_{bboe} & Z_{bboo} \end{bmatrix}\begin{bmatrix} I_{b1} \\ I_{b1e} \\ I_{b1o} \end{bmatrix} \\
V_{e_1} & = \begin{bmatrix} Z_{ae1} & Z_{aeo} \\ Z_{aeo} & Z_{aoe} \end{bmatrix}\begin{bmatrix} I_{a1} \\ I_{ao} \end{bmatrix} \\
V_{e_2} & = \begin{bmatrix} Z_{ae2} & Z_{aeo} \\ Z_{aeo} & Z_{aoe} \end{bmatrix}\begin{bmatrix} I_{a1} \\ I_{ao} \end{bmatrix} \\
V_{e_3} & = \begin{bmatrix} Z_{ae3} & Z_{aeo} \\ Z_{aeo} & Z_{aoe} \end{bmatrix}\begin{bmatrix} I_{a1} \\ I_{ao} \end{bmatrix}
\end{align*}
\]

**Find:**

\[
\begin{align*}
V_1 & = \begin{bmatrix} Z_{i11} & Z_{i1e} & Z_{i1o} \\ Z_{i1e} & Z_{iee} & Z_{ieo} \\ Z_{i1o} & Z_{ioe} & Z_{ioo} \end{bmatrix}\begin{bmatrix} I_{i1} \\ I_{ie} \\ I_{io} \end{bmatrix} \\
V_e & = \begin{bmatrix} Z_{ie1} & Z_{ieo} \\ Z_{ieo} & Z_{ioe} \end{bmatrix}\begin{bmatrix} I_{i1} \\ I_{io} \end{bmatrix} \\
V_0 & = \begin{bmatrix} Z_{i01} & Z_{i0e} & Z_{i0o} \\ Z_{i0e} & Z_{i0ee} & Z_{i0eo} \\ Z_{i0o} & Z_{i0oe} & Z_{i0oo} \end{bmatrix}\begin{bmatrix} I_{i0} \\ I_{i0e} \\ I_{i0o} \end{bmatrix} \\
V_{e_1} & = \begin{bmatrix} Z_{ie1} & Z_{ieo} \\ Z_{ieo} & Z_{ioe} \end{bmatrix}\begin{bmatrix} I_{i1} \\ I_{io} \end{bmatrix} \\
V_{e_2} & = \begin{bmatrix} Z_{ie1} & Z_{ieo} \\ Z_{ieo} & Z_{ioe} \end{bmatrix}\begin{bmatrix} I_{i1} \\ I_{io} \end{bmatrix} \\
V_{e_3} & = \begin{bmatrix} Z_{ie1} & Z_{ieo} \\ Z_{ieo} & Z_{ioe} \end{bmatrix}\begin{bmatrix} I_{i1} \\ I_{io} \end{bmatrix}
\end{align*}
\]

**Solution:**

\[
\begin{align*}
\begin{bmatrix} Z_{a11} & Z_{a1e} & Z_{a1o} \\ Z_{a1e} & Z_{aee} & Z_{aeo} \\ Z_{a1o} & Z_{aoe} & Z_{aoa} \end{bmatrix} & = \begin{bmatrix} 0 & Z_{a1e} & 0 \\ 0 & Z_{aee} & 0 \\ Z_{a1o} & Z_{aoe} & 0 \end{bmatrix} \\
\begin{bmatrix} Z_{b11} & Z_{b1e} & Z_{b1o} \\ Z_{b1e} & Z_{bbe} & Z_{bbo} \\ Z_{b1o} & Z_{bboe} & Z_{bboo} \end{bmatrix} & = \begin{bmatrix} 0 & Z_{b1e} & 0 \\ 0 & Z_{bbe} & 0 \\ Z_{b1o} & Z_{bboe} & 0 \end{bmatrix}
\end{align*}
\]

\[
\begin{align*}
\begin{bmatrix} Z_{a11} & Z_{a1o} \\ Z_{a1e} & Z_{aeo} \\ -Z_{b1o} & -Z_{b1e} \end{bmatrix} & \left( \begin{bmatrix} Z_{a11} + Z_{b11} \\ Z_{a1o} + Z_{b1o} \\ Z_{a1e} + Z_{b1e} \end{bmatrix} \right)^{-1} \begin{bmatrix} Z_{b11} & -Z_{a1e} & Z_{b1o} \\ Z_{b1e} & -Z_{aeo} & Z_{bbo} \\ Z_{b1o} & Z_{bbo} & Z_{bboo} \end{bmatrix}
\end{align*}
\]

where, \( \mathbf{0} \) = zero matrix

**Table 4.3 Circuit simulator function.**
**Function:** \[ Z = \mathcal{F} \left( Z_a, Z_b, Z_c, Z_1^{11}, Z_1^{12} \right) \]

**Diagram:**

![Diagam Image]

**Indices:**

\[ e = 2, 4, \ldots, N - 1 \]
\[ o = 3, 5, \ldots, N \]
\[ o' = o - 2 \]
\[ p = 1, 2, \ldots, \frac{N-1}{2} \]

**Given:**

\[
\begin{align*}
V_{a_e} &= \begin{bmatrix} Z_{a_{11}} & Z_{a_{1e}} & Z_{a_{1o}} \\ Z_{a_{e1}} & Z_{a_{ee}} & Z_{a_{eo}} \\ Z_{a_{o1}} & Z_{a_{oe}} & Z_{a_{oo}} \end{bmatrix} I_1 \\
V_{a_o} &= \begin{bmatrix} Z_{a_{1o}} & I_{a_e} \\ Z_{a_{eo}} & I_{a_o} \\ Z_{a_{oo}} & I_{a_o} \end{bmatrix} I_2 \\
V_{b_e} &= \begin{bmatrix} Z_{b_{11}} & Z_{b_{1e}} & Z_{b_{1o}} \\ Z_{b_{e1}} & Z_{b_{ee}} & Z_{b_{eo}} \\ Z_{b_{o1}} & Z_{b_{oe}} & Z_{b_{oo}} \end{bmatrix} I_2 \\
V_{b_o} &= \begin{bmatrix} Z_{b_{1o}} & I_{b_e} \\ Z_{b_{eo}} & I_{b_o} \\ Z_{b_{oo}} & I_{b_o} \end{bmatrix} I_2
\end{align*}
\]

**Find:**

\[
\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} Z_{11} & Z_{12} \\ Z_{21} & Z_{22} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix}
\]

**Solution:**

\[
Z_{11} = Z_{a_{11}} + Z_{a_{1e}} \left( X_{11}Z_{a_{e1}} + X_{12}Z_{a_{o1}} \right) + Z_{a_{1o}} \left( X_{21}Z_{a_{e1}} + X_{22}Z_{a_{o1}} \right)
\]

\[
Z_{12} = Z_{a_{e1}} \left( X_{13}Z_{b_{o1}} + X_{14}Z_{b_{e1}} \right) + Z_{a_{eo}} \left( X_{23}Z_{b_{o1}} + X_{24}Z_{b_{e1}} \right)
\]

\[
Z_{21} = Z_{b_{e1}} \left( X_{31}Z_{a_{e1}} + X_{32}Z_{a_{o1}} \right) + Z_{b_{eo}} \left( X_{41}Z_{a_{e1}} + X_{42}Z_{a_{o1}} \right)
\]

\[
Z_{22} = Z_{b_{11}} + Z_{b_{1e}} \left( X_{33}Z_{b_{o1}} + X_{34}Z_{b_{e1}} \right) + Z_{b_{1o}} \left( X_{43}Z_{b_{o1}} + X_{44}Z_{b_{e1}} \right)
\]

where,

\[
\begin{bmatrix} X_{11} & X_{12} & X_{13} & X_{14} \\ X_{21} & X_{22} & X_{23} & X_{24} \\ X_{31} & X_{32} & X_{33} & X_{34} \\ X_{41} & X_{42} & X_{43} & X_{44} \end{bmatrix}
\]

\[
\begin{bmatrix} (Z_{a_{ee}} + Z_{11}) & Z_{a_{eo}} & 0 \pp & 0 \pp \\ Z_{a_{oe}} & (Z_{a_{oo}} + Z_{c_{o'o'}}) & Z_{c_{o'e}} & 0 \pp \\ 0 \pp & 0 \pp & (Z_{b_{oo}} + Z_{12}) & (Z_{b_{ee}} + Z_{c_{ee}}) \\ 0 \pp & Z_{c_{eo'}} & (Z_{b_{eo'}} + Z_{c_{eo}}) \end{bmatrix}^{-1}
\]

where, \( \mathbf{0} \) = zero matrix

---

*Table 4.4 Circuit simulator function.*
Table 4.5 Circuit simulator function.
Function: \( T = \sum_{i=1}^{n} \left( Ta_i \cdot Tb_i \right) \)

Diagram:

Indices: \( n = 2, 3, \ldots, N \)

Given:

\[
\begin{bmatrix}
V_1 \\
\overline{Ta_{in}}
\end{bmatrix} = \begin{bmatrix}
Ta_{i1} & Ta_{in} \\
Ta_{i1} & Ta_{in}
\end{bmatrix} \begin{bmatrix}
Ia_i \\
\overline{Ta_{in}}
\end{bmatrix}
\]

\[
\begin{bmatrix}
V_1 \\
\overline{Tb_{in}}
\end{bmatrix} = \begin{bmatrix}
Tb_{i1} & Tb_{in} \\
Tb_{i1} & Tb_{in}
\end{bmatrix} \begin{bmatrix}
I_1 - Ia_i \\
\overline{Tb_{in}}
\end{bmatrix}
\]

Find:

\[
\begin{bmatrix}
V_1 \\
\overline{Ta_{in}}
\end{bmatrix} = \begin{bmatrix}
T_{i1} & T_{in} \\
T_{i1} & T_{in}
\end{bmatrix} \begin{bmatrix}
I_1 \\
\overline{Tb_{out}}
\end{bmatrix}
\]

Solution:

\[
\begin{bmatrix}
T_{i1} & T_{in} \\
T_{i1} & T_{in}
\end{bmatrix} = \frac{(Ta_{i1} \cdot Tb_{i1})}{x} \begin{bmatrix}
(Ta_{i1} \cdot Tb_{in} + Tb_{i1} \cdot Ta_{in} \cdot Tb_{in} - Ta_{in} \cdot Tb_{in}) \\
Ta_{i1} \cdot (Ta_{in} \cdot Tb_{in} - Ta_{in})
\end{bmatrix}
\]

where, \( x = Ta_{i1} + Tb_{i1} - Ta_{in} \cdot Tb_{in} \)

Table 4.6 Circuit simulator function.
### Function:

\[ Z = \frac{3}{\text{filter-T}} \left( T_a, T_b, T_c, Z_{11}, Z_{12} \right) \]

### Diagram:

same as in Section Error! Reference source not found.

### Indices:

- \( e = 2, 4, \ldots, N - 1 \)
- \( o = 3, 5, \ldots, N \)
- \( m = e, o \)
- \( p = 1, 2, \ldots, \frac{N-1}{2} \)

### Given:

\[
\begin{bmatrix}
V_a_e \\
I_a_e
\end{bmatrix}
= \begin{bmatrix}
T_{a_1} & T_{a_m} \\
T_{a_m} & T_{a_{mm}}
\end{bmatrix}
\begin{bmatrix}
I_1 \\
V_a_o \\
-\text{I}_a_o
\end{bmatrix}
\]

\[
\begin{bmatrix}
V_b_e \\
I_b_e
\end{bmatrix}
= \begin{bmatrix}
T_{b_1} & T_{b_m} \\
T_{b_m} & T_{b_{mm}}
\end{bmatrix}
\begin{bmatrix}
I_1 \\
V_b_o \\
-\text{I}_b_o
\end{bmatrix}
\]

\[
\begin{bmatrix}
0 \\
V_a_o \\
-\text{I}_a_o
\end{bmatrix}
= \begin{bmatrix}
0 & 0 \\
0 & T_{c_{mm}}
\end{bmatrix}
\begin{bmatrix}
0 \\
V_b_e \\
I_b_e
\end{bmatrix}
\]

where, \( \mathbf{0} = \) zero matrix

\[V_a_e = -Z_{pp}^1 I_a_e \]

\[V_b_o = -Z_{pp}^2 I_b_o \]

### Find:

\[\begin{bmatrix}
V_1 \\
V_2
\end{bmatrix}
= \begin{bmatrix}
Z_{11} & Z_{12} \\
Z_{21} & Z_{22}
\end{bmatrix}
\begin{bmatrix}
I_1 \\
I_2
\end{bmatrix}\]

### Solution:

\[
Z_{11} = T_{a_1} - T_{a_m} T_{c_{mm}} T_{b_{mm}} X T_{a_{m1}}
\]

\[
Z_{12} = T_{a_m} T_{c_{mm}} T_{b_{m1}} - T_{a_m} T_{c_{mm}} T_{b_{mm}} X T_{a_{m1}} T_{c_{mm}} T_{b_{m1}}
\]

\[
Z_{21} = -T_{b_m} X T_{a_{m1}}
\]

\[
Z_{22} = T_{b_1} - T_{b_m} X T_{a_{m1}} T_{c_{mm}} T_{b_{m1}}
\]

where, \( X = \)

\[
\begin{bmatrix}
Z_{pp}^2 & Z_{pp}^1 \\
1 & 1
\end{bmatrix}
\begin{bmatrix}
1 & T_{a_{mm}} T_{b_{mm}} T_{c_{mm}} \\
1 & 1
\end{bmatrix}
\]

\[
\begin{bmatrix}
Z_{pp}^2 & Z_{pp}^1 \\
1 & 1
\end{bmatrix}
\]

Table 4.7 Circuit simulator function.
Chapter 5

DESIGN EXAMPLE AND VERIFICATION

The filter design process is described in this chapter with an design example and simultaneously used to verify some of the results obtained in Section 3.2. Section 5.1 presents an illustrative set of filter design parameters obtained from the theory developed in the previous sections for the strip waveguide structure introduced in Section 2.2. Simulation results obtained using the circuit simulator of Chapter 4 for this filter design, are discussed in Section 5.2, and compared to the predicted filter performance in order to verify the equations of Section 3.2. A process flow for fabricating a structure similar to this example structure is briefly presented in Section 5.3. A brief discussion of the electrical parasitic effects and their modeling is presented in Section 5.4.

5.1 Filter Design

In this section, an example filter design is presented that uses the waveguide structure described in Section 2.2. The design parameters for this filter have been optimized by trial and error using the equations derived in Section 3.2. Four set of filter design parameters are presented in Table 5.1. Each column of numbers corresponds to one possible design. The first two columns correspond to the actual case where substrate losses are present. The last two columns correspond to a hypothetical case with the same waveguide where it is assumed that there are no substrate losses, i.e. $a_{cm} = a_m = 0$. All the parameters are calculated at a design frequency of 750 MHz, which means the filter is set to this center frequency. The values calculated here are typically valid when the pitch is also set to $d = \pi/\beta_0 = 1.75$ um, as required by (3.3). The optimization is done for a standard system impedance of $Z_0 = 50$ ohm. As can be seen
in the table, it has been possible to obtain a set of filter design parameters that yields an input resistance close to 50 ohm for both the series model and the parallel model at the same time. This is generally not required and the filter can either be optimized for series operation or parallel operation. The design parameters that neglect substrate loss have been presented in order to examine the performance degrading effect of the substrate loss, which is quantitatively evident in the values of the insertion loss $IL$, and the filter $Q$-factor $Q_{\text{filter}}$. The required DC voltage is also much lower when there are no substrate losses. Thus, a waveguide design that has lower substrate losses can substantially improve the filter performance.

From ANSYS Static analysis, it turns out that $x_{dc} \ll x_{cap}$, so the approximation $x_{cap} \sim x_0$, can be made, as mentioned in the table. The pull-in voltage in (2.26) for this design, obtained from the ANSYS Static analysis is found to be $V_p = 123$ V. Since the operating DC voltage is 100 V for the case with substrate loss, the transducers are in the stable region and will not collapse. Ideally, the operating DC voltage should be much lower than this to accommodate for fabrication uncertainties. It should be mentioned here that some of the structural design parameters obtained here may not be very practical with the current state of the art in microfabrication. However, these sets of parameters serve as a good example to illustrate the filter design process.
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Unit</th>
<th>With substrate loss</th>
<th>No substrate loss</th>
</tr>
</thead>
<tbody>
<tr>
<td>$Z_{mb}$</td>
<td>s/kg</td>
<td>54000</td>
<td>54000</td>
</tr>
<tr>
<td>$a_{cm}$</td>
<td>-</td>
<td>-0.06</td>
<td>0</td>
</tr>
<tr>
<td>$a_{rm}$</td>
<td>-</td>
<td>0.06</td>
<td>0</td>
</tr>
<tr>
<td>$x_{cap}$</td>
<td>Nm</td>
<td>30</td>
<td>30</td>
</tr>
<tr>
<td>$V_{dc}$</td>
<td>V</td>
<td>100</td>
<td>25</td>
</tr>
<tr>
<td>$N$</td>
<td>-</td>
<td>250</td>
<td>500</td>
</tr>
<tr>
<td>$M$</td>
<td>-</td>
<td>20</td>
<td>10</td>
</tr>
<tr>
<td>$\text{Re} \left[Z_{in}(\omega_0)\right]$</td>
<td>ohm</td>
<td>42</td>
<td>44</td>
</tr>
<tr>
<td>$1/\text{Re} \left[Y_{in}(\omega_0)\right]$</td>
<td>ohm</td>
<td>61</td>
<td>59</td>
</tr>
<tr>
<td>$Q_{mat}(\omega_0)$</td>
<td>-</td>
<td>0.6</td>
<td>0.6</td>
</tr>
<tr>
<td>$L_{mat}$</td>
<td>nH</td>
<td>10.7</td>
<td>10.7</td>
</tr>
<tr>
<td>$p_{wg}(\omega_0)$</td>
<td>-</td>
<td>0.06</td>
<td>0.03</td>
</tr>
<tr>
<td>$IL(\omega_0)$</td>
<td>dB</td>
<td>-30</td>
<td>-36</td>
</tr>
<tr>
<td>$Q_{filter}(\omega_0)$</td>
<td>-</td>
<td>7.8</td>
<td>8</td>
</tr>
<tr>
<td>$Q_{loss}$</td>
<td>-</td>
<td>8.3</td>
<td>8.3</td>
</tr>
</tbody>
</table>

Table 5.1 Design parameters optimized for an example filter design employing the waveguide structure of Section 2.2, and the corresponding filter performance predicted from the equations obtained in Section 3.2.
5.2 Results

Results of the circuit simulation for the filter design discussed in Section 5.1 using the circuit simulator described in Chapter 4 are presented in this section. The aim is to compare these results with the expected results from Section 5.1 that were calculated using the filter design equations derived in Section 3.2. In these simulations, it is assumed that $d_c = 100 \text{um}$, $d_f = 10 \text{um}$ and $Z_{ml} = Z_{m0}$ [See Figure 4.1]. Thus, in order to be consistent with the conditions of Section 3.1, the acoustic waveguides are simulated to be always terminated in a matched load at all frequencies. Three types of plots are presented here, namely, the input impedance defined in (4.6) with $Z_{ml1} = Z_{ml2} = Z_{m0}$, the conjugate of the image impedance defined in (4.4) and the filter response of the filter, $S_{21}$, in dB, obtained from (4.3). For some of the plots, simulation results are presented for a hypothetical filter design that does not experience any substrate losses. Unless otherwise stated, the simulation results computed in the presence of substrate loss are by default based on the design parameters specified in the first column of Table 5.1, whereas, for simulation results computed in the absence of substrate loss are by default based on the design parameters specified in the third column of Table 5.1. As discussed in Section 3.1, it is usually practical to implement only a discrete number of DC levels for biasing individual transducers, instead of a continuum. To reflect this practical restriction, unless mentioned otherwise, four DC levels, two positive and two negative, are used in the following simulations.
5.2.1 Input Impedance

The plots for the input impedance of the transducer array presented here are all computed for a filter center frequency of 750 MHz. In order to be able to compare the input impedance levels with the results obtained from theory, (3.3) has to be satisfied. Hence, the transducer pitch $d$ is also set to half the wavelength of the propagating mode at 750 MHz. In these plots, the effect of the reactance or susceptance of the total DC capacitance of the transducers has been removed from the input impedance and input admittance for better visualization. Figure 5.1 shows the input impedance and input admittance obtained in the presence of substrate loss. It can be seen that the imaginary parts go to zero at the center frequency as discussed in Section 3.2. Also, the real parts at the center frequency are equal to the values estimated in Table 5.1 using (3.23) and (3.24). Figure 5.2 shows the real part of the input impedance in the absence of substrate loss, comparing the result obtained from simulation and the theoretical plot obtained from (3.18) or (3.20). These plots are approximately equal only near the center frequency where (3.3) is satisfied. It can be seen that the frequency span of the central lobe of the simulated curve is approximately twice as wide as that of the theoretical curve. Hence, the frequency span of the theoretical curve calculated from the distance between the close-in nulls and the computed filter $Q$ of (3.30) can only serve as a rough estimate for the filter bandwidth and $Q$.

In order to study the effect of the number of transducers, $N$, on the input impedance and input admittance of the array, the simulations were run for different values of $N$, keeping all the other parameters constant. Figure 5.3 shows the real parts of the resulting input impedance and input admittance obtained from these simulations in the absence of substrate loss, whereas, Figure 5.4 shows the corresponding results in the
presence of substrate loss. Note that the input admittance in both these figures has been divided by $N^2$ for better visualization. As predicted by (3.23), the input impedance in Figure 5.3, which follows the series model, appears to be independent of $N$ at the center frequency. Similarly, as predicted by (3.24), the input admittance in Figure 5.3, which follows the parallel model, appears to be directly proportional to $N^2$ at the center frequency. Also, as predicted by these two equations for high substrate loss, the input impedance in Figure 5.4 appears to be inversely proportional to $N$, whereas, the input admittance in the same figure appears to be directly proportional to $N$. It should be noted here that this may not be true if there is interaction between the partial leakage waves generated at individual transducers, although, the model developed in this work is not set up to capture this interaction. Apart from the impedance values, another important observation can be made from these plots. Considering the circuit models of Figure 3.3 and Figure 3.4, the frequency dependence of the real part of the input impedance or input admittance appears to be an indicator of the Q-factor of the filter response. Accordingly, from Figure 5.3, it can be seen that the filter Q-factor is directly proportional to $N$, as estimated by (3.30). For high substrate loss, the saturating effect of $N$ on the filter Q-factor, as predicted by (3.32) and (3.33), is evident in Figure 5.4. Finally, it can be concluded that, these plots of input impedance and input admittance validate the theory and filter design equations developed in Chapter 3 to some extent. These observations are also in agreement with the results of [37].
Figure 5.1 Input impedance and input admittance of the transducer array, excluding the total DC capacitance, in the presence of substrate loss. At the center frequency, the imaginary parts go to zero and the real parts are equal to the expected values.
Figure 5.2 Real part of the input impedance obtained from simulation and theory, in the absence of substrate loss. These plots are approximately equal only near the center frequency, as expected. The width of the central lobe of the simulated curve is approximately twice as wide as that of the theoretical curve. Separation between the close-in nulls of the theoretical curve give a rough estimate of the Q-factor of the filter.
Figure 5.3 Effect of the number of transducers, $N$, on the real part of the input impedance and input admittance of the transducer array, in the absence of substrate loss. Note that the input admittance has been divided by $N^2$ for better visualization. At the center frequency, the input impedance appears to be independent of $N$ and the input admittance appears to be directly proportional to $N^2$, as expected.
Figure 5.4 Effect of the number of transducers, $N$, on the real part of the input impedance and input admittance of the transducer array, in the presence of substrate loss. Note that the input admittance has been divided by $N^2$ for better visualization. At the center frequency, the input impedance appears to be inversely proportional to $N$ and the input admittance appears to be directly proportional to $N$, as expected.
5.2.2 Image Impedance

To get an idea of the port impedances looking into the ports of the filter, simulated results of the conjugate of the image impedance, in the presence of substrate loss, are presented here. The filter has a symmetric design, so the image impedances at the input and output ports are the same. In these plots, the effect of the reactance or susceptance of the total DC capacitance of the transducers has been removed from the image impedance and image admittance for better visualization. As explained earlier, the transducer pitch has to be half the smallest wavelength within the entire operating band of the filter. From Figure 2.11, the smallest wavelength occurs at the highest frequency of operation, i.e. 1000 MHz. Hence, the transducer pitch \( d \) is set to half the wavelength at 1000 MHz. Figure 5.5 shows the conjugate of the image impedance and image admittance for a filter center frequency of 750 MHz. It can be seen that the imaginary parts go to zero at the center frequency. The real parts at the center frequency are different but close to the theoretical values estimated in Table 5.1. This is expected because the transducer pitch is based on a wavelength that is different from the one at the center frequency, thus violating (3.3). Figure 5.6 shows the effect of changing the center frequency of the filter, \( \omega_0 \), on the real parts of the conjugate of the image impedance and image admittance, keeping all other parameters constant. Empirically, it appears that the image impedance at the center frequency is inversely proportional to \( \omega_0^2 \), while the image admittance at the center frequency is inversely proportional to \( \omega_0 \). Within the operating band of the filter, values of the image impedance appear to be varying by a factor of 10, while those of the image admittance appear to be varying by a factor of 2.
Figure 5.5 Conjugate of the image impedance and image admittance of the filter, excluding the total DC capacitance, in the presence of substrate loss. At the center frequency, the imaginary parts go to zero and the real parts are different but close to the expected theoretical values.
Figure 5.6 Effect of the center frequency of the filter, $\omega_0$, on the real parts of the conjugate of the image impedance and image admittance, in the presence of substrate loss. At the center frequency, the image impedance appears to be inversely proportional to $\omega_0^2$ and the image admittance appears to be inversely proportional to $\omega_0$. Also, the values within the operating band appear to be varying by a factor of 10 for the image impedance, and by a factor 2 for the image admittance.
5.2.3 Filter Response

Various filter response plots are presented here, mainly to examine the effect of using varying number of DC levels and, either a series or parallel inductor to cancel out the total DC capacitance of the transducers. The simulated responses of a filter tuned to various center frequencies, in the absence of substrate loss, are presented in Figure 5.8; while the simulated responses of a filter tuned to various center frequencies, in the presence of substrate loss, are presented in Figure 5.9. To avoid redundancy, the legend for all these plots is shown in Figure 5.7. The first plot in Figure 5.8 is simulated for a filter design that uses 100 DC levels to excite the transducers, and a series inductor to cancel out the transducer capacitance. The second plot in Figure 5.8 is also simulated for a filter design that uses 100 DC levels to excite the transducers, but with a parallel inductor for cancelling out the transducer capacitance. The third plot in Figure 5.8 shows the filter responses generated with only 2 DC levels, one positive and one negative, and a series inductor to cancel out the transducer capacitance. This plot shows that, in the absence of substrate loss, only 2 DC levels are enough to generate an acceptable filter response. There could be slight shifts in the center frequencies, but they are not noticeable for typical values of $N$. All the plots in Figure 5.9 are simulated for a filter design that uses a series inductor to cancel out the transducer capacitance, but a varying number of DC levels, namely, 100, 2 and 4. It appears that when substrate loss is significant, at least 4 DC levels are required to generate filter responses that are close to the ones generated using 100 DC levels. The performance degrading effect of the substrate loss is clearly evident in these plots. Insertion loss is quite high and is close to the values estimated in Table 5.1. Also, the Q-factor of the filter response is significantly reduced due to the presence of substrate loss.
Figure 5.7 Legend for the filter response plots.
Figure 5.8 Simulated filter response in the absence of substrate loss. It appears that, only 2 DC levels are enough to generate an acceptable filter response. Slight shifts in the center frequencies due to this discretization are not noticeable for typical values of $N$. 
Figure 5.9 Simulated filter response in the presence of substrate loss, using a series inductor to cancel out the transducer capacitance. It appears that, at least 4 DC levels are required to generate filter responses that are close to the ones generated using 100 DC levels. Insertion loss is quite high as expected and close to the estimated values. The Q-factor of the filter response is also significantly reduced.
5.3 Layout and Fabrication

In this section, a potential way to fabricate the waveguide structure similar to the one proposed in Section 2.2, is briefly discussed. The sample structure introduced in Section 2.2 was completely made of Silicon to simplify the simulations and analysis. The structure described here uses a metal waveguide sitting on thermal oxide instead of a Silicon waveguide. Hence, all the design parameters, performance estimations and simulated results presented in the earlier sections are not valid for this structure and should be re-calculated.

A basic illustration of the layout of a metal based *Strip Waveguide* design and the cross-sectional side view of the device layers is shown in Figure 5.10 and Figure 5.11, respectively. The process starts with a high resistivity intrinsic Silicon wafer. The top side of the wafer is then doped with the appropriate mask to define the electrodes and the conducting channels under the pads of the device. These conducting features can also be formed from conductive amorphous Silicon or poly-Silicon, by doing a reactive ion etch, followed by a trench refill and polish. Once the conducting features are defined, a high quality thermal oxide layer is formed, which is dry etched using an appropriate mask to expose the DC bias locations. This is followed by a high quality LPCVD layer of Silicon Nitride which is dry etched with an appropriate mask to define the locations of the metal waveguides and the transducer air gap. Next, a high quality metal layer is deposited and etched with the appropriate mask to define the metal waveguide arrays and, bias and signal pads. Small holes are etched in the metal waveguide so that it can be released. Finally, the Silicon Nitride is wet etched to release the metal waveguides. DC sources, matching inductors and RF probes can then be connected externally to the chip.
Although, the fabrication process flow described here looks quite straightforward, it can be challenging at higher frequencies of operation due to the smaller dimensions, and may require non-standard fabrication processes. Also, in practice, it is usually difficult to implement a waveguide with a matched load at both ends. Hence the ends of the waveguide are either clamped or left free. The free end condition does not always correspond to an open circuit for all modes. Hence, the mechanical impedance offered by a clamped or free end should be estimated by performing appropriate simulations in ANSYS.

Figure 5.10 Cross-sectional side view of the device layers in the metal based Strip Waveguide.
5.4 Electrical Parasitic Modeling

The exact thicknesses of the layers, transducer spacing, operating DC voltages and dimensions of the mask features can be determined from the desired frequency range of operation of the filter. Once the exact layout of the filter is designed, an electrical parasitic analysis should be done to determine electrical leakage and other electrical parasitic elements. For complex geometries, a commercial electromagnetic FEM software like Ansoft HFSS can be used. These electrical parasitic models can then be integrated with the filter model to improve the accuracy of the simulations. There can be issues with the DC and RF isolation between the electrodes, especially at higher frequencies, considering the small spacing required between the transducers. The parasitic models can greatly help in getting a better insight into such issues during the filter design process. An illustration of the parasitic modeling done for the ridge waveguide structure is shown in later sections.
Chapter 6

OTHER DESIGNS

In this chapter, primarily two designs are described and analyzed in detail. In Section 6.1.6.2, an acoustic waveguide design based on a tethered beam is described, and in Section 6.3, a structure based on a ridge waveguide is discussed. It should be mentioned here that the actual historical order in which the project proceeded was different than the order in which the work has been presented in this dissertation. During the earlier phases of the project, preliminary analysis techniques were developed based on Finite Element simulations to analyze the various proposed structures for the filter. These basic analysis techniques are briefly discussed in Section 6.1. The waveguide analysis presented in the later sections of this chapter is based on these methods. Many of the techniques and concepts presented in this chapter bear similarity to the detailed techniques described in the earlier chapters and some of the descriptions might be redundant. Due to the limited time frame of this project, a filter design based on the ridge waveguide was finalized for fabrication in the earlier phases of the project and analyzed using these basic techniques. Unfortunately, due to fabrication difficulties, the ridge based design was not successful. Also, due to monetary constraints, other potential designs could not be fabricated and tested. Consequently, the research efforts were diverted towards analyzing and modeling the filter in more detail, the results of which have already been presented in earlier chapters. As a result of this different project timeline, simulation results for the ridge waveguide design based on the detailed filter design theory described in earlier chapters which includes transducer-line coupling, are not available. Instead, the analysis results presented in this chapter are based on some basic techniques developed earlier like the ones mentioned in Section 6.1.
In order to realize some of the desired filter properties described in Section 1.1 like isolation from substrate and low leakage, one can imagine a silicon acoustic waveguide structure sitting on top of a PDMS layer. At first this approach looks quite promising, but on second thoughts it can be readily seen that the soft PDMS layer will cause pull-in problems even at low voltages. Also, considering the high electric fields within the transducer, it can lead to dielectric breakdown. Silicon structures sitting on top of PDMS can also be difficult to fabricate. As mentioned in Section 1.1, any acoustic waveguide has many different elastic modes. From the point of view of transduction, the mode which yields a better coupling and high mechanical input impedance is more desirable. In general, shear modes or Rayleigh modes are better in this respect compared to longitudinal modes. Hence, the modes of operation chosen for all conceived structures presented here always have a dominant shear component. Primarily, two different acoustic waveguides were studied before fabrication was undertaken. One of them is a periodically tethered beam in which the primary mode of propagation is a lamb wave. The other is a kind of topographical waveguide consisting of a ridge made on a semi-infinite substrate in which the primary mode of propagation is expected to be a mode similar to a guided Rayleigh surface wave. The first design was discarded in the initial stages due to poor propagation characteristics. The second design was more thoroughly analyzed from a structural, electrical and electromagnetic point of view using numerical and analytical methods. This design was finally chosen for microfabrication.

6.1 Types of Structural Analysis

To design the filter and to optimize its response, it is necessary to get an idea of the modal propagation characteristics of the acoustic waveguides used. It is not always easy to get an analytically expression for the dispersion relations and field distributions in 3 dimensional acoustic waveguides. Sometimes, the only way to analyze a waveguide and
obtain an understanding of the modal characteristics is to perform a Finite Element simulation of the waveguide structure and extract the propagation parameters and other properties from the resulting data. The problem is further complicated by the fact that there is no impedance boundary condition similar to the one in electromagnetics. In this section, a few techniques are briefly discussed that can be used to obtain useful propagation parameters from FEM simulations in ANSYS. These techniques have been used to analyze the 2 proposed waveguides and the results are presented in their respective sections on structural analysis.

Harmonic, Modal and Static analyses can be performed in ANSYS to examine the structural properties of the design. The propagating structure can be viewed as a periodic transmission line with its own equivalent characteristic impedance. In the convention that has been followed, particle velocity is equivalent to voltage and force to current; hence the acoustic impedance is the ratio of velocity to force. Input impedance is the ratio of relative velocity between the electrode and beam and the applied force in the transducer area. Acoustic wave impedance of a uniform plane wave with pure shear and pure longitudinal polarizations in an infinite medium can be easily calculated using the bulk and shear elastic modulus. In general continuous or periodic guided structures, the equivalent of characteristic impedance can be estimated from the power flow or the input impedance seen by an exciting source in an infinite acoustic waveguide. Power flow can be calculated from the stress and velocity using the acoustic Poynting theorem. In an infinite waveguide, the characteristic impedance equals twice the input impedance at any point. For simple continuous acoustic waveguides like beams, the characteristic impedance of pure shear and pure longitudinal modes can be simply calculated from the cross sectional area and material properties. By using harmonic and modal analyses to analyze appropriate test structures with proper excitations and boundary conditions, an
estimate of the input impedance, equivalent characteristic impedance, power loss and the propagation velocities of modes, can be obtained.

A harmonic *propagation analysis* can be done by analyzing a cascade of unit cells of a guided structure terminated with Perfectly Matched Layers (PML's). The PML's have slowly increasing attenuation which ensures that there is no reflection and can simulate an infinite waveguide. This technique only works at high frequencies where the length of the lossless layers is more than a few wavelengths, which implies that the propagation analysis estimations are reliable only at higher frequencies. Power loss inside the acoustic waveguide can be studied by calculating the power flow using the pointing vector in the direction of propagation at successive cross sections inside each unit cell for each frequency. Periodic measurements in the structure can be used to estimate the velocity of propagation. Input impedance at the exciting electrode can be used to approximate the characteristic impedance of the acoustic waveguide. A modal-harmonic *excitation analysis* can also be performed by cascading a few unit cells and identifying the propagating modes using modal analysis. The fields at various ports for a given mode can be used to excite the same structure to perform a harmonic analysis. This single moded simulation can be used to estimate the ABCD parameters and invert for the propagation velocities. With the help of correct boundary conditions, a harmonic *even-odd analysis* can be performed for a single unit cell to obtain the input impedance for identifying the parallel and series resonances of the structure for further modeling. In simple structures, a modal analysis can be directly used to estimate the propagation velocity of each mode with the help of resonant frequencies and dimensions. An important concern is the reflection behavior of the free end of the guided structure in terms of its characteristic impedance. It is different for different modes and is not the same as an electrical open circuit or acoustic open end for all modes. The free end is
equivalent to an extended or truncated waveguide with an open end. Based on modal
simulations of simple waveguide sections of different lengths with open and free end
boundary conditions, the free end impedance or the equivalent electrical length can be
estimated for use in modeling the termination of the waveguide. Finally, a **static
analysis** of the structure helps to determine the pull-in voltage of the capacitive
transducer. This helps to set a limit on the applied DC bias voltages so that a short
circuit can be avoided.

6.2 Tethered Beam Waveguide

An acoustic waveguide using Lamb waves as the primary mode of propagation was
analyzed. After a thorough analysis it became clear that the structure led to significant
loss and the design was rejected. Few variations of the design were also analyzed but
were discarded either due to fabrication difficulties or inefficient propagation
characteristics. An approximate electrical equivalent model was also developed in ADS
based on the parameters extracted from ANSYS.

6.2.1 Structure

A free floating beam without any anchors is the simplest acoustic waveguide that can be
conceived, but such a structure is not practical. The immediate solution is to anchor the
beam using tethers at many points. These tethers have to be thin compared to the beam
so that they don’t load the beam too much and do not offer any significant impedance.
The tether dimensions also determine the operating bandwidth of the filter. For single-
moded operation at the operating frequency, the lateral dimensions of the waveguide
must be less than half the wavelength. This requires that the beam should not be more
than 2.5 um at 1 GHz, assuming a shear mode of propagation. Correspondingly, the
tethers should have a much smaller dimension so that they don’t interfere substantially
with the propagation. Such small dimensions need electron beam lithography and can be difficult to fabricate. So it was decided to make the tethers as thick as the beams and operate the filter at a frequency band where the tethers would resonate and not affect the propagation in the beam. The primary mode of propagation in such a structure is a lamb wave.

Figure 6.1 shows half of the unit cell of the structure. Many parallel beams are used to bring down the total acoustic impedance. There is an electrode between two adjacent beams that excites the beams from sides. Electrodes are fed by bridges across the beams. The tethers and electrodes are anchored on isolated islands between adjacent beams. The electrode regions that excite the beams are all isolated from each other and have small dimensions in order to avoid exciting any resonant modes in them.

6.2.2 Electrical Equivalent Modelling

In the past, researchers have tried to apply microwave concepts to the modeling of acoustic waves and waveguides [23][24]. An electrical equivalent model is useful for quickly optimizing the parameters of the design and to test its performance. By setting appropriate boundary conditions on a mechanical unit cell for two extreme cases, an even-odd harmonic analysis was done in ANSYS to identify the parallel and series resonances in the input impedance seen by the electrode. Results of the simulation illustrating the particle displacement are shown in Figure 6.1. An attempt was made to replicate this response using an electrical circuit in Agilent ADS. After several modifications the model that most closely approximated the mechanical unit cell, is shown in Figure 6.2.
Figure 6.1 An even-odd simulation showing particle displacements. This simulation was used to extract the electrical equivalent model parameters.

Figure 6.2 Equivalent electrical circuit of the unit cell modeling the shear mode in the beams and shear and longitudinal modes in the tethers. Mechanical losses and reactive effects are also accounted for.
The mode of propagation in the beams is quasi-shear and in the tethers it is quasi-shear for the odd case and quasi-longitudinal for the even case. A propagation analysis and modal analysis was conducted for a section of beam to estimate the propagation velocity and characteristic impedance of its 3 primary modes depicted in Figure 6.3. Acoustic impedance and the various types of structural analysis are explained in more detail in the section on structural analysis. The dispersion data and characteristic impedance curves obtained from ANSYS, as shown in Figure 6.4, are used to model the transmission line segments that represent the beam and tethers.

Figure 6.3 ANSYS modal analysis showing the 3 primary modes of a section of beam – Quasi-shear, Torsional and Quasi-longitudinal.

Figure 6.4 Mode propagation velocities and characteristic impedances extracted from ANSYS simulations for the beam section for all 3 primary modes.
Capacitors and inductors are used to model the behavior of anchors and resistances are used to model the loss into the substrate. All the values in the circuit were tuned several times to fit the mechanical response. Input impedance from ANSYS and ADS for both even and odd cases is shown in Figure 6.5. All the resonances could not be accounted for using the electrical model. The complex field interaction between the stress tensor and velocity fields at the mechanical T-junction of the beams and tethers is especially difficult to model using an electrical circuit.

Figure 6.5 Input impedance for the even and odd cases from ANSYS simulations compared with the ADS model after optimization. Not all resonances are accounted for by the model.

6.2.3 Structural Analysis

A propagation analysis of the design was performed. A sample structure with 2 unit cells used for the excitation analysis is shown in Figure 6.6. The unit cells are stacked on PML’s that simulate an infinite substrate. The long cascaded structure used for propagation analysis and the resulting simulation at 250 MHz is shown in Figure 6.7.
Figure 6.6 Structures of 2 unit cells used in excitation analysis and the resulting displacement field distribution.

Figure 6.7 Cascaded unit cells of the tethered beam design used for propagation analysis in ANSYS showing the Perfectly Matched Layers (PML’s). Results of the displacement field are also shown on the right.

A lamb wave travelling along the beam is clearly visible in the simulation. The fields in the tethers are not a simple shear or longitudinal wave and can be difficult to model. Propagation parameters derived from these simulations are shown in Figure 6.8. The characteristic impedance which is twice the input impedance from the propagation analysis is around 15000. Estimated propagation velocity is around 3000 m/s. Shear wave velocity obtained from the modal simulation of a beam is also shown for comparison. Power loss into the substrate is quite significant and there is no single band
that is wide enough where the operating range can be fixed. A static analysis of the structure shows that the pull-in voltage is around 220 V.

Figure 6.8 Data extracted from ANSYS showing power loss, input impedance and estimated mode propagation velocity.

Equivalent electrical lengths of the free end estimated from the modal analysis of a section of beam are shown in Figure 6.9. To understand how the electrical lengths are calculated, consider the 2D illustration of a section of waveguide in Figure 6.9. At a given frequency, the lengths of waveguide sections with open and free end boundary
conditions that generate the fundamental harmonic of each mode, are found as $l_{\text{open}}$ and $l_{\text{free}}$, respectively. $Z_{\text{open}}$ is infinite, hence the free end impedance can be written as,

$$Z_{\text{free}} = -jZ_{\text{md}} \cot(\beta (l_{\text{open}} - l_{\text{free}})/2)$$

(6.1)

The electrical length is $\beta (l_{\text{open}} - l_{\text{free}})/2$. A sample simulation showing the shear modes in a beam section with open and free end boundary conditions is also shown in the figure. For torsional and longitudinal modes, the free end is the same as an open end. For a shear mode, it is equivalent to a waveguide truncated by around 45 degrees with an open end. Note that in this estimation of the free end impedance it is assumed that the modes chosen for comparison from the open end and free end simulations are equivalent.

Figure 6.9 Modal simulations in ANSYS showing open end and free end modes that are assumed to be comparable. Corresponding estimated free end electrical length is shown in the accompanying graph.
Due to huge power loss and low propagation velocity, this design with the lamb wave as the mode of propagation was abandoned. Each unit cell in this design is around 16 um wide, which reduces the number of parallel beams that can be fabricated on a single chip. This is another disadvantage because it becomes difficult to bring down the total electrical impedance of the filter.

6.3 Ridge Waveguide

A different topographical waveguide consisting of parallel ridges in single crystal silicon that would overcome the shortcomings of the previous design was designed, analyzed and optimized. In the previous design it was seen that the tethers and electrodes lead to significant losses. The new structure tries to reduce the loss by making the electrodes a part of the propagating structure and using modes similar to Rayleigh waves that decay naturally in the transverse direction. Some issues that can arise during the filter design stage are mentioned in Table 2 of the original proposal [9]. The present design addresses these issues as follows -

1. Spurious passbands - Narrowband matching network
2. Multi-moding - Many parallel ridges
3. Standing waves - Tall ridges propagating Rayleigh mode, matched port impedances
4. High impedance - Many ridges, small transducer gap
5. Mechanical coupling to bridge electrodes - Electrodes part of the propagating structure
6. Transducer capacitance - Multiband matching network
7. DC leakage and Dielectric breakdown - High quality thermal oxide, medium resistivity silicon, ion implantation
This design was analyzed in ANSYS to estimate some propagation parameters. An electrical parasitic model was then developed in ADS and an electromagnetic simulation was also done in HFSS to get an idea of the parasitics and the values of the DC bias and RF signal levels. A circuit simulator was developed in MATLAB to emulate and optimize the frequency response of the FIR filters with various parameters and to obtain the values of the matching elements. This helped to gain a better understanding of the filter performance.

A deeper investigation of this waveguide branched out into a more rigorous theoretical analysis of its operating modes, as explained in Chapter 7. Although this offshoot did not significantly aid in the filter design process, it did provide some literary contributions. After the design was finalized, the fabrication process flow was outlined and an automated layout generator was developed in MATLAB for creating the masks of the design. A few resonator designs and chips for measurement and TRL calibration were also included in the layout. Microfabrication of this device was undertaken, but several challenges were encountered during the process, as explained in Chapter 8.

6.3.1 Structure

The new design has a differential topology in which the electrostatic attraction between the plates of the capacitive transducers are expected to primarily excite modes similar to non-leaky guided Surface Acoustic Waves (SAW) inside the ridge waveguides and Lamb or shear modes in the electrodes. SAW waves or Rayleigh waves decay in the direction perpendicular to the direction of propagation, hence they are expected to radiate less into the substrate. A set of parallel ridges etched in Silicon act as the waveguide and a set of equally-spaced electrodes running perpendicular to the ridges and anchored on top of the ridges in a checkered pattern excite acoustic modes that
propagate along the structure. The alternating topology of the electrodes, as shown in Figure 6.10, has certain advantages. Every electrode is anchored on every alternate ridge. Adjacent electrodes are anchored on the other set of alternate ridges. Thus both the ridges and electrodes have alternating polarities. By designing the lengths of the electrode segments between the ridges to be equal to half the wavelength of the shear mode in the electrodes at the center frequency of the operating band, the electrodes can be made to resonate and become a part of the propagating structure. Since the ridges in this design are vertical and are only 2 um wide with a 2 um gap between adjacent ridges, a large number of parallel ridge waveguides can be accommodated in a small space on a single chip. An illustration of the complete design including the ridge waveguides, the RF and DC contacts and the electrodes is also shown in Figure 6.10.
Figure 6.10 Illustration showing the alternate topology of the ridge waveguide design. On the right is an illustration of a single die of a final filter device. Gray region is the SCS silicon forming the ridges and pads; and the orange region corresponds to the metal layer forming the electrodes and the RF and DC contacts.

6.3.2 Structural Analysis

A complete structural analysis of the design was done, which yielded various parameters like the power loss, estimated propagation velocity of the primary mode, approximate input impedance and the depth profile of the vertical particle displacement field, as shown in Figure 6.12. Figure 6.11 shows the structure used for propagation analysis and
the result of the simulation showing the vertical particle displacement. The PML’s used
to absorb the propagating waves can also be seen as colored layers.

![Image](image.png)

Figure 6.11 Unit cells cascaded for propagation analysis showing the multicolored
Perfectly Matched Layers for simulating radiation conditions. Corresponding
displacement field distribution from ANSYS at 400 MHz is shown on the right.

Propagation velocity is found to be around 4800 m/s which is quite close to the Rayleigh
wave velocity. The depth profile also shows the wavelength calculated for a Rayleigh
wave. It shows that the depth penetration of the wave is almost equal to one wavelength,
as is expected for a Rayleigh wave. To avoid aliasing, the distance between two
consecutive electrodes must be less than half a wavelength. Due to fabrication
difficulties, the electrodes cannot be close than 5 um, which means the highest operating
frequency is around 480 MHz. The power loss image obtained from the propagation
analysis shows that the region below this frequency limit with the lowest power loss lies
between 250 and 400 MHz, hence the operating band has been fixed in this region and
the electrode pitch is set at 5.5 um. From the input impedance graph of propagation
analysis, the characteristic impedance is found to be almost equal to 20000. The peaks
and nulls in the reactance plot can be correlated to the power loss in the waveguide. It is
seen that the reactance is relatively low in the operating region. A static analysis shows that the pull-in voltage of the structure is around 120 V.

Figure 6.12 Data extracted from the ANSYS simulations showing the power loss, depth penetration, input impedance and estimated mode propagation velocity for the ridge acoustic waveguide.

The equivalent electrical length of the free end as estimated from modal analysis is shown in Figure 6.13. A typical modal simulation of 2 blocks with free and open boundary conditions shows the modes whose resonant frequencies are used to calculate the free end conditions. In this calculation it is assumed that these modes are comparable. It is seen that the free end of a ridge waveguide corresponds to an open ended ridge waveguide extended by around 45 degrees.
Figure 6.13 Free end and open end modes obtained from ANSYS modal analysis for a section of the ridge waveguide that are assumed to be comparable. The corresponding estimated equivalent electrical lengths.

In the design, the electrodes need to resonate with the ridge waveguides in the operating band, so that they can be a part of the propagating structure and offer very low impedance. This resonance is shown in Figure 6.14 which shows two snapshots of the synchronized ridge electrode oscillations separated by half a time period. A simple harmonic analysis shows that a nickel electrode that is connected symmetrically at both ends and is excited in the middle has to be 1 um thick, 4 um wide and 8 um long to exhibit a series resonance at around 400 MHz. Impedance seen by the exciting source is shown in Figure 6.15, along with the operating region and the displacement field.
Figure 6.14 ANSYS harmonic analysis showing the synchronized ridge electrode oscillations separated by half a time period. The color represents the particle displacement in the vertical direction along the height of the ridges.

Figure 6.15 ANSYS harmonic analysis of a section of electrode showing series resonances around 400 MHz.
6.3.3 Electrical Parasitics

A thorough analysis of the parasitic resistances and capacitances was performed in order to get an idea of the RF signal losses and actual DC bias voltages. This helps to determine the signal voltages that need to be applied during the testing phase. In the design, DC bias lines are essentially ridges on either side of the chip. Electrodes are alternately connected to RF+ and RF- through large MIM DC bypass capacitors. They are also in direct contact with the appropriate DC bias lines depending on the tuning frequency. Ridges are alternately connected to RF+ and RF- by the electrodes through MIM anchors. In the region midway between the input and output transducers, all waveguides are in direct contact with DC ground. There is an undoped region on the ridges between the middle DC ground region and the transducer region which ensures that the ridges remain RF isolated but are close to DC ground. Resistance of this undoped region is a critical parameter and depends on the undoped length, doping levels and substrate resistivity. The parasitic simulation helps to ascertain these values as well as the DC bypass capacitor areas. Figure 6.16 shows the complete circuit schematic of the parasitic circuit model developed using Agilent ADS. It includes leakages through the buried oxide, parasitics due to airgap MAM and anchor MIM capacitors, leakages caused by wide RF and DC pads, effects of the bias electrodes and capacitances caused by proximity of the structures. It also accounts for leakage through the MIM capacitors formed by the oxide anchors. The RF and DC simulation results are shown in Figure 6.17. After optimizing some parameters, it is possible to get 60% of the input RF signal to drop across the transducers. It is also seen that a good input-output RF electrical isolation is present in the design. With appropriate doping levels and lengths, almost the full applied DC bias voltage can be seen by the transducers.
Figure 6.16 ADS schematic of the complete electrical parasitic model of the ridge waveguide design.
Figure 6.17 Results of the ADS parasitic model showing the RF signal drop and DC bias voltage across the airgap transducers for typical design parameters. RF simulation shows that around 60% of the input RF signal drops across the transducers and there is very good input-output electrical isolation. DC simulation shows that with practical doping levels, there is negligible drop in the DC bias levels.

6.3.4 Electromagnetic Simulations

Adjacent ridges have opposite polarity and their physical separation is only 2 um. This can lead to parasitic capacitances between the 2 RF ports. An electromagnetic simulation was done in Ansoft HFSS to get an estimate for the overall capacitance seen at the waveport between the 2 electrodes. Figure 6.18 shows the unit cell that was simulated in HFSS along with the waveport and a plot of the input impedance. In a typical filter there about 200x300=60000 of these unit cells that are electrically parallel to each other. So the effective capacitance is around 30 pF, which gives an impedance of 15 ohms at 350 MHz. This parallel capacitance needs to be cancelled by the shunt inductor or series inductor at the center of the matching bandwidth. The parasitic resistance turns out to be around 3000 ohms for 60000 unit cells and comes in parallel with the 50 ohm impedance of the acoustic transducers. Thus the parasitic resistance can be neglected while matching to the system.
Figure 6.18 Unit cell structure defined for electromagnetic simulation in Ansoft HFSS. Results show that for a typical design, the parasitic resistance is 3000 ohms and the reactance is 15 ohms at the design frequency, which needs to be cancelled by the matching inductor.

6.3.5 Filter Response

A circuit simulator for the complete filter circuit was developed in MATLAB, as described in Chapter 4. The parameters obtained from the ANSYS simulations, namely the transmission line characteristics and free end behavior of the waveguides, were used to create blocks for each unit cell. A cascade of unit cells with the appropriate bias voltages, terminations and matching inductors was used to simulate the filter response. An illustration of the circuit diagram for 3 electrodes is shown in Figure 6.19. The Mason’s model was used to model the capacitive transducer, as marked in the figure. Each unit cell in the simulation is, in general, an equivalent model of the unit cell or a black box with network parameters derived from Agilent ADS or ANSYS. In the present case, it is just modeled as a segment of transmission line with length equal to the pitch of the tap line. This circuit model helped in simulating and optimizing the response at different frequencies by varying various parameters like the number of acoustic
waveguides and electrodes, air gap, pitch, ridge and electrode widths, DC bias functions and number of DC bias levels. It helped to determine the values of the system impedance required to match the filter RF ports and the inductors required to cancel out the huge reactances seen at the RF ports, both in series and shunt configurations. The effect of mechanical losses in the acoustic waveguides and exponential tapers in the DC bias functions could also be studied using the simulator. The designs selected in the layout are based on this circuit simulator.

Based on the simulations it is found that only 2 DC quantization levels are enough to tune the filter to a particular frequency with sufficient accuracy using around 200 electrodes. A typical frequency response obtained for a particular design tuned at 350 MHz is shown in Figure 6.20, along with its zoomed version. The filter passband is less than 2 MHz and the insertion loss is around 3 dB. This design has 600 ridge waveguides, 250 electrodes, 50 nm airgap, +/- 10 V DC supply, sinusoidal bias function, 4 um wide electrodes, 2 um wide ridges and 5.5 um electrode pitch. It is found that a 1 nH shunt inductor is required to cancel out the parallel capacitance at the tuning frequency. The resulting port input impedance is 51 ohms and the unloaded matching Q
is 24. This is good enough to match the filter to the 50 ohm system impedance and to accommodate sufficient bands within the matching bandwidth.

![Figure 6.20 Simulated filter response of a typical filter design tuned at 350 MHz using only 2 DC bias levels and assuming a mechanical attenuation of 1000 dB/m at 350 MHz in the acoustic waveguide. Fractional bandwidth is around 0.5%.

When a two-port network is simultaneously matched at both ports, the resulting single port input impedance at both ports is called the image impedance. They can be thought to have a series or shunt equivalent as shown in Figure 6.21. (Note: A more detailed model has been derived in the earlier chapters, although, that model is not presented here for reasons mentioned earlier in the introduction of this chapter.) Image impedances calculated using the simulator are also shown in the figure. In general, the port input impedance is a function of the applied DC bias. It is seen from the simulations that the image impedance is dominated by the parallel capacitance. Thus the shunt inductor needs to be designed to only cancel out this fixed parallel capacitance for different tuning frequencies within the matching bandwidth. In the series configuration, it can be seen that in order to have a resistance R of around 50 ohms, only 1 or 2 waveguides are needed. Such designs with only 1 or 2 waveguides that can be tuned with a series inductor have also been included in the layout.
Figure 6.21 Shunt and series equivalent models of the port impedances of the filter derived from the image impedances for the filter design tuned at 350 MHz. The series model indicates that for obtaining a 50 ohm port impedance using a series matching inductor, only 1 or 2 waveguides are required.

This simulator was also used to simulate the responses of the tethered beam design. These are shown in Figure 6.22 to illustrate the matching bandwidth and the suppression of spikes. The shunt inductor leads to a matching bandwidth for the filter within which the filter must be tuned. An inductor bank can be used to cover a wider range of frequencies. Due to multiple reflections inside the waveguides, spikes can be present in a lossless simulated response. Mechanical attenuation in the acoustic waveguides can suppress these spikes. An exponential taper can be added to the bias function to suppress the side lobes.
Figure 6.22 Filter responses for the tethered beam design at 1 GHz illustrating the matching bandwidth and the effect of mechanical attenuation in suppressing spikes caused by multiple reflections.
Chapter 7
THEORETICAL MODAL ANALYSIS OF RIDGE WAVEGUIDE

A better insight into the performance of an acoustic waveguide can be obtained by deducing the elastic modes supported by the waveguide and their propagation characteristics. To this end, an intuitive solution to the general elastomechanic problem of an anisotropic ridge waveguide was investigated. Considering the complexity of elastomechanic fields compared to electromagnetic fields, a purely theoretical solution to the problem is implausible. The problem is further simplified by assuming a ridge with a support at infinity. Thus, a semi-analytical method for finding the elastic modes propagating along the edge of an anisotropic semi-infinite plate is presented in this section. Solutions are constructed as the linear combination of a finite number of the corresponding infinite plate modes with the constraint that they decay in the direction perpendicular to the edge and collectively satisfy the free boundary condition over the edge surface. Such modes are confined to the edge and can be used to approximate solutions of the acoustic ridge waveguides whose supporting structures are sufficiently far away from the free edge. The semi-infinite plate or ridge is allowed to be oriented arbitrarily in the anisotropic crystal. Modifications to the theory to find the symmetric and anti-symmetric solutions for special crystal orientations are also presented. Accuracy of the solutions can be improved by including more plate modes in the series. Numerical techniques used to find modal dispersion relations and orientation dependent modal behavior, are discussed. Results for ridges etched in Silicon using deep RIE, along various angles, are presented. The fundamental symmetric pseudo-Rayleigh and the anti-symmetric flexural modes of the ridge are analyzed. Good agreement is found between Finite Element simulations and results obtained from the theory. For the case of Silicon, it is found that the variations in the modal phase velocity with respect to crystal
orientation are not significant, suggesting that anisotropy may not be a critical issue while designing ridge waveguides in Silicon.

7.1 Introduction

Apart from the application presented in this project, the acoustic ridge waveguide has applications in many fields like microwave engineering and ultrasonics. Due to the low velocity of acoustic waves, compared to electromagnetic waves, miniature scale acoustic transmission lines can be fabricated at microwave frequencies for use in filters and resonators. An acoustic transmission line made from a vertical ridge etched in Silicon is of special interest because of its ease of fabrication and small footprint. The modes of a ridge waveguide decay perpendicular to the edge surface and exhibit strong confinement to the free edge. This makes the ridge waveguide suitable for making low loss acoustic transmission lines. The symmetric mode of the ridge also shows little dispersion over a wide frequency range and is similar to surface waves. Silicon is a diamond-cubic crystal and so is anisotropic. This makes the analysis a little complicated. Secondly, there is no simple expression for the impedance or radiation boundary condition like the one found in electromagnetics.

A significant body of work can be found in the literature, addressing the modal analysis of acoustic ridge waveguides. However, most of the existing work focuses on isotropic ridge waveguides. The ridge as a topographic waveguide has been examined in [17]. Experimental results for a ridge made of the alloy duralumin are presented in [18]. A rectangular overlay waveguide over a rigid substrate has been analyzed in [20][21]. A finite element method analysis of isotropic ridges has been presented in [22]. Using modes of an isotropic infinite plate, approximate modes of a semi-infinite thin ridge are obtained in [29]. Microwave circuit models for the solid-solid interface and free surface of
a solid are given in [24][25] and used in a transverse resonance formulation to derive approximate dispersion relations for an isotropic thin ridge [26][28]. Flexural edge waves in isotropic semi-infinite plates have been studied in [30]. Existence of edge waves in orthotropic thin plates has been shown in [31]. Flexural edge waves on ridges in monoclinic crystals with the ridge lying in the plane of crystal mirror symmetry are examined in [32]. Their uniqueness and a method to obtain their velocity based on impedance calculations has also been presented. Using the modes of an isotropic infinite plate, 3-dimensional symmetric edge waves in semi-infinite plates have been analyzed in [33]. The only possible closed form expression obtained is for the case where the Poisson’s ratio is zero. Some recent work using finite element method for ridges on a rigid substrate has been reported in [34].

An anisotropic ridge or a rectangular acoustic beam, in general, do not have exact analytical solutions. Some numerical methods must be used to arrive at an approximate solution. The method described here aims to arrive at semi-analytical solutions for the modes propagating along the edge of a semi-infinite plate. The basic idea is to express the modes of the semi-infinite plate in terms of the modes of an infinite plate. In the past, a similar semi-analytical approach has been used to find surface waves in infinite anisotropic half spaces and modes of anisotropic plates [12][13][15][16], starting from an orthogonal and complete basis set of plane wave solutions in an infinite anisotropic crystal. Only, modes that decay in depth are considered here. Normally a ridge waveguide is excited from the top and so the modes of interest are only the ones that decay in depth. Thus, the solutions obtained for the semi-infinite plate can be taken as approximate solutions to the modes of an acoustic ridge waveguide with supporting structures that are sufficiently far away from the free edge such that the reflections from the interface can be neglected. The words ridge and semi-infinite plate are used
interchangeably in this discourse. A ridge waveguide having a width of \( w_R \) is illustrated in Figure 7.1. The coordinate system is chosen such that the edge surface is in the \( y-z \) plane, the top surface normal is in \( \hat{x} \) direction, and propagation is along \( z \) axis (lying on the middle of the top plane). This coordinate system will be used in all subsequent analysis. The ridge is made of a homogenous anisotropic material confined to the \(|y| \leq \frac{w_R}{2}, x \leq 0\) region.

![Coordinate system and ridge waveguide](image)

Figure 7.1 (a) and (b) illustrate the geometry and coordinate system of the ridge waveguide. (c) shows the cross section of a practical finite ridge waveguide etched in Silicon.

Section 7.2 outlines basic elasticity theory and a methodology for finding the modes of an anisotropic plate followed by the anisotropic ridge. Section 7.3 discusses the numerical tricks and issues involved in implementing the methods discussed in Section 7.2, along with a detailed example of a ridge etched in Silicon to illustrate the process step by step. In Section 7.4, results of the theory presented in this chapter are verified with a Finite Element simulation in ANSYS, followed by dispersion curves and behavior of modes for ridges etched in Silicon at various angles. Finally, Section 7.5 summarizes and concludes the discussion. The Appendix at the end expresses some of the equations from Section 7.2 in greater detail.
7.2 Theory

A brief overview of elasticity theory and a mathematical description of the general approach are provided in this section. The methodology given here can, in general, be used to find propagating modes bound to the free edge of a ridge waveguide made of an anisotropic material with arbitrary crystal orientation. There are special cases where the plane of the ridge lies along one of the symmetry planes of the crystal. In such a situation, it is possible to find approximate symmetric and anti-symmetric solutions. In this chapter, all matrices are represented by bold symbols, unit vectors by capped symbols, vectors by symbols with an arrow on top and matrix transpose with a superscript $T$.

7.2.1 Elastic Wave Equation

The homogenous time harmonic acoustic field equations are [11],

\[
\nabla \cdot \vec{T} = j \rho \omega \vec{v} \tag{7.1}
\]

\[
c \nabla \times \vec{v} = j\omega \vec{T} \tag{7.2}
\]

where, $\omega$ is the frequency, $\rho$ is the material density, $\vec{v} = [v_x, v_y, v_z]^T = [v_1, v_2, v_3]^T$ is the particle velocity field, $\vec{T} = [T_{xx}, T_{yy}, T_{zz}, T_{yz}, T_{xz}, T_{xy}]^T = [T_1, T_2, T_3, T_4, T_5, T_6]^T$ is the abbreviated notation for the second-order stress tensor,

\[
T = \begin{bmatrix}
T_1 & T_6 & T_5 \\
T_6 & T_2 & T_4 \\
T_5 & T_4 & T_3
\end{bmatrix} \tag{7.3}
\]
and $c$ is the symmetric 6x6 elastic stiffness matrix in abbreviated notation after a bond transformation. The bond transformation expressed in (7.4) rotates the original stiffness matrix in crystal coordinate axes, $c^E$, to the ridge coordinate axes using the bond transformation matrix, $M_b$ given in [11]. It should be mentioned here that in this chapter the symbol $T$ is used to represent the second-order stress tensor, and not the 2-port transmission matrix or the T-matrix in Chapter 4.

$$c = M_b c^E M_b^T$$  \hspace{1cm} (7.4)

In a general triclinic crystal, which only has center point symmetry and no planes of mirror symmetry, $c^E$ has 21 independent constants. For a monoclinic crystal, which has only one plane of mirror symmetry, the stiffness matrix simplifies to 13 independent constants. If the plane of mirror symmetry lies in the $x$-$z$ plane, the corresponding monoclinic stiffness matrix can be used to obtain simplified expressions for symmetric and anti-symmetric solutions to the plate or ridge. Expressions for $\nabla \cdot$ and $\nabla \times$ are given in (A.1) and (A.2), respectively, in the Appendix.

The field equations can be rewritten to give the following wave equation and stress field in terms of the velocity field,

$$\left[ \nabla \cdot (c \nabla v) + \rho \omega^2 \right] \bar{v} = 0$$ \hspace{1cm} (7.5)

$$\bar{T} = -j(c \nabla \times \bar{v}) / \omega$$ \hspace{1cm} (7.6)
For uniform plane waves of the form \( v_{\text{upw}} = e^{-j(k_z z + k_x x + k_y y)} \hat{u} \), the elastic wave equation reduces to the matrix equation in (7.7), also known as the Christoffel equation (for details see (A.3) to (A.6) in Appendix).

\[
\Gamma \hat{u} = 0 \quad (7.7)
\]

Here, \( \hat{u} = [u_x, u_y, u_z]^T \) is the velocity polarization and \( \vec{k} = [k_x, k_y, k_z]^T \) is the propagation vector with \( k = |\vec{k}| \). The solutions are obtained by setting the characteristic determinant equal to zero. For a given material and frequency, the surfaces in \( \vec{k} \)-space satisfying (7.8) correspond to the various slowness surfaces of the infinite crystal. For an isotropic medium, these surfaces are spheres, yielding the longitudinal and transverse solutions. In view of the ridge problem, \( k_z \) is the propagation direction and has to be real, while \( k_x \) must be complex to allow for decay in the transverse direction. By setting \( k_z \in \mathbb{R} \) and \( k_x \in \mathbb{C} \), a 6th degree polynomial in \( k_y \) is obtained, whose roots \( k_{\gamma_m} \), in general, cannot be found analytically as stated by the Abel-Ruffini theorem and must be found numerically as functions of \( k_x \) and \( k_z \) as \( k_{\gamma_m} = k_{\gamma_m}(k_x, k_z) \). If \( k_{\gamma_m} \) is not purely real, then it appears as a pair with its conjugate \( k_{\gamma_m}^* \). If the crystal has mirror symmetry in the \( x-z \) plane, and if \( k_{\gamma_m} \) is not purely imaginary, then it also appears as a pair with \( -k_{\gamma_m} \). For every \( k_{\gamma_m} \), the corresponding \( \hat{u}_m \) is the eigenvector corresponding to the zero eigenvalue. In practice, where \( k_{\gamma_m} \)'s are found numerically, \( \hat{u}_m \) may be found as the eigenvector corresponding to the smallest eigenvalue \( \lambda_\Gamma \) as described in (7.9).
\[
\text{det} \left( \Gamma(k_x, k_y, k_z) \right) = 0 
\tag{7.8}
\]
\[
\Gamma(k_x, k_y, k_z) \hat{u}_m = \min \left( |\lambda_m| \right) \hat{u}_m, \ m = 1...6 
\tag{7.9}
\]

### 7.2.2 Free Anisotropic Plate

Since the wave equation is a linear equation, a linear combination of the plane wave solutions to the wave equation can be used to construct a solution for a free infinite plate, as shown in (7.10).

\[
\vec{v}^{\text{plate}} = \sum_{m=1}^{6} b_m \vec{v}^{\text{apw}}_m 
\tag{7.10}
\]

If the plate is parallel to a plane of mirror symmetry of the crystal, then the roots of (7.8) appear in pairs of \( \pm k_y \) with polarizations \([u_x, \pm u_y, u_z]^T\). In such cases, the plate modes are found to be symmetric (even) or anti-symmetric (odd) and can be expressed as shown in (7.11) and (7.12).

\[
\vec{v}^{\text{plate-e}} = e^{-jk_z z} e^{-jk_x x} \sum_{m=1}^{3} b_{m}^{e} \begin{bmatrix} \cos(k_y y) u_{x_m} \\ -j \sin(k_y y) u_{y_m} \\ \cos(k_y y) u_{z_m} \end{bmatrix} 
\tag{7.11}
\]

\[
\vec{v}^{\text{plate-a}} = e^{-jk_z z} e^{-jk_x x} \sum_{m=1}^{3} b_{m}^{a} \begin{bmatrix} -j \sin(k_y y) u_{x_m} \\ \cos(k_y y) u_{y_m} \\ -j \sin(k_y y) u_{z_m} \end{bmatrix} 
\tag{7.12}
\]
The stress field can be calculated using (7.6) and made to satisfy the following free boundary condition on 3 traction components at each free surface with a surface normal \( \hat{n} \),

\[
\mathbf{T}_{\text{plate}} \hat{n} \big|_{\text{free boundary}} = 0
\]  

(7.13)

The 2 free surfaces of the plate give rise to a matrix equation in 6 unknown coefficients represented by \( \hat{b} = [b_1, b_2, b_3, b_4, b_5, b_6]^T \). Without loss of generality, the boundary conditions are applied at \( x = 0, z = 0 \), as shown in (7.14) (see (A.7) in Appendix). In the symmetric or anti-symmetric cases, the boundary condition needs to be applied only on one side of the plate with a coefficient vector \( \hat{b}^{s/as} = [b_1, b_2]^T \) to give a 3x3 matrix equation, as shown in (7.15) (see (A.8) and (A.9) in Appendix). Note that the symmetric cases have superscript \( s \) and anti-symmetric cases have superscript \( as \).

\[
\mathbf{B} \hat{b} = \begin{bmatrix}
\mathbf{T}_{\text{plate}} \hat{y} \big|_{x=0, y=\frac{w_y}{2}, z=0} \\
-\mathbf{T}_{\text{plate}} \hat{y} \big|_{x=0, y=-\frac{w_y}{2}, z=0}
\end{bmatrix} = 0
\]  

(7.14)

\[
\mathbf{B}^{s/as} \hat{b}^{s/as} = \mathbf{T}_{\text{plate-\text{as}}} \hat{y} \big|_{x=0, y=\frac{w_y}{2}, z=0} = 0
\]  

(7.15)

Exact solutions these equations are obtained where the characteristic determinant in (7.16) goes to zero. In general, it is not possible to find closed form analytical expressions for the solutions of this determinant. A practical approach is to perform a two-dimensional sweep in the \( k_x - k_z \) plane and search for the zeros of the determinant.
(note that $k_{\alpha_{\text{max}}} = k_{\alpha_{\text{max}}} \left( k_x, k_z \right)$ according to (7.8)). For the infinite plate, the search is conducted for real values of $k_x$ and $k_z$, and results in closed contour in the $k_x-k_z$ plane, or $k_{x_n} = k_{x_n} \left( k_z \right)$, corresponding to different propagating modes of the plate at the frequency of analysis. For the purpose of constructing the ridge modes, however, one needs to sweep $k_x$ in the upper half of the complex plane, $\text{Im}(k_x \geq 0)$, which corresponds to the edge-bound solutions. If $k_{x_n}$ is not purely real, then it appears as a pair with its conjugate $k_{x_n}^*$. If the crystal has mirror symmetry in the $y-z$ plane, and if $k_{x_n}$ is not purely imaginary, then it also appears as a pair with $-k_{x_n}$. For every $k_{x_n}$, the corresponding coefficient vector $\hat{b}_n$, theoretically representing the nullspace, is approximated as the eigenvector corresponding to the smallest eigenvalue $\lambda_n$ as described in (7.17).

\[
\det \left( \mathbf{B} \left( k_x, k_z \right) \right) = 0 \quad (7.16)
\]
\[
\mathbf{B} \left( k_{x_n} \right) \hat{b}_n = \min \left( \left| \lambda_n \right| \right) \hat{b}_n, \forall n \quad (7.17)
\]

In Section 7.3, issues involved with locating and tracking the zeros of $\det \left( \mathbf{B} \left( k_x, k_z \right) \right)$ or the poles of $\log \left( \left| \det \left( \mathbf{B} \left( k_x, k_z \right) \right) \right| \right)$ are discussed.
7.2.3 Anisotropic Semi-Infinite Plate Or Ridge

General solutions to the ridge can be constructed as a linear combination of \( N \) modes of the plate as shown in (7.18). Also, the symmetric and anti-symmetric ridge modes can be constructed from the symmetric and anti-symmetric modes of the plate. As mentioned above, only plate modes with \( \text{Im}(k_x) \geq 0 \) contribute to edge-bound solutions. If the crystal has mirror symmetry with respect to the \( y-z \) plane, and if \( k_x \) is not purely imaginary, then the modes should be chosen in pairs of \( [k_x, -k_x^*] \) to enable standing waves that decay in depth. Accuracy of the ridge solution can be increased by including more plate modes in the series, that is, by increasing \( N \).

\[
\vec{\psi}_{\text{ridge-(s/as)}} = \sum_{n=1}^{N} a_n \vec{\psi}_{n\text{plate-(s/as)}}
\]  

(7.18)

Without loss of generality, the boundary condition is applied at \( z = 0 \) on the top surface of the ridge to yield the matrix equation (7.19) which should be satisfied over the range \( |y| \leq \frac{w_r}{2} \). Since the boundary conditions are a function of \( y \), in general it is not possible to obtain an exact solution to the ridge problem. There are two main steps in finding the ridge solution: 1) constructing an appropriate matrix \( A \) corresponding to the field quantities that must vanish on the top surface of the ridge, and 2) finding the value of \( k_z \) that makes this matrix singular and the corresponding nullspace \( \hat{a} \). One way of expressing the boundary conditions is by expanding them in terms of appropriate domain functions over the range of \( y \). Point matching is a special case wherein the domain functions are delta functions. Another approach is to expand the boundary conditions as a Taylor series about a fixed point in \( y_0 \). For the case of free boundary
conditions, setting the traction component and its higher order derivatives at a fixed point in \( y \) equal to zero, the Taylor series expansion about that point approaches zero, thereby forcing the traction in a neighborhood of that point to zero. Here we have chosen to the latter method to construct the approximate boundary conditions as shown in (7.20) (also see (A.12) to (A.16) in Appendix), where, \( \hat{a} = [a_i, \ldots, a_N]^T \) is the coefficient vector weighing each plate mode.

\[
T_{\text{ridge}} \hat{x} \bigg|_{x=0, y=0, z=0} = 0 \tag{7.19}
\]

\[
\frac{d^p}{dy^p} T_{\text{ridge}} \hat{x} \bigg|_{x=0, y=0, z=0} = \left[ A_1(p, y_0) \ldots A_N(p, y_0) \right] \hat{a} = 0 \quad ; \quad p = 0, 1, \ldots, P \tag{7.20}
\]

For \( 0 < |y_0| < w_R / 2 \), (7.20) gives 3 non-trivial equations for each value of \( p \). For \( y = w_R / 2 \) or \( -w_R / 2 \), (7.20) only gives 2 non-trivial equations for \( p = 0 \) because one traction component \( T_{xy} \) is already zero by the plate boundary conditions. For \( y_0 = 0 \), and the symmetric case, \( T_{xy} \) and its even derivatives are zero at \( y_0 \) and (7.20) produces only 2 non-trivial equations for the even values of \( p \). Similarly, the odd derivatives of \( T_{xx} \) and \( T_{xz} \) are zero, yielding only 1 non-trivial equation for every odd value of \( p \). For \( y_0 = 0 \) and anti-symmetric case, (7.20) gives 1 and 2 non-trivial equations for each even or odd value of \( p \), respectively. The number of equations obtained for the \( p^{th} \) derivative for different choices of \( y_0 \) in the general, symmetric and anti-symmetric cases are summarized in Table 7.1. The non-trivial boundary condition equations are combined into a single matrix equation (7.21), as follows,
In order to have a square boundary condition matrix $A^{(s/πr)}$, the values of $p$ much be appropriately chosen such that the total number of equations is $N$.

After constructing a suitable $A$ matrix encapsulating the boundary conditions of the ridge, the next problem is to find its nullspace $\hat{a}$. If the matrix is not square, then the nullspace can be found either by using the method of Lagrange multipliers or by performing a search in the complex space $\mathbb{C}^N$ of $\hat{a}$. If the matrix is square, then the characteristic determinant in (7.22) is set to zero and the values $k_{z_i}$ corresponding to the propagating modes of the ridge are found numerically. The edge bound modes only correspond to those values of $k_{z_i}$ for which none of the contributing $k_{x_i}$'s with non-zero coefficients are purely real. For every $k_{z_i}$, the respective nullspace $\hat{a}_{i\lambda}$ representing the coefficient vector is approximated as the eigenvector corresponding to the smallest eigenvalue $\lambda_{\lambda}$ as described in (7.23). As functions of frequency, the dispersion relations of the ridge modes can be expressed as, $k_{z} = k_{z}(\omega)$, $k_{x} = k_{x}(k_{z}, \omega)$ and $k_{y} = k_{y}(k_{x}, k_{z}, \omega)$. 

$$A \hat{a} = 0 \quad (7.21)$$
\begin{tabular}{|c|c|c|c|}
\hline
\textbf{# equations} & \( y_0 = 0 \) & \( 0 < |y_0| < w_r / 2 \) & \( y_0 = \pm w_r / 2 \) \\
\hline
\textbf{General} & \( p=0 \) & 3 & 3 & 2 \\
 & \text{odd} \( p \) & 3 & 3 & 3 \\
 & \text{even} \( p \) & 3 & 3 & 3 \\
\hline
\textbf{Symmetric} & \( p=0 \) & 2 & 3 & 2 \\
 & \text{odd} \( p \) & 1 & 3 & 3 \\
 & \text{even} \( p \) & 2 & 3 & 3 \\
\hline
\textbf{Anti-symmetric} & \( p=0 \) & 1 & 3 & 2 \\
 & \text{odd} \( p \) & 2 & 3 & 3 \\
 & \text{even} \( p \) & 1 & 3 & 3 \\
\hline
\end{tabular}

Table 7.1 Number of ridge boundary conditions obtained at each point on the \( y \)-axis for the \( p \)\textsuperscript{th} derivative for the general, symmetric and the anti-symmetric cases.

\[ \det \left( A \left( k_z \right) \right) = 0 \quad (7.22) \]

\[ A \left( k_z \right) \hat{a}_j = \min \left( |\hat{A}_\lambda| \right) \hat{a}_j, \forall l \quad (7.23) \]

For thicker ridges, in order to obtain higher order ridge modes, many plate modes must be used in the expansion. Since the solutions obtained are only approximate, the only way to ensure that the solutions are authentic is to check for convergence of \( k z \). If \( k_N z \) is the propagation constant obtained using \( N \) plate modes, then \( \lim_{N \to \infty} k^N z = k z \).

### 7.3 Numerical Calculations

#### 7.3.1 Pole Tracking

As mentioned earlier, the solutions of (7.16), \( k_x \left( k_z \right) \), cannot be found analytically, hence the zeros of the determinant of \( B \) or the poles of \( \log \left( |\det(B)| \right) \) must be found numerically. Performing a raster scan in the complex \( k_x \) plane for each \( k_z \) to track the poles is a computationally intensive task. To expedite the process, some heuristic
methods can be employed to predict and locate the poles. A high resolution raster scan is performed for a few initial values of $k_z$ to identify the precise location of poles. The subset of the plate modes used for synthesizing the ridge solution must be carefully selected and these are then tracked over successive values of $k_z$ to ensure the continuity of the determinant. Using a polynomial fit, the approximate location of poles or $k_{x_k}$'s for each mode are estimated for successive $k_z$'s. A more precise location upto a desired degree of accuracy is then arrived at by using a combination of gradient descent and a 2-dimensional version of the direct line search algorithms. A good prediction helps to make the gradient descent approach converge faster and reduces the search area for the direct search algorithm. For the gradient descent algorithm, the estimates are advanced at each step such that the drop in the value of the function remains constant. Usually the gradient descent algorithm is used to track minimax and tends to become slower when it closes in on zeros. In the present formulation, since the algorithm is operating in the vicinity of a pole, it tends to converge faster as the estimate advances towards the location of the pole. In some cases, when $k_z$ is scanned, it is observed that two poles meet and then fly away in opposite orthogonal directions, rendering the predicted values grossly off the mark. Pathological cases such as these can cause the starting point to lie on a saddle point or a flat area. These are taken care of by limiting the jump in the estimate to within a certain radius from the current position or by resorting to the direct search algorithm. The use of prediction and precision search algorithms makes the overall pole-tracking process hundreds of times faster than a brute force raster scan. This also helps in tracking the behavior of individual plate modes and gives an estimate for their computed dispersion relations.
Once the required plate modes are tracked over $k_z$ to get $k_{x_i}(k_z)$, the appropriate boundary conditions (7.20) for the ridge top surface are applied on them to construct the $A$ matrix. The zeros of the determinant of $A$ or the poles of $\log(|\text{det}(A)|)$ represent the propagation constants of the ridge modes. Locations of these poles are $k_{z_i}$ with the constituent plate modes having $k_x = k_{x_i}(k_{z_i})$. This entire process of pole-tracking and application of ridge boundary condition yields the ridge modes only at a given frequency $\omega$ or ridge thickness, and at a given ridge orientation in the anisotropic crystal. In order to get the full dispersion relations or behavior of the ridge modes over frequency or orientation, this entire process has to be repeated for each frequency point or ridge orientation. This process can again be time consuming and may need significant manual intervention. To automate this process and make it much faster, the plate modes are directly tracked over ridge modes. That is, instead of tracking $k_{x_i}(k_z)$, $k_{z_i}(\omega)$ and $k_{x_{i\alpha}}(k_z,\omega)$, or $k_{z_i}(c)$ and $k_{x_{i\alpha}}(k_z,c)$, are tracked using a combination of gradient descent and direct line search.

### 7.3.2 Spurious Poles

When $\log(|\text{det}(B)|)$ is plotted, some spurious poles are observed that do not correspond to any plate modes, that is, they do not satisfy the plate boundary conditions. These poles appear at locations where $k_{y_{i\alpha}}$'s become redundant with the same velocity polarization vectors. Such degeneracies occur when two $k_{y_{i\alpha}}$'s meet and split in orthogonal directions. In order to remove these spurious peaks and ensure smooth functioning of the automatic pole tracking algorithm, the 6x6 matrix $\tilde{B}$ in (7.24), is
defined for the general case with \( m = 1 \ldots 6 \). Correspondingly, a 3x3 matrix \( \tilde{B}^{(s/\alpha s)} \) in (7.25) and (7.26), is defined for the symmetric and anti-symmetric cases, respectively, with \( m = 1 \ldots 3 \). The determinant of the main plate boundary condition matrix \( B \) or \( B^{s} \) or \( B^{\alpha s} \) is divided by the determinant of this pole nullifying matrix \( \tilde{B} \) or \( \tilde{B}^{s} \) or \( \tilde{B}^{\alpha s} \), respectively, to cancel out the spurious poles in the logarithm of their absolute values, as shown in (7.27). The pole tracking algorithms use \( d(k_{x},k_{z}) \) while tracking the plate modes.

\[
\tilde{B}: \begin{bmatrix} \tilde{B}_{1m}, \tilde{B}_{2m}, \tilde{B}_{3m}, \tilde{B}_{4m}, \tilde{B}_{5m}, \tilde{B}_{6m} \end{bmatrix}^{T} \triangleq \begin{bmatrix} u_{x_{1}}, u_{y_{1}}, u_{z_{1}}, k_{y_{1}}, u_{y_{1}}, k_{y_{1}}, u_{z_{1}}, k_{z_{1}} \end{bmatrix}^{T} \quad (7.24)
\]

\[
\tilde{B}^{s}: \begin{bmatrix} \tilde{B}_{1s}, \tilde{B}_{2s}, \tilde{B}_{3s} \end{bmatrix}^{T} \triangleq \begin{bmatrix} u_{x_{s}}, k_{y_{s}}, u_{y_{s}} \end{bmatrix}^{T} \quad (7.25)
\]

\[
\tilde{B}^{\alpha s}: \begin{bmatrix} \tilde{B}_{1\alpha s}, \tilde{B}_{2\alpha s}, \tilde{B}_{3\alpha s} \end{bmatrix}^{T} \triangleq \begin{bmatrix} k_{y_{\alpha s}}, u_{y_{\alpha s}} \end{bmatrix}^{T} \quad (7.26)
\]

\[
d(k_{x},k_{z}) = \log \left( \frac{\det(\tilde{B}^{(s/\alpha s)}(k_{x},k_{z}))}{\det(\tilde{B}^{(s/\alpha s)}(k_{x},k_{z}))} \right) \quad (7.27)
\]

7.3.3 Example Case

An example is presented to illustrate the procedure for finding ridge modes starting from plate modes. All the numerical computations have been done in MATLAB. Symbolic math has been used to compute the long expressions resulting for the general anisotropic cases. Propagating modes at 350 MHz are calculated for a 2 micron wide ridge deeply etched in a <100> Silicon wafer with the z-axis along the <001> crystal axis. Silicon is a cubic crystal with a density \( \rho = 2300 \) kg/m\(^3\) and 3 independent stiffness constants, \( c_{11} = 165.7 \) GPa, \( c_{12} = 63.9 \) GPa and \( c_{44} = 79.56 \) GPa.
The first step is to identify the plate modes for a 2 micron wide plate in Silicon with the same orientation by doing a raster scan in the complex $k_z$ plane for $k_z = 0$, as shown in Figure 7.2. Plate boundary conditions for the general case have been used in this calculation, hence, $m = 1...6$. The axes in this figure and subsequent $k$-space figures are normalized to the propagation constant of shear waves in bulk Silicon defined as $k_{sh} = \sqrt{\frac{\rho}{c_{44}}}$. The plate modes are then tracked over $k_z$ to obtain the mode constellation shown in Figure 7.3. Individual plate modes have been labeled in this figure. The apparent convoluted evolutions of the curves are manifestations of the inherent modal dispersion relations of the plate modes in the complex plane. The $n = 1$, $n = 2$, and $n = 3$ plate modes are purely propagating (real $k_z$) for small values of $k_z / k_{sh}$ and can be identified as the fundamental longitudinal L1, fundamental shear SH0 and fundamental flexural F1 modes of a plate, respectively. Since the crystal orientation is such that it has mirror symmetry in the $y$-$z$ plane, the plate modes are seen to evolve symmetrically about the imaginary $k_z$ axis. At higher values of $k_z$, the $n = 1$ and $n = 2$ combine to give a hybrid shear-longitudinal plate mode. This is in contrast to the isotropic plate, where the SH0 and L1 modes can be separately distinguished for all values of $k_z$. 
Figure 7.2 Plate modes of a 2 micron wide plate with $x$-axis along the <100> crystal axis and $z$-axis along the <001> crystal axis at 350 MHz for $k_z = 0$.

Figure 7.3 Plate modes of Figure 7.2 tracked over $k_z$ at 350 MHz. The $n = 1$, $n = 2$ and $n = 3$ plate modes are identified as the L1, SH0 and F1 modes of a plate, respectively.
In order to find the modes of the ridge, only 3 symmetric and 3 anti-symmetric plate modes with \( k_{n_i} (n = 1 \ldots 6) \) are used in the expansion and the top boundary conditions are applied at \( y = 0 \) and \( p = 0, 1 \) (see Table 7.1), separately, for the symmetric and anti-symmetric cases. This results in 3x3 square \( A_s \) and \( A_{as} \) matrices whose determinants are plotted in Figure 7.4(a) for the symmetric case and Figure 7.4(b) for the anti-symmetric case. Two zeros are observed in this plot, marked as \( l = 1 \) and \( l = 2 \). Each zero corresponds to a propagating ridge mode. Values of \( k_{z_i} \) and the \( k_{x_i} \)'s of the 6 constituent plate modes along with the magnitude of their coefficients \( a_{nl} \) are listed in Table 7.2.

![Figure 7.4 Determinant of the matrix of ridge boundary conditions separately applied to (a) 3 symmetric and (b) 3 anti-symmetric plate modes tracked in Figure 7.3. Two poles are identified with \( l = 1 \) and \( l = 2 \).](image-url)
It can be seen that the main contribution to \( l = 1 \) is from the 2 fundamental symmetric plate modes \( n = 1 \) and \( n = 2 \), both of which have complex \( k_{x_n} \)'s. Hence, this mode decays in depth and behaves as the fundamental propagating symmetric edge mode bound to the top surface of the ridge. The displacement field of this ridge mode, shown in Figure 7.5(a), resembles a surface wave. In fact, the propagation constant \( k_z \) is almost equal to the propagation constant of a \( z \)-directed surface wave. For the case of \( l = 2 \), the main contribution is from the fundamental anti-symmetric plate mode \( n = 3 \) which has a small but imaginary \( k_{x_3} \). Hence this can be called as the fundamental propagating anti-symmetric ridge mode. Its displacement field, as shown in Figure 7.5(b), resembles a flexural plate mode decaying in depth. Comparing the values of \( k_{x_1} \) and \( k_{x_2} \) with \( k_{x_3} \), it is seen that \( l = 2 \) decays much slower compared to \( l = 1 \). For a ridge waveguide standing on a substrate, in order to minimize reflections from the substrate, a higher aspect ratio \((h_{R}/w_{R})\) in Figure 7.1(c) should be used for the ridge carrying the anti-symmetric mode. If it is carrying the symmetric mode, then the aspect ratio need not be as large.
Figure 7.5 Displacement fields for the modes, (a) $l = 1$ and (b) $l = 2$ identified in Figure 7.4. $l = 1$ resembles a surface wave and $l = 2$ resembles a flexural plate mode slowly decaying in depth.

Particle velocity and stress fields within the cross-section for $l = 1$ and $l = 2$ are shown in Figure 7.6. In both cases, $T_2$, $T_4$ and $T_6$ should be zero on the sides walls in order to satisfy boundary conditions of the plate, and $T_1$, $T_5$ and $T_6$ should be zero on the top surface in order to satisfy boundary conditions of the ridge. In the present example, the values obtained for $k_{\text{real}}$ are found to be quite small compared to the width of the ridge. Thus, even though the boundary conditions were applied only at the center of the ridge,
they appear to be satisfied across the entire range of \( y \) on the top surface to a good extent.

Figure 7.6 Magnitudes of particle velocity and stress fields in the cross-section for the modes, (a) \( l = 1 \) and (b) \( l = 2 \) identified in Figure 7.4. The \( x \) and \( y \) dimensions are in microns. In both cases, \( T_2, T_4 \) and \( T_6 \) are zero on the sides walls, thus satisfying boundary conditions of the plate, and \( T_1, T_5 \) and \( T_6 \) are zero on the top surface, thus satisfying boundary conditions of the ridge.
The ridges modes found here can also be obtained using the general formulation as a single expansion constituting all 6 plate modes with boundary conditions applied at $y_0 = 0$ and $p = 0, 1$ (see Table 7.1). This results in a 6x6 square $A$ matrix whose determinant has zeros at the same values of $k_z$ as the ones found using the symmetric and anti-symmetric formulations. In addition to these ridge solutions, some spurious zeros are observed that correspond to values of $k_z$ where the plate modes become degenerate, which happens when the curves of Figure 7.3 intersect. Such false zeros not representing a solution to the ridge can be rejected by verifying the boundary conditions from field plots similar to Figure 7.6.

7.4 Numerical Results And Validation

7.4.1 Verification With ANSYS

Finite Element simulations were done in ANSYS to verify the calculated mode propagation velocities. In order to find the mode velocity in ANSYS, a modal analysis was performed for an anisotropic block of Silicon, as shown in Figure 7.7. The block acts as a resonator imitating a section of the ridge waveguide. It has length $l_R$ along the $z$-direction and the same width $w_R$ and orientation as the ridge waveguide described in Section 7.3.3. The idea is to identify and study the resonant modes that resemble standing wave patterns resulting from propagating modes on the ridge waveguide. The vertical size of the block $h_R$ in the $x$-direction is chosen by trial and error such that the top surface bound modes decay to an acceptable level in depth. Boundary conditions imposed on the block are summarized in (7.28). Additional boundary conditions for the symmetric and anti-symmetric cases are given in (7.29) and (7.30), respectively.
Figure 7.7 Geometry and coordinate system of an anisotropic block of Silicon simulated in ANSYS. The block imitates a resonating section of the ridge waveguide.

\[ v_x = 0 \text{ at } x = -h_R \]
\[ v_z = 0 \text{ at } z = -l_R / 2, l_R / 2 \]  
(7.28)

symmetric \( \rightarrow v_y = 0 \text{ at } y = 0 \) 
(7.29)

anti – symmetric \( \rightarrow v_x = v_z = 0 \text{ at } y = 0 \) 
anti – symmetric \( \rightarrow v_y = 0 \text{ at } y = 0 \text{ and } z = 0 \) 
(7.30)

Modes with half-wave resonance along \( z \) can be identified for the symmetric or anti-symmetric cases, as shown in Figure 7.8 and the resonant frequency \( f_R \) for each mode is recorded. The propagation velocity of the constituent travelling wave modes can be estimated as, \( c_R = 2l_R f_R \). This process is repeated for blocks of different lengths to obtain a dispersion curve over the frequency range of interest, as shown in Figure 7.9. Dispersion curves obtained in MATLAB by automatically tracking the \( l = 1 \) and \( l = 2 \) modes of Section 7.3.3 directly over \( \omega \), as described in Section 7.3.1, are also plotted. The ANSYS simulations and MATLAB computations match quite well within the frequency range of interest.
Figure 7.8 Results of modal analysis in ANSYS showing the standing wave pattern of the symmetric ridge mode on left and the anti-symmetric ridge mode on right. In both cases, the fields span half a wavelength along the length of the block. The color represents displacement in the $x$- and $y$-direction for the symmetric and anti-symmetric case, respectively. Entire blocks are not shown because their height’s are much larger than their length’s.
Figure 7.9 Comparison of modal dispersion curves obtained for the (a) symmetric and (b) anti-symmetric ridge modes shows good agreement between the ANSYS simulations and MATLAB computations.
7.4.2 Example Cases

Results for a ridge etched in Silicon with various crystal orientations are presented in this section. In order to give an intuitive visual idea of the effect orientation has on the plate modes inside an anisotropic crystal, a plot similar to Figure 7.2 is presented in Figure 7.10. In this plot, the determinant is shown only for the symmetric plate modes in the ‘folded’ $k_x - k_z$ plane, for a 2 micron wide plate oriented along various planes inside Silicon at 350 MHz. The dark lines correspond to the modal solutions. The behavior of the modes for the $<100>$ @ 0° and $<110>$ @ 90° orientations are similar along real $k_x$ and $k_z$ axes due to crystal symmetry. It should be noted that if the crystal was isotropic, then the dark lines would form quarter arcs of a circle in the right half plane for real values of $k_x$. For the $<111>$ @ 0° and $<111>$ @ 60° orientations, the modes seem to disappear when $k_z$ becomes imaginary. This is because the value of $k_z$ actually becomes complex in this region and is not purely imaginary or real. The full picture showing the evolution of the modes can only be obtained by looking at the complex $k_z$ plane, similar to the plot in Figure 7.3.

The complete solutions of the ridge were obtained for some of these cases and the results are presented next. Only the fundamental symmetric and anti-symmetric modes of the ridge are considered. Dispersion curves for the ridge etched in a $<100>$ Silicon wafer with $x$-axis along the $<100>$ crystal axis and $z$-axis along the $<001>$ crystal axis have already been presented in previous sections. Since the solutions only depend on the electrical dimensions of the ridge at a given frequency, the $x$-axis in the figures of this section has been generalized to the product of ridge width and frequency, having the units of velocity. Results for ridges aligned to the remaining symmetry planes of Silicon
(x-axis along the wafer surface normal) are shown in Figure 7.11. The cases correspond to orientations with z-axis at 45 degrees from the <001> crystal axis on a <100> Silicon wafer, with z-axis at 0 and 90 degrees from the <001> crystal axis on a <110> Silicon wafer and with z-axis along the <112> crystal axis on a <111> Silicon wafer. Varying numbers of plate modes and an appropriate set of ridge boundary conditions, as mentioned in Section 7.2.3, were used in each case to construct the ridge solutions. The anti-symmetric mode was found to be quite dispersive, whereas, the symmetric mode does not exhibit a strong frequency dependence. This can be explained in view of the similarity of the symmetric mode to a surface wave. For surface waves, the propagation velocities are independent of frequency. Plots of Figure 7.11 also show that the variations of the velocity with respect to the angle of the ridge appear to be larger in the case of symmetric modes, where the ridge aligns with a plane of symmetry of the crystal. This dependence can be further investigated by using the general formulation and performing a continuous sweep of the ridge angle.
Figure 7.10 Determinant showing the symmetric plate modes in the ‘folded’ \( k_x - k_z \) plane, for a 2 micron wide plate oriented along various planes inside Silicon at 350 MHz. The dark lines correspond to the modal solutions.
Figure 7.11 Modal dispersion curves obtained for the fundamental (a) symmetric and (b) anti-symmetric modes in a ridge waveguide oriented at various angles in a Silicon crystal. The velocity of the symmetric mode does not vary with frequency significantly, because this mode closely resembles the dispersionless surface wave.
Mode velocities as a function of ridge angle are presented in Figure 7.12 for a ridge width and frequency product of 700. This corresponds to the behavior of a 2 micron wide ridge at 350 MHz. Note that the symmetric and anti-symmetric are only meaningful when the ridge lies in a plane of mirror symmetry. For all intermediate angles, the ridge modes are formed by tracking the same plate modes used to construct the solutions at the symmetry planes, as a function of ridge angle. Therefore, these intermediate modes can only be classified as quasi-symmetric and quasi-anti-symmetric. A <100> Silicon wafer has 2 different mirror symmetry planes at 0 and 45 degrees from the <001> axis and rotation symmetry in 90 degrees, in the plane of the wafer. A <111> Silicon wafer has similar mirror symmetry planes at 0 and 60 degrees, but pointed in opposite directions, and a rotation symmetry in 120 degrees, in the plane of the wafer. Since the homogenous wave equation for uniform crystals gives the same mode velocity in the +z or –z direction, the plots are expected to be symmetric around 30 degrees for the <111> case. The plots of Figure 7.12 also confirm the stronger angular dependence of the quasi-symmetric mode (~4% variation vs. 1.5% for the quasi-anti-symmetric case). The dependence on angle is smaller for the ridge waveguides in <111> wafer and is limited to <2%. 
Figure 7.12 Mode behavior for the fundamental (a) quasi-symmetric \((l = 1)\) and (b) quasi-anti-symmetric \((l = 2)\) ridge modes as a function of scan angle between planes of mirror symmetry for different Silicon wafers. Variations in velocity are quite subtle, suggesting that anisotropy may not be a significant issue while designing ridge waveguides in Silicon.
7.5 Conclusion

A semi-analytical method for finding the approximate solution of the elastic equations in a ridge waveguide made of an anisotropic crystal was presented. The proposed formulation is general and leads to the propagating modes of the waveguide for the arbitrary orientation of the crystal and can be simplified to give symmetric and anti-symmetric modes when the ridge is parallel with a plane of crystal symmetry. Numerical issues involving the tracking of the plate modes were discussed. The method has been used for the modal analysis of deep ridges etched in Silicon. Some of these results have been verified by Finite Element simulations in ANSYS. For the case of Silicon, the modal behavior appears to be quite similar along various crystal orientations. Thus, it can be concluded that the effect of the anisotropy may be neglected in a first order analysis.
Chapter 8
MICROFABRICATION OF RIDGE WAVEGUIDE FILTER

8.1 Introduction

After the filter design was finalized to be based on the ridge waveguide, a way to fabricate the device was formulated. Based on this process flow, the layout was worked out and the masks were made. The final device cross section that was required to be fabricated is shown in Figure 8.1, and an illustrative 3-dimensional layout is shown in Figure 8.2. The figures also show the different materials and layers comprising the device. Note that the ridge widths are only 2 um wide. This makes the process extremely alignment critical requiring alignment accuracy of upto 1 um. Following sections explain in detail the layout of the filters, the process flow and the numerous challenges that were encountered during the fabrication.

![Figure 8.1 Cross-section of a filter die showing the various dimensions and layers of the device.](image-url)
Figure 8.2 An illustrative 3-dimensional layout of a filter die showing the various device layers and the electrical connections.

8.2 Layout

After planning the process flow for the current design, the layouts were generated for making the masks. Various designs of the filter have been included in the layout. The designs vary in terms of the number of acoustic waveguides, electrodes, filter tuning frequency and airgap distance. It should be noted that at this stage the filters are not designed to be tunable in order to avoid any complications arising from the tuning interface circuitry. Some of the filters included have only 2 waveguides. These are for testing the matching characteristics using a series inductor. In addition to the filters, some resonator designs are included to study their frequency response and to compare it with simulations. These resonators are essentially arrays of blocks similar to the one shown in Figure 7.7. In order to calibrate the acoustic waveguide for its characteristic
impedance, some layouts similar to a Thru-Reflect-Line (TRL) measurement setup have been included. A comprehensive list of all the designs included on the wafer is given in Table 8.1, Table 8.2 and Table 8.3.

<table>
<thead>
<tr>
<th>Design #</th>
<th>Total Ridges (M)</th>
<th>Total Electrodes on each side (N)</th>
<th>Airgap (nm)</th>
<th>Tuned frequency (MHz)</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
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</table>

Table 8.1 List of filter designs included on the wafer.
<table>
<thead>
<tr>
<th>Design #</th>
<th>Total Ridges (M)</th>
<th>Total Electrodes on each side (N)</th>
<th>Airgap (nm)</th>
<th>Tuned frequency (MHz)</th>
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<td>2</td>
<td>250</td>
<td>100</td>
<td>430</td>
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</table>

Table 8.2 List of filter designs to be used with a series inductor that were included on the wafer.

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<tr>
<th>Design #</th>
<th>Block width (um)</th>
<th>Block length (um)</th>
<th>Excitation</th>
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<td>Symmetric</td>
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</table>

Table 8.3 List of resonator designs included on the wafer.
Table 8.4 Resonant frequencies of the resonator designs listed in Table 8.3.

<table>
<thead>
<tr>
<th>Set</th>
<th>28 sym, 28 asym</th>
<th>216 sym, 216 asym</th>
<th>48 sym, 48 asym</th>
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<tr>
<td>1</td>
<td>6.9746E+07</td>
<td>1.1430E+07</td>
<td>6.9802E+07</td>
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<td>3</td>
<td>3.1527E+08</td>
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<td>3.7697E+08</td>
<td>2.8854E+08</td>
<td>3.7697E+08</td>
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<tr>
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<td>4.5099E+08</td>
<td>3.1575E+08</td>
<td>4.5101E+08</td>
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<td>3.4313E+08</td>
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<td>3.7555E+08</td>
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<td>9</td>
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<td>12</td>
<td>5.4246E+08</td>
<td>4.7765E+08</td>
<td>5.3779E+08</td>
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<td>13</td>
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<td>4.9382E+08</td>
<td>5.4292E+08</td>
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<td>14</td>
<td>5.4651E+08</td>
<td>5.3721E+08</td>
<td>5.4723E+08</td>
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<tr>
<td>15</td>
<td>5.5094E+08</td>
<td>5.4079E+08</td>
<td>5.4943E+08</td>
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<td>16</td>
<td>5.5806E+08</td>
<td>5.4535E+08</td>
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<td>5.9492E+08</td>
<td>5.9116E+08</td>
<td>5.9380E+08</td>
</tr>
</tbody>
</table>

The 4 inch wafers have a total of 120 chips in the upper half of the wafer. The wafer is divided into 3 zones with equal number of chips. Every chip design has 3 copies on the wafer, one in each zone, as shown in Figure 8.3. This ensures that the various designs have a fair chance in the wake of radial variations in the process parameters, across the wafer. Each Chip has a code etched in the metal layer at the top and bottom to identify what design it is. The code at the bottom has the format [Chip # – Design # – Zone#] and can be used to identify the design using the tables given in this section. The code at the top directly gives the parameters used in that filter in the format, [M – N – Airgap – Tuned frequency]. In summary, there are 30 filter designs occupying 30 dies, 12 series matching filter designs occupying 4 dies, 6 resonator designs occupying 2 dies and 4 TRL calibration dies occupying 4 dies, giving a total of 40 dies in each zone.
Figure 8.3 Placement of all the designs listed in the previous tables, showing the chip numbers and die numbers. Die numbers are nothing but cumulative design numbers. Note that 3 series matching filters and 3 resonators could be fitted onto one die. The 3 zones are also shown in different colors.

The overall top view of a typical filter die is shown in Figure 8.4, along with some dimensions of the die. It should be noted that the trenches separating adjacent ridges are 2 um wide, whereas the ones separating the pads and adjacent dies were set to be 50 um wide in order to increase electrical isolation. There are 6 masks in the process flow, as shown in Figure 8.5 for a single filter die. The complete process flow is explained in another section. Figure 8.6 shows a stack of the 6 layer mask for a die comprising of 3 series matching filters, a die comprising of 3 resonators, a die of a TRL calibration chip and a module of alignment marks. Alignment mark modules also have
some test structures which can be cleaved out to monitor the process flow in an electron microscope without destroying the actual devices. The complete masks with all the 120 dies are shown in Figure 8.7. The planned process flow requires 6 masks, 4 of them are high resolution and 2 are low resolution. One of them is a clearfield mask and 2 are darkfield masks. There are over 10 million rectangles in the complete layout. So it is not feasible to manually draw these masks. An automatic layout generator was written in MATLAB for generating these layouts as a CIF file which was later converted to GDSII using the commercial software called LayoutEditor. This automation also allows for quick changes to any filter design on the wafer. These layouts were taped out to Photosciences Inc. for making chrome on glass masks.

Figure 8.4 Typical die on the wafer (not to scale). Gray regions are the ridges/pads and white regions are the 30 um deep trenches. The region with 2 um wide trenches that were completely refilled during the trench refill process are at the center of the die. The 50 um wide trenches that did not get completely refilled are also shown.
Figure 8.5 The 6 different mask layers for a typical filter die.

Figure 8.6 Typical layout of the dies for series matching filters, resonators and a TRL calibration chip. A sample of the vast armada of alignment mark modules is also shown. The alignment marks are of various sizes and the module also includes sample test structures that can be used for SEM imaging of the process flow without destroying the actual filter dies.
Figure 8.7 A large scale picture of the complete layout of the masks showing all the 120 dies. There are 2 high resolution and 1 low resolution mask plates, each with 2 mask layers. Masks 1 and 5 are clearfield, whereas, masks 2, 3, 4, 6 are darkfield.
8.3 Process Flow

The devices are fabricated on 4" double side polished, high resistivity SOI wafers or silicon wafers. High resistivity helps for DC decoupling. SOI wafers with a 30 um device layer have a resistivity of 1000 ohm-cm. It was decided to use SOI wafers as a main substrate because the buried oxide layer helps to prevent electrical leakage through the substrate and also acts as an etch stop during DRIE. The silicon wafers have a resistivity of around 100 ohm-cm and were used for characterization purposes only. The wafers were first rinsed with acetone, methanol and IPA, followed by a Piranha clean to remove any organic contaminants. An RCA clean was also done to remove any inorganic contaminants. The cross section of the SOI wafers used is shown below. The buried oxide layer is not shown in the illustrations presented in the following sections.

![High resistivity Silicon device layer (30 um) Buried oxide layer (1 um) Silicon handle (500 um)](4" 500 um thick SOI wafer)

The layout has many small critical patterns all over the wafer. Tiny bubbles in the spin coated resist can comprise the performance of an entire chip by causing shorting. Hence, it was recommended to use a well settled bottle of photoresist with no bubbles. The basic photolithography steps are understood, but for the sake of completion they are listed below. Details of the intermediate photolithography steps for each process step are not illustrated in the following sections.
- Spin photoresist
- Soft bake photoresist
- Align mask and expose (EVG620)
- Develop photoresist (AZ300 MIF)
- Hard bake photoresist
- **Perform process step**
- Strip photoresist (acetone, asher, nanoremove, piranha etc)

Description of every process step starts with an illustration showing what that process step achieves. Various color codes are used to depict the different layers. The legend below shows what each color represents. Note that the illustrations are not to scale.

Table 8.5 lists all the masks used in the process flow for reference and, Table 8.6 summarizes all the process steps with process details and the tools used.

![Legend of Colors](image)

<table>
<thead>
<tr>
<th>MASK #</th>
<th>Code</th>
<th>Type</th>
<th>Resolution</th>
<th>For Photoresist</th>
<th>Purpose</th>
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<td>Clearfield</td>
<td>High</td>
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<td>Doping</td>
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<td>63B</td>
<td>Darkfield</td>
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<td>AZ3312 (+ve PR)</td>
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<td>24B</td>
<td>Darkfield</td>
<td>Low</td>
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<td>Amorphous Si 1</td>
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<tr>
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<td>High</td>
<td>AZ5214 (Image reversal)</td>
<td>Metal</td>
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Table 8.5 List of all the masks used with their properties and application.
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<th>Process details</th>
<th>Mask</th>
<th>Facilities/Tools</th>
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<tr>
<td>1</td>
<td>spin photoresist (AZ3312 – 1 um) photo (topside)</td>
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<td>EVG620 Aligner RIE Floey (CF₄/O₂)</td>
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<td><strong>RIE silicon</strong> – 1 um (backside of wafer) strip photoresist</td>
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<td>spin photoresist (AZ4330 – 2.7 um) photo (bottomside)</td>
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<td>EVG620 Aligner CSSER ASE</td>
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<td><strong>Deep RIE silicon</strong> - 30 um strip photoresist</td>
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<td>RCA clean</td>
<td>-</td>
<td>CSSER Furnaces</td>
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<td></td>
<td><strong>Thermal oxide</strong> - 100 nm</td>
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<td></td>
<td><strong>LPCVD polysilicon</strong> – 2 um (trench refill)</td>
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<td></td>
</tr>
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<td><strong>Chemical Mechanical Planarization</strong> - 2 um</td>
<td>-</td>
<td>University of Arizona</td>
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<td>spin photoresist (AZ4330 – 2.7 um) photo (bottomside)</td>
<td>Mask 2</td>
<td>Innovion Inc.</td>
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<td><strong>Boron Ion Implantion</strong> – 0.2 um Piranha clean (3:1 at 100 C for 10 mins)</td>
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<td>spin photoresist (AZ3312 – 1 um) photo (bottomside)</td>
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<tr>
<td></td>
<td><strong>RIE oxide</strong> – 100 um Piranha clean (3:1 at 100 C for 10 mins)</td>
<td></td>
<td>CSSER Furnaces EVG620 Aligner RIE Floey (CF₄/O₂)</td>
</tr>
<tr>
<td>7</td>
<td>RCA clean</td>
<td>Mask 4</td>
<td>CSSER Furnaces EvG620 Aligner RIE Floey (CF₄/O₂)</td>
</tr>
<tr>
<td></td>
<td><strong>LPCVD amorphous silicon</strong> - 50 nm spin photoresist (AZ3312 – 1 um) photo</td>
<td></td>
<td>CSSER Furnaces EvG620 Aligner RIE Floey (CF₄/O₂)</td>
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<tr>
<td></td>
<td>(bottomside)</td>
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<td>CSSER Furnaces EvG620 Aligner RIE Floey (CF₄/O₂)</td>
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<tr>
<td></td>
<td><strong>RIE polysilicon</strong> – 50 nm Piranha clean (3:1 at 100 C for 10 mins)</td>
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<td>CSSER Furnaces EvG620 Aligner RIE Floey (CF₄/O₂)</td>
</tr>
<tr>
<td>8</td>
<td>RCA clean</td>
<td>Mask 5</td>
<td>CSSER Furnaces EvG620 Aligner RIE Floey (CF₄/O₂)</td>
</tr>
<tr>
<td></td>
<td><strong>LPCVD amorphous silicon</strong> - 50 nm spin photoresist (AZ3312 – 1 um) photo</td>
<td></td>
<td>CSSER Furnaces EvG620 Aligner RIE Floey (CF₄/O₂)</td>
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<td>CSSER Furnaces EvG620 Aligner RIE Floey (CF₄/O₂)</td>
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<td></td>
<td><strong>RIE polysilicon</strong> – 50 nm Piranha clean (3:1 at 100 C for 10 mins)</td>
<td></td>
<td>CSSER Furnaces EvG620 Aligner RIE Floey (CF₄/O₂)</td>
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<tr>
<td>9</td>
<td><strong>E-beam evaporate Aluminum</strong> – 1 um spin photoresist (AZ5214 – 1.3 um) photo</td>
<td>Mask 6</td>
<td>CHA1 EvG620 Aligner RIE Cloey (BCl₃)</td>
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<td></td>
<td>(bottomside)</td>
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<td></td>
<td><strong>RIE Aluminum</strong> – 1 um strip photoresist (No Piranha clean)</td>
<td></td>
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<tr>
<td>10</td>
<td><strong>XeF₂ polysilicon release</strong></td>
<td>-</td>
<td>Xactix XeF₂ etcher</td>
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Table 8.6 Summary of all the process steps showing all the steps involved with their process details, the masks used and the tools used.
8.3.1 Bottomside Alignment Marks

Due to the need for highly accurate alignment to within 1 um, all the masks are aligned to a pattern on the bottom of the wafers for consistency. Bottomside alignment also helps to avoid any alignment mark wear out during CMP or other process steps. It also eliminates the problems caused by mark visibility when using a dark field mask. All wafers used in the process flow are double side polished to aid in bottomside alignment. Positive photoresist AZ3312 is spun on the back of the wafer to give a thickness of 1 um. Photolithography was done using mask 5 (any of the high resolution masks could have been used) by topside alignment. Silicon on the backside was etched to 1 um using a Fluorine based plasma etch. Finally, the photoresist was stripped using acetone and ash. An cross-sectional illustration showing the bottomside marks is shown above. These marks will be omitted from subsequent process step illustrations.
Ridges are etched in silicon by Deep RIE to define the acoustic waveguide structures and the pads. Photoresist AZ4330 is spun on the topside and the pattern is defined with high resolution mask 1 using bottomside alignment. Thickness of the resist is around 2.7 um, which is thick enough to survive the entire DRIE process designed to etch 30 um deep trenches. In case of the SOI wafer, the buried oxide layer acts as an etch stop. Finally, the resist is stripped using acetone and asher. Two types of trenches are etched in this process – narrower 2 um wide trenches between adjacent ridges and wider 50 um wide ridges between pads and adjacent dies to increase electrical isolation. Figure 8.8 shows a photo of the etched dies and Figure 8.9 shows SEM images of the etched trenches in a test sample. The images clearly show the parallel ridge acoustic waveguides, bias pads and alignment marks. The ‘RIE grass’ present in the test sample was not present in the actual wafers. It can be seen that the ridge walls are not exactly vertical and have a slight taper. Undulating sidewalls resulting alternating DRIE steps can be clearly seen.
Figure 8.8 Images of regions on the 4 inch silicon wafer showing the etched device dies.

Figure 8.9 SEM image of the ridge acoustic waveguide fabricated using Deep RIE. Width of each ridge is around 2 μm. The spikes seen in the leftmost image are called as ‘RIE grass’ thought to be caused by micro-masking during the DRIE step and can be removed by tweaking the etch recipe. These are only present in the imaged test samples. Bias pads can be seen in the lower left image. Alignment marks and test structures can be seen in the lower right image.
8.3.3 Trench Refill

The next step involves a trench refill process to fill up all the trenches between the ridges and the pads and dies, so that metal electrodes can be built on top of these ridges. Before putting the wafers inside the furnace, an RCA clean is done to remove any inorganic contaminants. A 100-120 nm thick layer of thermal oxide is grown to protect the silicon ridges. This is followed by a trench refill with 2 um thick LPCVD polysilicon. In this refill process, only the 2 um wide trenches are completely filled and leveled, whereas, the 50 um wide trenches are still wide open. An SEM image showing the trench refilled test sample is shown in Figure 8.10. The 50 um wide unfilled trench can be clearly seen in the images. High resolution SEM shows the thin oxide layer enveloping the silicon ridges. LPCVD has very good step coverage and can cause voids in a trench refill process known as ‘keyholes’. Some of these voids are visible in the SEM images.
Figure 8.10 SEM images showing the ridges after thermal oxidation and trench refill by LPCVD polysilicon. In the bottom left image, the white region outlining the silicon ridges is the 120 nm thick thermal oxide. Small ‘keyholes’ can also be seen in the refilled trenches on the bottom left. A 2 um wide alignment cross covered in polysilicon ‘snow’ can be seen in the bottom right image.

8.3.4 Chemical Mechanical Planarization

Chemical Mechanical Planarization – 2 um
The trench refill process completely covers the silicon ridges. In order to gain access to these ridges, the LPCVD films must be polished down to the oxide layer. This is achieved by a chemical mechanical planarization (CMP) step which exposes the silicon and also makes the surfaces flat for subsequent process steps. This step was performed by the staff at University of Arizona using their CMP tool. The polishing removed around a 2 um thick layer to expose the tops of the silicon ridges. This is evident from the profilometer plots shown in Figure 8.11. Due to the presence of wide and deep trenches, the edges and corners of the pads have been rubbed off creating a concave depression which is about 1-2 um deep.

Figure 8.11 The CMP step was done at the University of Arizona. Top right profilometer plot shows the removed oxide and polysilicon layer. Lower left plot shows the concave dents in the edges and corners of the pads caused by uneven topography. The 30 um height of the pads can be seen in the lower right plot.
The wafers used in this process flow were intentionally chosen to have high resistivity so that the conductive regions on the device could be controlled by doping the right regions to make the top surfaces highly conductive. Highest concentration of the dopants was required nearest to the surface to reduce the sheet resistance. So it was essential to control the depth profile of the dopants. This is why the doping was done using ion implantation rather than diffusion because the dopant depth is independent of dopant concentration in the case of ion implantation. The dopant chosen was Boron and the projected range was set to 0.2 um. The ion implantation step was carried out at a company called Innovion Inc. Dopant concentration and projected ranges are given in Figure 8.12.
Figure 8.12 Dopant concentration and the resulting resistivity is shown in the figure on top. Projected ranges and ion energies are shown in the lower figure, which has been borrowed from the Innovion website.

The doping step also created an undoped region that provided the right resistance for emulating an RF choke. Length of this undoped region was determined from the parasitic simulations in Section 6.3.3. This also helped to determine the right dopant concentration. The undoped region does not cause any reduction in the DC bias voltage.
drops, because the transducers are essentially open circuits and therefore there is no DC current flowing in the bias rails. Another reason why ion implantation was chosen over diffusion was because in later steps, the wafers will anyway go through a number of high temperature furnace processes which can cause further dopant diffusion, closing in on this undoped gap that was meant to provide the RF blocking resistance.

A photoresist mask was used for the ion implantation process. AZ4330 is spun to give a 2.7 um thickness. This thickness was chosen so as to not cause any penetration into the undoped regions during the implantation process. The resist is patterned using mask 2, a low resolution mask, which is aligned by bottomside alignment. Spinning the photoresist was a challenge because the wafers now had trenches that were 30 um deep and 50 um wide. The resist film was extremely non-uniform and resulted in uneven developing across the wafer. Fortunately, mask 2 was a low resolution mask with large linewidths and the patterns were away from the edges of the elevated areas, so it was easy to work around the recommended recipe to obtain an acceptable photoresist pattern. Again, after the process, stripping of the photoresist was now another challenge. The hard baked resist with unequal thickness did not come off easily with acetone or ashing. Thick resist clogged in the trenches would contaminate the elevated pads with shattered pieces of photoresist. It was not easy to remove these contaminants. Finally, when all approaches failed, a 3:1 Piranha clean at 100 C for 10 minutes was done to wipe out the hard baked resist.
During the CMP step, the tops of the silicon ridges were exposed. To protect them, another high quality thermal oxide layer was grown to a thickness of 100 nm. This layer also acts as the electrode anchor and forms the MIM capacitors between the ridges and the electrodes. An RCA clean was done to remove any inorganic contaminants before putting the wafers in the furnace.

After growing the oxide, it had to be etched in certain regions to expose the refilled polysilicon trenches that would later be removed in the release step. The mask used for this step was a high resolution mask and needed a uniform coating of photoresist to work properly. It also had critical patterns near the edges of elevated areas. As mentioned earlier, spinning photoresist on this patterned wafer would now produce a highly non-uniform film which was especially thin near the edges of elevated areas. An important job of the oxide layer is to protect the silicon ridges underneath during the final release step. If the mask pattern is disfigured, then the entire device is compromised.
So, a significant amount of time was spent in researching ways to obtain a better film quality before proceeding with the photolithography for this step. A discussion of all these methods is given in Section 8.4.1. Unfortunately, the wafer had too many variations in surface topography and the photolithography requirements were very stringent, so none of the methods tried gave satisfactory results. Finally, a decision was made to optimize the spin coating recipe as much as possible and work with it.

After a number of trial and errors, some tweaks were made to the photoresist spin coating recipe. Primarily, the develop times had to be increased to two and half times the recommended values. AZ3312 was spun over the wafer to achieve an expected thickness of 1 um. It was patterned using mask 3 with bottomside alignment. Oxide was etched using a Flourine based plasma etch. Again, like in the previous step, the resist had to be removed by a hot Piranha clean.

Due to the thinner film thickness near the edges, these areas can get over developed, thus completely wiping out the patterns in these regions. All the oxide in these regions can get etched. This has the potential to etch away all the exposed silicon ridges underneath in the release step and it can also cause shorting of metal electrodes in subsequent steps. Apart from the problems caused by uneven topography of the wafer, another issue can be caused by the small linewidths present on the mask. This mask had many lines that were 1 um wide creating regions of photoresist with a gap of 1 um. These narrow gaps can easily close in due to the flow of resist. This can lead to many regions where no oxide windows opened up for polysilicon release or biasing, thereby significantly compromising the device structure and function. More details about this issue are discussed in Section 8.4.3.
Transducers in this filter have a narrow airgap in between the capacitor plates. There are two types of designs in this layout with airgap thickness of 50 nm and 100 nm. To obtain both types of airgaps, 2 layers of a sacrificial layer were successively deposited and patterned. This step corresponds to the first layer. A 50 nm thick high quality sacrificial LPCVD layer of amorphous silicon was deposited on top to define these air gaps. An RCA clean was done to remove any inorganic contaminants before putting the wafers in the furnace. Amorphous silicon was chosen over polysilicon because it has a slower deposition rate of about 2 nm/min, which reduces the grain size and gives a more uniform film. The roughness of a sample LPCVD film of polysilicon can be seen in Figure 8.10. This layer was later patterned using mask 4 by bottomside alignment. AZ3312 was spin coated with an expected thickness of 1 um. Amorphous silicon was etched using a Flourine based plasma etch. The designs that had only a 50 nm airgap were exposed to etch away the sacrificial layer deposited in this step. Again, the resist was removed by a hot Piranha clean.
This step deposits the second layer of the sacrificial material as described in the previous step. Another 50 nm thick high quality sacrificial LPCVD layer of amorphous silicon was deposited on top of the previous layer. An RCA clean was done to remove any inorganic contaminants before putting the wafers in the furnace. Designs whose first sacrificial film was etched away in the previous step would now have only a 50 nm layer of the second sacrificial layer, whereas the other designs would now have a stack of 2 films totaling a thickness of 100 nm of sacrificial layer. This layer was patterned using mask 5 by bottomside alignment. AZ3312 was spin coated with an expected thickness of 1 um. Amorphous silicon was etched using a Flourine based plasma etch. The resist was removed by a hot Piranha clean. Photographs of the wafer after this stage are shown in Figure 8.13. The entire array of 120 dies can be seen in these images. Multicolored regions arise due to the thin films deposited in the previous process steps. Figure 8.14 shows the images of the patterns through an optical microscope. Pads, ridges, trenches and amorphous silicon patterns can be seen in these images.
Figure 8.13 Photographs of the wafer after this process step before depositing any metals. Various types of dies and alignment marks can be clearly seen on the wafer surface. The multicolored regions are caused by the various thin films deposited in the previous process steps.
Figure 8.14 A view of the patterns through an optical microscope. Trench refilled areas with ridges. 50 um wide trenches, Bias pads and checkered patterns of amorphous silicon can be seen in these images. Denting around the edges of the pads caused by CMP can also be seen. The ‘broken’ patterns on the pads are a result of the problems encountered during photolithography due to the uneven wafer topography.
8.3.9 Metal Deposition

The metal layer is an important layer and defines the electrode bridges and contacts. This mask also has the chip design numbers and other details at the top and bottom of each die. A 1 um thick layer of Aluminum was e-beam evaporated onto the wafer surface. The decision to use Aluminum was arrived at after considering other metals, as discussed in Section 8.4.4. Originally, another metal was planned to be deposited by electroplating and the mask was designed accordingly. Since the process was modified to a deposit and etch step, the same mask was used with an image reversal resist. This resist acts like a negative photoresist, but has positive sloped sidewalls and is less hazardous. The image reversal photoresist AZ5214 was spin coated to an expected thickness of 1.3 um. It was patterned using mask 6 by bottomside alignment. Aluminum was etched using a Chlorine based plasma etch which had an etch rate of 50 nm/min. The etching of Aluminum could not be verified by a continuity test using a multimeter. This was because evaporation is a directional process and due to the presence of deep
trenches, the Aluminum film was not continuous and had many breaks along the edges of the pads.

The mask used is a high resolution mask and also suffers from the narrow linewidth problem discussed earlier for mask 3. There is a gap of only 1.5 um between the electrodes. If this gap closes in, then no electrode patterns are defined and electrodes are essentially shorted, making the device unusable. After the etch process, the photoresist was stripped using acetone and ashing. Piranha clean could not be used as in the earlier steps because Piranha solution reacts violently with Aluminum. This causes a lot of the thick hard baked photoresist to remain on the wafer and inside the trenches. The main problem is caused by microscopic flakes of resist from the trenches that contaminate the surface of the devices. Since the metal film was quite thick at 1 um, it was peeled off in many regions due to stress.

8.3.10 Release

Release using XeF\textsubscript{2} polysilicon & amorphous silicon dry etch

The final step involves a dry etch of all the refilled polysilicon and sacrificial amorphous silicon layers using XeF\textsubscript{2}. Figure 8.15 shows SEM images of the devices after the release. Due to the problems arising in the metal deposition step and the ones
mentioned earlier, the patterns in these images are not clearly visible. Peeling of metal films, ridges, shorted metal electrodes can all be seen in these images.

Figure 8.15 SEM images of the devices after release using XeF$_2$. In the upper left image, it can be seen that all the metal electrodes are shorted. Peeled metal films can be seen in the upper right image. Die identification numbers etched in the metal layer can be seen in the lower left image. In the lower right image, ridges surrounded by polysilicon are still visible, indicating that the release step did not succeed.
8.4 Challenges

A number of challenges were encountered during the entire process flow. Overall the fabrication did not succeed with the expected accuracy and the condition of the final fabricated devices was not within acceptable tolerance levels so they could not be tested. Apart from the issues discussed in the subsequent sections, other concerns were:

- Presence of tiny bubbles in the spin coated resist that could comprise the performance of an entire chip by distorting the etched patterns causing shorting of the metal electrodes. These bubbles could be avoided by using a clean well settled bottle of photoresist.

- The differential design has many elements of opposite polarity right next to each other. Hence, alignment was a very critical step in the photolithography process. Bottomside alignment did help a lot in obtaining accurate alignments, but there was still some error on the order of 1 um.
8.4.1 Photolithography On A Patterned Surface

The wafers are covered in trenches that are 30 μm deep and 50 μm wide. Trench refill did not fill up these wide trenches. Ideally the trench refill process should have resulted in a wafer as shown below, in which case, the problems would have been greatly reduced.

![Ideal trench refill](image)

The uneven topography causes a spin coated photoresist film to have an extremely non-uniform thickness that is thinner near the edges of elevated areas due to surface tension. This problem is present in all process steps after CMP. Figure 8.16 shows SEM images of the spin coated photoresist AZ3312 on a test wafer with wide trenches. A tapering film thickness profile near the edges of elevated areas can be clearly seen in these images. Extensive fringing is visible to the naked eye due to the non-uniform film and the measured thickness varies from 0.1 μm to 4 μm. Unequal film thickness causes over-developing in some areas and under-developing in others, which results in an undesired pattern. Especially, the silicon ridges near the edges can be exposed to the release step, causing them to disappear completely or to short the deposited metal electrodes. Also, some masks have linewidths as small as 1 μm. The thick hard baked resist is also difficult to strip using regular methods. A hot Piranha clean is required to remove the stubborn resist whenever possible. Apart from the resist on the surface, the thick resist also clogs the trenches and gives rise to ‘flakes’ or shattered pieces of resist that contaminate the device regions.
Figure 8.16 SEM images of AZ3312 spin coated on a test wafer with wide trenches. The dark tar-like material is the photoresist. Thinning of the film near the edges of elevated areas can be clearly seen in these images.

After some researching, a number of methods were found that could be used on wafers with rough topography. Some of these methods are listed below.

- Dry film photoresist
- Electrodeposition of photoresist
- Surface planarization process using Futurrex planarizing coatings
- Refill trenches with some polymer and etch back
- Use thinner to reduce photoresist viscosity
- Spray coating (spray coater or artist's air brush)
- Refill trenches by spin coating photoresist at slow rpm and etch back
• Refill trenches with PMMA and etch back

Some of these processes are expensive and require specialized tools and chemicals. So only a few of these could be tried. Refill using by spin coating with reduced rpm did not really yield any useful results. Spray coating was tried using a spray coater at the Flexible Display Center. The spray coating process was optimized for AZ1505 and the results are shown in Figure 8.17. The step coverage of the film is still not good and the film tapers significantly near the edges. Visually, the film still had a lot of fringing indicting variations in film thickness. Though these are slightly better than spin coating, they still do not yield an acceptable film quality.

Figure 8.17 Spray coating of photoresist AZ1505 on a test wafer with wide trenches. Still there is a significant amount of thinning near the edges.
Another method was tried to fill the trenches using PMMA. The plan was to spin coat PMMA at low rpm, hard bake and then etch back using RIE. The photoresist film was then deposited on this ‘planarized’ wafer. Unfortunately, the photoresist film was still quite non-uniform and exhibited a lot of fringing. This meant that the PMMA was unsuccessful in filling the trenches completely. The removal of this hard baked film made of photoresist and PMMA was a big challenge. This is discussed in more detail in the next section.

8.4.2 Removal Of PMMA

As mentioned previously, the removal of hard baked PMMA and photoresist film posed a major challenge in itself. The PMMA was hard baked at 170 C for 2 mins. The film did not yield to any of the methods listed below.

- Microstrip 2001 at 70 C for 1 hour
- Asher at 200W for 4 hours
- Piranha clean at 100 C for 3 hours
- AZ 300MIF developer for 1 hour
- Acetone at ambient for 1 day
- Acetone at 50 C in Ultrasonic bath for 3 hours
- Nano-remover PG at 80 C for 3 hours
- Nano-remover PG at ambient for 4 days
- Nano-remover PG at 50 C in Ultrasonic bath for 1 hour

After all these steps, the film appeared like a shattered piece of glass and the thickness was around 0.01-0.1 um. Finally, a Fluorine based dry etch with CF$_4$+O$_2$ was able to
etch away a substantial amount of the film. This hard baked film was sitting on top of a 100 nm thermal oxide layer. Some oxide was sacrificed in the process but the timing was short enough so the oxide loss was within acceptable levels. Unfortunately, the Fluorine dry etch was still not able to etch a final 5-10 nm of the residue, as shown in Figure 8.18. The dry etch could not be continued for a longer time, because the Fluorine could have attacked the silicon if there were any holes in the oxide layer. Finally, an oxide wet etch using BOE was done to etch away the underlying oxide film to completely remove the remaining residue. The 100 nm thermal oxide had to be regrown after this step.

Figure 8.18 The shattered hard baked PMMA & photoresist film can be seen in the top left figure. After a Fluorine dry etch, a significant amount of the film was gone, but there was still a 5-10 nm of residue remaining on the oxide layer as seen in the lower figures. This was later removed by etching away the underlying oxide film.
8.4.3 Narrow Linewidths

The smallest linewidths on masks 3 and 6 were too small on the order of 1-1.5 um, thus pushing the limits of photolithography. These masks were especially critical in defining windows for release, windows for bias patterns and metal electrodes. If these gaps are closed, then the trenches cannot be etched, electrodes cannot be correctly biased and the electrodes can get shorted. In order to give an idea of the resolution of the photolithography process, some images are shown next. Figure 8.19 shows the actual mask pattern and an optical microscope image of the actual patterned sacrificial layer. The green region corresponds to amorphous silicon and the pink is oxide. The pink gaps between the checkered patterns of amorphous silicon were supposed to be rectangles of size 4 um x 5 um. It can be seen that these gaps have been heavily rounded. Figure 8.20 shows a mask pattern and SEM images of the actual corresponding pattern of the 1 um thick spray coated film of photoresist AZ1505 developed using the inverted mask 6. The diamond shaped gaps between the resist were supposed to be rectangles of size 2 um x 4 um. The squares have been distorted into a diamond with rounded corners. Also, in the lower half, there should have been 1.5 um wide strips of resist, but these did not develop. From these images, it can be expected that if the gap was 1 um wide, then there was a very chance that it would have been closed. The problem is compounded by the fact that, in many of the later process steps, the photoresist film is highly non-uniform and can be quite thick in some regions.
Figure 8.19 The mask pattern is shown on the left and an optical microscope image of the actual patterned sacrificial layer is shown on the right. Green region is amorphous silicon and the pink region is oxide. The pink gaps are supposed to be rectangles of size 4 um x 5 um.

Figure 8.20 The mask pattern is shown at the top and SEM images of the actual corresponding pattern are shown at the bottom. The pattern is developed in a AZ1505 spray coated film having a thickness of 1 um. Diamond shaped gaps between the resist were supposed to be rectangles of size 2 um x 4 um. In the lower half of the left image, there should have been 1.5 um strips of resist that are missing.
8.4.4 Metal Deposition

Choosing the right metal was a challenge because of availability issues. Though not the best choice, Aluminum was chosen because it was readily available. Several other metals were considered before Aluminum was selected. Gold and Titanium are attacked by XeF$_2$, so they could not be used. The etchants and etch rate data for various metals were obtained from [36].

**Nickel** - Originally, Nickel was to be deposited using the following process flow and the metal mask was made for Nickel. Unfortunately, there was no Nickel electroplating solution available in the lab at the time, so Nickel could not be deposited.

- Sputter Titanium adhesion layer – 50 nm
- Sputter Nickel seed – 50 nm
- Spin photoresist AZ3312 – 1 um
- Photo (bottomside)
- Electroplate Nickel – 1 um
- Wet etch Nickel (no RIE recipe for Nickel)
- RIE Cloey Titanium

**Copper** - Since the metal mask was designed for electroplating, the only other metal that could be electroplated at the time was Copper. Lift-off was not possible with the available mask because positive photoresist has positive sloped sidewalls and secondly, the linewidths were too small. The below listed procedure was followed for depositing Copper. Evaporators could not be used for depositing the seed layer because they are directional and have poor step coverage. Hence, the seed layer was grown by sputtering (Courtesy: Prof. Junseok Chae). The result of electroplating was not as expected.
because the electroplating was occurring quite non-uniformly across the wafer in spite of using meshed electrodes. The film quality was also very rough. The Copper electroplating solution was probably contaminated. Also, due to the deep trenches in the wafer, the seed layer may have had a lot of cracks along the edges of the pads, thus making the seed film discontinuous.

- Sputter Chromium adhesion layer
- Sputter Copper seed – 100 nm
- Spin photoresist AZ3312 – 1 um
- Photo (bottomside)
- Electroplate Copper – 1 um (deposition rate - 0.5 um/min for 1 A current)
- Piranha clean for photoresist and Copper seed (no RIE recipe for Copper)
- $\text{H}_2\text{O}_2$ or RIE Cloey etch to remove Chromium adhesion layer

**Chromium** – Ideally, Chromium would have been the best choice from a mechanical and fabrication point of view. Chromium is more elastic than Nickel. The Young's modulus for Chromium is 280 GPa compared to 200 GPa for Nickel. Velocity of sound is around 6000 m/s compared to 5000 m/s for Nickel. The simple deposit and etch procedure outlined below, similar to the one followed for Aluminum, could have been followed for Chromium. Unfortunately, Chromium pellets were not available at the time for evaporation.

- E-beam evaporate Chromium – 1 um
- Spin photoresist AZ5214 – 1.3 um
- Photo (bottomside)
- RIE Cloey Chromium – 1 um
- Piranha clean
Chapter 9

CONCLUSION

A MEMS based tunable RF filter was discussed in this dissertation. The design equations were derived and the design process was illustrated with examples. For an example design with finite width membrane waveguide, simulation results were presented and compared to the theoretical models. It was observed that, at least for this simple case, substrate losses can significantly degrade the performance of the filter. A process to fabricate a filter structure based on this type of waveguide was also briefly discussed. Other designs including a tethered beam design and a ridge waveguide based design were discussed. A semi-analytical theoretical modal analysis of the ridge was presented. Microfabrication of the ridge waveguide was discussed along with the challenges and limitations.

The main design of choice in this project was a differential filter based on the ridge waveguide. From the various analysis, theoretical calculations and fabrication experience, it can be concluded that the ridge waveguide had some significant drawbacks. Some of them are listed below. Due to fabrication hurdles, the final devices were not in a condition acceptable enough to be tested.

- Due to the nature of the excitation, there might have been more than 1 mode excited inside the ridge waveguide structure that would not decay along the depth of the ridge. This multi-modedness is harmful to the functioning of the filter. There could have been significant leakage into the bulk due to this second mode.
• In some simulations, it was observed that after a mode of the ridge encountered any discontinuity like an anchored electrode, it got scattered into other modes compounding the issue mentioned above.

• Fabrication of this filter was a major challenge. Some of the issues could have been mitigated by a better layout or more investment in the process flow, while other issues require a radical rethinking of the entire filter design.

In general, the following issues can create significant challenges when designing the filter –

• Transduction efficiency
• Attaining single moded operation
• Free boundary conditions causing undesired reflections
• Mechanical RF coupling of the transducer array causing loading of the waveguide
• Substrate losses and electrode reactances
• Small transducer spacing at high design frequencies
• Transducer capacitance and matching bandwidth
• Fabrication difficulties
9.1 Alternative Structures

A few other possible waveguide geometries are suggested in this section that can have a better chance of success. These are mostly modifications and combinations of the designs that have already been presented, namely, the strip waveguide, the tethered beam waveguide and the ridge waveguide. Only a basic finite element based harmonic analysis is presented here for all the structures along with some elementary observations. More detailed analyses and fabrication schemes are left up to the reader.

9.1.1 Rayleigh Ledge waveguide

In view of the difficulties mentioned above with respect to the ridge waveguide, another waveguide design incorporating structural changes to the ridge waveguide but still using the same symmetric Rayleigh-like mode was analyzed. The structure is made of a horizontal symmetric ridge waveguide which looks like a ledge, as shown in Figure 9.1. It also shows the simulated propagating wave at 200 MHz for the solid plate as well as the perforated plate. A propagation analysis was done for this structure. Resulting power loss plot and input impedance graphs for the solid plate are shown in Figure 9.2. A disadvantage of this type of waveguide is that it has slightly lower input impedance because of the solid plate. One way to increase the impedance is to make perforations in the solid plate, but it also reduces the propagation velocity. The characteristic impedance calculated as twice the input impedance was around 8000, which is smaller than the tethered beam design. In other simulations it was also seen that the loading effect and coupling of the biasing bridges to the central electrodes was quite negligible. In this symmetric ridge structure, it was hoped that due to the symmetry, the guide would not leak into the substrate. There is some leakage in this structure, as the plot shows. To avoid leakage, some strategies were experimented with, including the use of triangular
perforations to emulate an anechoic cone for an elastic wave. An array of slits along the propagation direction was also tested for its ability to confine the ridge mode. An acoustic equivalent of a photonic band gap, based on an array of holes of specific size was also tried. These techniques did help to confine the mode to some extent, but the overall attenuation constant of the structure was still not within acceptable limits. Fabrication of this design can pose a challenge in terms of biasing and anchoring the electrode structures.

Figure 9.1 The Rayleigh ledge waveguide resembling a horizontal symmetric ridge waveguide, displaying a guided Rayleigh-type propagating mode. Note that only half of the waveguide is shown. The acoustic impedance can be improved by making perforations in the solid plate, as shown in the simulation on the lower right.
9.1.2 Flexural Ledge waveguide

A variation of the previous ledge like waveguide was tried in which the ledge is excited from the bottom instead of from the sides. The manner of excitation is similar to the strip waveguide design with electrodes defined either by trench refilled high conductivity polysilicon or by doped regions in the substrate. Due to the nature of excitation, the operating mode is the anti-symmetric flexural mode of the ridge waveguide. This waveguide is shown in Figure 9.3 propagating the operating mode. As with the strip waveguide, an advantage of this structure is that the transduction area is much larger which reduces the acoustic impedance and the substrate electrodes avoid any bridge structures that could cause loading. Since the structure resembles a strip anchored only on one side, the acoustic impedance is also expected to be better than the strip waveguide which is anchored on both sides. Scaling a design like this is also quite feasible without significant changes in the process flow. This type of structure needs to be analyzed more thoroughly to estimate the substrate losses and to compare its
advantages over the strip waveguide. If a way can be devised to reduce the leakage into the substrate, this type of waveguide can lead to a successful filter design.

9.1.3 Symmetric Tethered Beam waveguide

Another possible structure which is a combination of the tethered beam design and the strip design is shown in Figure 9.4 operating in its mode of propagation. It consists of a single beam that is tethered on either side. The tethered beam is excited from the bottom using substrate electrodes similar to the strip design. The mode of propagation is again the Lamb mode as with the tethered beam waveguide discussed earlier, although here the particle displacement is primarily in the vertical direction. The structure also needs to be carefully analyzed to examine its performance and fabrication feasibility.
Figure 9.4 The symmetric tethered beam waveguide excited with electrodes underneath to produce a Lamb mode that propagates along the structure. Note that only half of the waveguide is shown.

9.2 Future Work

Future work and a few suggestions to improve the filter design are discussed next. A better acoustic waveguide structure with lower substrate losses needs to be conceived, in order to realize acceptable filter responses with lower insertion losses and higher filter Q values. To avoid leakage, waveguides can be lined with slits or holes resembling ‘anechoic cones’ that can confine the wave within the waveguide. Complex Electron Band Gap (EBG) like structures can also be designed to prevent losses from the waveguide within the frequency band of operation. If the working mode of a waveguide structure resembles the surface waves propagating at the edge of a mechanical ridge, then the results derived earlier in this dissertation and published in [35] can help in modeling the waveguide. Before finalizing a device, parasitic simulations should be done in Ansoft HFSS and Agilent ADS to study electrical leakage and other parameters. In the layout masks, a few dies should be modified specifically to do TRL measurements of the
acoustic waveguides. These measurements can be helpful in calibrating the filter model and design. A programmable tuning interface to electronically control the DC bias voltage of individual transducers can truly exploit the full potential of the proposed FIR filter. For example, if such a circuit is conceived, then the filter can rapidly switch between various frequency bands or can have multiple passbands in the same filter response. If a CMOS implementation of the device is worked out then it could add reliability and accuracy to the process flow. A CMOS based tuning interface circuitry with a programming capability can also be a part of the process flow. Even if part of the process flow is done in CMOS, it could aid in reducing fabrication errors. After such a process flow is conceived, it should first be tested in a physical fabrication simulation software like Silvaco before proceeding with the fabrication. Apart from the design of the FIR filter, an IIR filter based on resonators can also be implemented. The IIR structure can also be designed to be tunable to some extent with the DC bias voltages. The IIR structure must be simulated in Agilent ADS to verify its filter performance. To avoid reflections from the free end, a waveguide laid out in the form of a closed ring can be considered.

Analysis and modeling work to this point has given a good understanding of the working principles, performance tradeoffs and fabrication pitfalls of the device proposed in this dissertation. To date, there are no real programmable tunable filters for the microwave frequency range. With the appropriate acoustic waveguide structure, the proposed device has the potential to open the way for making miniature tunable filters in the GHz range.
REFERENCES


A-1 Elastic Wave Equation

\[ \nabla \cdot = \begin{bmatrix} \partial / \partial x & 0 & 0 & 0 & \partial / \partial z & \partial / \partial y \\ 0 & \partial / \partial y & 0 & \partial / \partial z & 0 & \partial / \partial x \\ 0 & 0 & \partial / \partial z & \partial / \partial y & \partial / \partial x & 0 \end{bmatrix} \]  
\[ (A.1) \]

\[ \nabla_s = (\nabla \cdot)^T \]  
\[ (A.2) \]

\[ \Gamma = k^2 \Gamma_{ch} - \rho \omega^2 \textbf{I} \]  
\[ (A.3) \]

\[ \Gamma_{ch} = \left( \Gamma_k \cdot \epsilon \Gamma_k^T \right) / k^2 \]  
\[ (A.4) \]

\[ \Gamma_k = \begin{bmatrix} k_x & 0 & 0 & 0 & k_y & k_z \\ 0 & k_y & 0 & k_z & 0 & k_x \\ 0 & 0 & k_z & k_y & k_x & 0 \end{bmatrix} \]  
\[ (A.5) \]

\[ \Gamma_{11} = k_x \left( c_{11} k_x + c_{16} k_y + c_{15} k_z \right) + k_y \left( c_{16} k_x + c_{66} k_y + c_{56} k_z \right) + k_z \left( c_{15} k_x + c_{56} k_y + c_{35} k_z \right) - \rho \omega^2 \]  
\[ (A.6) \]

\[ \Gamma_{12} = k_x \left( c_{16} k_x + c_{66} k_y + c_{56} k_z \right) + k_y \left( c_{12} k_x + c_{26} k_y + c_{25} k_z \right) + k_z \left( c_{14} k_x + c_{46} k_y + c_{45} k_z \right) \]

\[ \Gamma_{13} = k_x \left( c_{15} k_x + c_{56} k_y + c_{35} k_z \right) + k_y \left( c_{14} k_x + c_{46} k_y + c_{43} k_z \right) + k_z \left( c_{13} k_x + c_{36} k_y + c_{35} k_z \right) \]

\[ \Gamma_{21} = k_x \left( c_{16} k_x + c_{12} k_y + c_{14} k_z \right) + k_y \left( c_{66} k_x + c_{26} k_y + c_{46} k_z \right) + k_z \left( c_{56} k_x + c_{25} k_y + c_{45} k_z \right) \]

\[ \Gamma_{22} = k_x \left( c_{66} k_x + c_{26} k_y + c_{46} k_z \right) + k_y \left( c_{26} k_x + c_{22} k_y + c_{24} k_z \right) + k_z \left( c_{46} k_x + c_{24} k_y + c_{44} k_z \right) - \rho \omega^2 \]

\[ \Gamma_{23} = k_x \left( c_{56} k_x + c_{25} k_y + c_{45} k_z \right) + k_y \left( c_{46} k_x + c_{24} k_y + c_{44} k_z \right) + k_z \left( c_{16} k_x + c_{23} k_y + c_{34} k_z \right) \]

\[ \Gamma_{31} = k_x \left( c_{15} k_x + c_{14} k_y + c_{13} k_z \right) + k_y \left( c_{56} k_x + c_{46} k_y + c_{36} k_z \right) + k_z \left( c_{55} k_x + c_{45} k_y + c_{35} k_z \right) \]

\[ \Gamma_{32} = k_x \left( c_{56} k_x + c_{46} k_y + c_{36} k_z \right) + k_y \left( c_{25} k_x + c_{24} k_y + c_{23} k_z \right) + k_z \left( c_{45} k_x + c_{44} k_y + c_{34} k_z \right) \]

\[ \Gamma_{33} = k_x \left( c_{55} k_x + c_{45} k_y + c_{35} k_z \right) + k_y \left( c_{45} k_x + c_{44} k_y + c_{34} k_z \right) + k_z \left( c_{35} k_x + c_{34} k_y + c_{33} k_z \right) - \rho \omega^2 \]
A-2 Plate Boundary Conditions

(m=1⋯6 for the general case & m=1⋯3 for the symmetric/anti-symmetric cases)

\[
\overline{B}_m = \frac{\left( \tilde{D}_m^1 + \tilde{D}_m^2 \right) e^{-j \frac{k_m w_R}{2}}}{\left( \tilde{D}_m^1 + \tilde{D}_m^2 \right) e^{+j \frac{k_m w_R}{2}}} / \omega \tag{A.7}
\]

\[
\overline{B}_m = \left[ j \tilde{D}_m^1 \sin \left( k_y w_y / 2 \right) - \tilde{D}_m^2 \cos \left( k_y w_y / 2 \right) \right] / \omega \tag{A.8}
\]

\[
\overline{B}_m = \left[ j \tilde{D}_m^1 \sin \left( k_y w_y / 2 \right) - \tilde{D}_m^2 \cos \left( k_y w_y / 2 \right) \right] / \omega \tag{A.9}
\]

\[
\tilde{D}_m^1 = \begin{bmatrix}
  c_{46} ( k_y u_x + k_y u_y ) + c_{66} ( k_y u_x + k_y u_y ) \\
  c_{24} ( k_y u_x + k_y u_y ) + c_{26} ( k_y u_x + k_y u_y ) \\
  c_{44} ( k_y u_x + k_y u_y ) + c_{46} ( k_y u_x + k_y u_y )
\end{bmatrix} \tag{A.10}
\]

\[
\tilde{D}_m^2 = \begin{bmatrix}
  c_{16} k_x u_x + c_{26} k_x u_y + c_{36} k_z u_x + c_{56} ( k_x u_x + k_x u_z ) \\
  c_{12} k_x u_y + c_{22} k_x u_y + c_{23} k_z u_y + c_{32} ( k_x u_y + k_x u_z ) \\
  c_{14} k_x u_x + c_{24} k_x u_y + c_{34} k_z u_x + c_{45} ( k_x u_x + k_x u_z )
\end{bmatrix} \tag{A.11}
\]
A-3 Ridge Boundary Conditions

\( n = 1 \ldots N \)

\[
\overline{A}_n(p, y) = \sum_{m=1}^{6} b_{mn} \left( -j k_{\gamma_{mn}} \right)^n \left( \tilde{C}_{mn}^1 + \tilde{C}_{mn}^2 \right) e^{-j k_{\gamma_{mn}} y} / \omega
\]  \( (A.12) \)

\[
\overline{A}_n(p, y) = \sum_{m=1}^{3} b_{mn} \left( k_{\gamma_{mn}} \right)^n \left[ j \tilde{C}_{mn}^1 \sin \left( \frac{p \pi}{2} + k_{\gamma_{mn}} y \right) - \tilde{C}_{mn}^2 \cos \left( \frac{p \pi}{2} + k_{\gamma_{mn}} y \right) \right] / \omega
\]  \( (A.13) \)

\[
\overline{A}_n(p, y) = \sum_{m=1}^{3} b_{mn} \left( k_{\gamma_{mn}} \right)^n \left[ j \tilde{C}_{mn}^2 \sin \left( \frac{p \pi}{2} + k_{\gamma_{mn}} y \right) - \tilde{C}_{mn}^1 \cos \left( \frac{p \pi}{2} + k_{\gamma_{mn}} y \right) \right] / \omega
\]  \( (A.14) \)

\[
\tilde{C}_{mn}^1 = \left[ c_{14} \left( k_{\gamma_{mn}} u_{\gamma_{mn}} + k_{c} u_{\gamma_{mn}} \right) + c_{16} \left( k_{c} u_{\gamma_{mn}} + k_{\gamma_{mn}} u_{\gamma_{mn}} \right) \right]
\]  \( (A.15) \)

\[
\tilde{C}_{mn}^2 = \left[ c_{11} k_{x} u_{\gamma_{mn}} + c_{12} k_{x} u_{\gamma_{mn}} + c_{13} k_{x} u_{\gamma_{mn}} + c_{15} \left( k_{x} u_{\gamma_{mn}} + k_{c} u_{\gamma_{mn}} \right) \right]
\]  \( (A.16) \)