Integrated Distributed Power Management

System for Photovoltaic

by

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A Dissertation Presented in Partial Fulfillment
of the Requirements for the Degree
Doctor of Philosophy

Approved July 2014 by the
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August 2014
ABSTRACT

Photovoltaic (PV) systems are affected by converter losses, partial shading and other mismatches in the panels. This dissertation introduces a sub-panel maximum power point tracking (MPPT) architecture together with an integrated CMOS current sensor circuit on a chip to reduce the mismatch effects, losses and increase the efficiency of the PV system. The sub-panel MPPT increases the efficiency of the PV during the shading and replaces the bypass diodes in the panels with an integrated MPPT and DC-DC regulator. For the integrated MPPT and regulator, the research developed an integrated standard CMOS low power and high common mode range Current-to-Digital Converter (IDC) circuit and its application for DC-DC regulator and MPPT. The proposed charge based CMOS switched-capacitor circuit directly digitizes the output current of the DC-DC regulator without an analog-to-digital converter (ADC) and the need for high-voltage process technology. Compared to the resistor based current-sensing methods that requires current-to-voltage circuit, gain block and ADC, the proposed CMOS IDC is a low-power efficient integrated circuit that achieves high resolution, lower complexity, and lower power consumption. The IDC circuit is fabricated on a 0.7 μm CMOS process, occupies 2mm x 2mm and consumes less than 27mW. The IDC circuit has been tested and used for boost DC-DC regulator and MPPT for photo-voltaic system. The DC-DC converter has an efficiency $\eta = 95\%$. The sub-module level power optimization improves the output power of a shaded panel by up to 20%, compared to panel MPPT with bypass diodes.
DEDICATION

To my wife, for her comprehension, support and love.

    I love you darling.

    We finally made it!!!!

To my family, for their support and trust.
ACKNOWLEDGMENTS

Special thanks to my wife Alix Rivera-Albino who was my companion and support through every step of the way. I would like to thank Dr. Sayfe Kiaei and Dr. Bakkaloglu for their continuous guidance, support and their invaluable help in the development of this research. Thanks to my committee members Dr. Jennifer Kitchen and Dr. Jae-Sun Seo. The invaluable help of James Laux was crucial in this work. Finally, to Dr. Debashis Mandal, Chenxi Liu, Yao Zhao, Kiran Kumar Krishnan Achary and Shrikant Singh who were always there when I needed them.
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CHAPTER 1

INTRODUCTION

Due to the rising concerns about energy cost and environmental impact, along with the depleting resources associated with fossil fuels, there is an increasing demand on the development of alternative low-impact sustainable energy sources such as photo-voltaic (PV), wind, hydro-electric and fuel cells. The PV source alternative produces electricity in any location with direct sun light (even remote areas where utility grid is not available), does not generate any noise (ideal for dense residential areas) and requires low maintenance.

1.1 SYSTEM OVERVIEW

An example of a residential PV system is illustrated in Figure 1-1. Residential PV power sources are considered small, with a power generation of less than 10kW [1], [2]. These power sources consist of:

- *Energy harvesting elements*: array of PV panels,

- *Power management (PM) unit*: used to maximize the power generation of the PV array and convert from DC to AC power,

- *Distribution devices*: junction box, meters, fuse, etc. used to direct the power to the residence and electric utility grid [3].

The first two elements of the PV system can be represented in a block diagram as shown in Figure 1-2. The PV generator, or array of panels, converts the incident light (irradiance) to electric power. As part of the PM unit, the DC-DC converter is responsible to track the maximum power point (MPP) of the PV panel/array to ensure the system is
working at its optimum point for any variation in irradiance, temperature or load. Finally, an inverter is used to convert the DC power of the PV system to AC power. Once the power is AC, it can be used to energize typical house appliances or connected it to the utility grid.

Figure 1-1: Residential solar power system.

Figure 1-2: Block diagram of a PV system.

The basic unit of a PV system is the solar cells, as shown in Figure 1-3a. These cells are $pn$-junction devices (diodes) that emit a high amount of current when exposed to the sun light. In typical mono-crystalline photovoltaic panels, the cells produce a voltage
of 0.5 V and a current from 5 to 9 A. These cells are combined in series to increase the output voltage in row called panels. A conventional mono-crystalline panel contains 72 cells in series to produce an output voltage of 36 V with a current of 5 to 9 A [4], [5]. The panels contains bypass diodes every 24 cells to protect the cells against hot-spot [6], [7] as illustrated in Figure 1-3b. This smaller group of 24 cells is called sub-panel.

The current to voltage (I-V) characteristic of a PV panel is illustrated in Figure 1-4a. This I-V characteristic shows the fourth quadrant of an illuminated pn-junction diode curve: as the voltage increases, the current will stay almost constant (similar to a
current source) until a specific voltage is reached where the current start falling exponentially. Based on the I-V curve, the power of the PV panel is obtained as illustrated in Figure 1-4a. The PV power characteristic shows a unique maximum power point. This means that a specific load have to be connected to be able to operate the PV panel at its maximum power point. Unfortunately, the IV curve varies with environmental factors, such as incident light and temperature as shown in Figure 1-4b and c, respectively. A different load is required to optimize the power for each light/temperature condition. Real time optimization system is used to track the maximum power point of the panel for any condition.

![Figure 1-4: Electrical characteristics of a mono-crystalline PV panel. (a) Typical current and power as function of the voltage. (b) Response to changes to incident light (irradiance). (c) Response to changes in temperature.](image)

The power maximization (MPPT) is achieved by combining a switched DC-DC converter (buck, boost, buck-boost, etc.) and a maximum power point tracking (MPPT) algorithm [3], [8-10]. Figure 1-5 illustrates the flow chart of one MPPT algorithm known as perturb-and-observe (P&O). This algorithm uses a current and voltage sensor located
at the input of the DC-DC converter to calculate the generated power. Then, it determines if the power is rising or falling compared to previous samples. With this information, the conversion rate (e.g. duty-cycle, D) of the DC-DC converter is varied by a step size (ΔD). This change results in variation of the input impedance of the converter (input current and voltage change). The MPPT algorithm iterates to ensure the input impedance of the DC-DC converter and the PV array match. The matching point is where the maximum power is produced by the panel/array.

![Flowchart](image)

Figure 1-5: Perturb and observe MPPT algorithm.
An important step on MPPT for PV systems is the power sensing (voltage and current sensing). The integration of voltage, current, or signal sensing (e.g. power-line communication) is vital to enable improved performance and real-time stability. The voltage is easy to measure, because most of the analog-to-digital converters (ADC) are based on input voltage. On the other hand, current represents a challenge requiring either lossy or large elements to convert current to voltage to then use an ADC. Given that the DC current (power) in each PV panel is over several amperes (200-300W Power), standard CMOS circuits cannot handle direct signal measurements. For PV application, development of integrated circuits (IC) using standard CMOS technology will improve size, efficiency, performance, reliability (minimum off-chip passive components), and reduce the system cost [11], [12].

1.2 OBJECTIVES

In this research, a power management unit for residential or small commercial solar systems is designed and implemented. The proposed system is aimed at improving the current technology in photovoltaic power management units through the design of an integrated current sensor using standard CMOS technology and a sub-panel distributed converter. In order to achieve this goal, the following objectives must be fulfilled:

- Reduce the system design complexity and size in an effort to make a simple converter that can be integrated to the panels. This will make the system design modular (single panel required for power increase), greatly simplified, and smaller in size.
• Minimize the use of passive and external components. This step will also help in the reduction of the size of the converter. The use of state of the art FETs, converters, and design techniques will allow this reduction.

• Improve power extraction efficiency, converter availability (if a single converter fails the reminder of the system is not affected), and MPPT (better response to partial shading). The ability to perform MPPT at a sub-panel level improves the power extraction and reduces the effects of partial shading and mismatches over the panels. Having additional converters in the system reduces power outage under converter failure by affecting only a small portion of the output power.

• Reduce current sensing losses. Current sensing is a procedure that requires a bulky coupling element or lossy passive element in series with the panels. This research will use an alternate method that removes the series passive and coupling elements, helping to improve the efficiency and size of the converter. The sensor is designed in standard CMOS technology to minimize its size and the use of off-chip components.

1.3 SUMMARY OF THE FOLLOWING CHAPTERS

This dissertation is organized as follows.

• Chapter 2: Literature review. This chapter starts with the review of the common PV architectures and a comparison between them. Then, it presents the typical current sensing techniques used for photovoltaic applications.

• Chapter 3: Proposed MPPT Photovoltaic Architecture. This chapter is devoted to the high level PV architecture. It presents the block diagram of the proposed system and gives an overview of the main blocks of the system.
• Chapter 4: Proposed Current Sensor. This chapter introduces and explains the proposed current sensor technique. It gives a detailed explanation of the proposed current sensing technique as well as the high level of the circuit used in the implementation.

• Chapter 5: Circuits and Simulations. This chapter is devoted to the circuit implementation and simulations used in the design process of the sub-panel system and the current sensor. The first part gives the characteristics of PV panel used for the design. Then, it contains the design of the DC-DC converter. Finally, the details on the current sensor circuit are discussed.

• Chapter 6: Measurements and Analysis. This chapter starts presenting and describing the prototype. Then, the test goals and setup are explained. Finally, the measured results and analysis of the proposed system are discussed.

• Chapter 7: Conclusions and recommendations. This chapter provides the conclusions and recommendations for future work.
CHAPTER 2

BACKGROUND

The objective of the MPPT systems is to optimize the output power of a PV source [3], [8-10]. The output power that can be extracted from a PV system, under mismatch conditions, depends on the type of MPPT architecture that is used and the losses in the converters [1],[2]. This chapter will review and compare the system architectures used for MPPT. Then, it will show the common current sensors used in PV applications. This information will help on the development of specifications for the system proposed in this research (PV architecture, DC-DC converter and sensor).

2.1 PHOTOVOLTAIC SYSTEMS ARCHITECTURE

The architecture employed for a PV system depends on the environment, location, application, shape and size of the system. Typical PV systems for residential customers produce power between 4kW to 10kW. These systems are commonly affected by environmental factors such as shading, bird dropping and soiling [1],[2],[13-15]. This section discusses and compares three PV power management architectures for residential power sources: (1) centralized [3, 16, 17], (2) distributed panel level [13] [18-23] and (3) sub-panel level [2, 24-28].

Centralized PV System

Residential photo-voltaic sources are commonly configured for centralized power management. In a centralized PM system, the solar panels are configured in strings (panels connected in series) to build the required voltage (e.g. ~ 400V for efficient DC-AC conversion). Then, various strings are connected in parallel to get the desired power
level (e.g. 4kW to 10kW). Figure 2-1 shows the block diagram of a 4kW residential PV system. The PV array is configured in strings of eleven panels to provide approximately 400Vdc at the input of the inverter (~ 2kW per string). The system contains two parallel PV strings to achieve the desired power level (~ 4kW). Blocking diodes are added to each string to avoid reverse current flow through the string under partial shading conditions [3]. This combination of parallel strings is called PV array. The output power of the array is then fed to the central PM unit for MPPT and DC-AC conversion [16, 17].

Figure 2-1: Block diagram of a 4kW residential PV system. The system consists of two strings in parallel, each with 11 panels.

Figure 2-2 shows a block diagram of a central PM unit (inverter box). The inverter box consists of two PM levels: (a) MPPT and (b) DC-AC conversion. The MPPT is achieved by employing a DC-DC converter together with a maximization algorithm controller. The controller senses the array power and decides the new converter’s duty cycle to maximize the PV power. The output of the MPPT circuit is fed to an inverter to convert the power from DC to AC. The AC output voltages amplitudes are 120Vac and 240Vac at a frequency of 60Hz (i.e. standard grid and household appliances voltage levels in the United States).
Figure 2-2: Block diagram of an inverter box, including the MPPT and the DC-AC

The central system is the most intuitive architecture for photovoltaic systems, but its performance could be limited. Some of the factors that affect the central power management are: (a) components power stress (low reliability), (b) MPPT (partial shading response), (c) fire and shock hazard and (d) system design complexity. Details of the limitation of the central PM are as follow:

(a) Components power stress:

The central inverter box process the power of the entire array (4kW, in this case). The components of this inverter must handle high voltage and current levels under environments of high humidity and high temperature. To handle the conversion rate and power levels, they normally require components such as transformers and unreliable electrolytic capacitors [29]. Therefore, they occupies a large area and suffer from a limited lifetime [29], [30]. The central inverter represents 25% to 35% of the total cost of the system. On existing products, a PV panel warranty is around 25 years, while, the warranty for a centralized inverter is only 5 to 10 years[30]. This disadvantage requires to provide maintenance more often to the system, replacing the inverter box up to five times in the life of the solar panels.
(b) MPPT:

Photo-voltaic systems located in residences are exposed to different environmental characteristics (i.e. trees, chimney, pipes, satellite dish, etc.). These conditions cause mismatches due to clouds, partial shading, soiling, temperature gradients, bird droppings, and physical degradation of the panel [1], [13-15]. The mismatches degrade the performance of centralized inverter used in a residential system by reducing the power yield in the operating points of the individual panels [1],[2],[13-15]. Panels affected by mismatches in incident radiation or temperature gradients does not allow other panel in the system to operate at their maximum operating points, because they are limited by the series currents or parallel voltages in the system. Bypass diodes are used to reduce this effect at the expense of a reduction in the available power of the system (i.e., the power generated by the shaded cells is not used).

(c) Fire and shock hazards:

The central PV system has to process the power of the entire array in a single power management unit. There is not option of disconnecting or powering down the array under any emergency (i.e. even if the inverter is OFF the array still is energized). For example, in case of a fire, the array represents a shock hazard to the fire fighters as well as any other person that throw water over the panels (current flow through the water) [31]. Hazards also exist in any other type of disaster where the emergency response people may be exposed to the array.
(d) System design complexity:

In a centralized design, the number of panels per strings, the brand, model and orientation of the panels must be the same in the entire array. If a panel fails it has to be replaced by the same brand and model, which may be difficult to find after several years [13]. This configuration suffer from two limitations to increase the power of the system after installation: (1) the inverter must be changed to satisfy the new power level and (2) if the area where the system is installed does not allow an entire new string, the system power cannot be increased (even if there is space for some panels) [3].

In an effort to find the optimum power management for centralized PM systems, academia has proposed reconfigurable arrays as shown in Figure 2-3 [32-36]. This architecture combines the panels with a switch matrix that allow the reconfiguration of the electrical path between individual panels in an array. The concept is to use the information from each panel to search the configuration that provides the higher power. Once the best configuration of the array is found the MPP is tracked by a centralized converter.

Ideally, the reconfigurable concept provides great advantages to improve the system performance under partial shading conditions. However, this architecture has several limitations, such as:

(a) The switching matrix requires a high number of switches to be able to configure the array.
Figure 2-3: Reconfigurable photovoltaic array architecture. A switch network is used to find the configuration that provides the highest power.

(b) Driving the static switches represents a big challenge, because the gate voltage required by all the switches is different and has to be independently controlled.

(c) The losses introduced by the switches and extra wiring in the DC path degrade the performance of the system.

(d) The status of all the panels has to be known to identify the shaded panels. Iteration between configurations to find the higher MPPT slows down the maximization process.

(e) The cost and complexity of the system is increased compared to the typical centralized design.

All these problems results in a non-practical alternative for real time PV output power maximization.
Distributed Power Management

Improvements in power electronics technology allowed relocating the power management circuit from the central inverter box to the individual panels, as shown in Figure 2-4. These single panel PMs are known as distributed MPPT converters (DMPPT). Figure 2-4 presents the three more common DMPPT circuits: (a) micro-inverter [13] [18-20], (b) parallel power optimizer [13] [21] and (c) series power optimized [13], [22], [23]. Micro-inverters are DMPPT that maximize the power of the panel and provides an AC output voltage (120Vac). The two optimizers (Figures b and c) track the MPP at each panel and then use a simple central inverter for the DC-AC.

Figure 2-4: Distributed converters. (a) Micro-inverter. (b) Parallel power optimizer (DC-DC). (c) Series power optimizer (DC-DC).
DMPPT converters—either DC-DC converters or micro-inverters (DC-AC)—provide many advantages over central PM. These advantages are: reduce power stress of the components, additional power recovery, reduces system design constrains, individual panel monitoring and diagnostics, and increase the availability of the system. DMPPT circuits only process the power of a single panel (180W instead of 4kW). The reduced power stress (voltage and current) on the components allows the replacement of electrolytic capacitors and high voltage/current devices for more reliable parts. The use of reliable parts allow companies to increase the warranties of these DMPPT circuits to match the 25 years of the panels [37] [38].

Distributed converters are used to mitigate the effects generated by panel mismatch and partial shading. This improvement is achieved by tracking the MPP of the individual panels instead of the operating point of the entire array. There are several models of DMPPT converters on the market [37] [38].

The distributed PM requires one converter per panel, increasing the system cost. However, their use allows local maximization of the power (i.e., at the panel level). Taking into account only partial shading mismatch, this method allows 11.8% improvement to the annual output power, compared to the centralized PM [1] [2] [13].

Panel circuitry permits additional functions, such as, local monitor and diagnostic of the system (fail detection). The communication with the individual panels also allows the shutdown of the system under any emergency or disaster, reducing the shock hazard. The next sub-sections will provide an overview of the available alternatives for distributed power management including: (a) micro-inverter, (b) parallel power optimizer, and (c) series power optimizer.
Micro-Inverter

One type of DMPPT circuit is the micro-inverter [13] [18-20]. This configuration maximizes the power and provides an AC output voltage at each panel. Similar to the central inverter box, this system uses a DC-DC converter for MPPT and a DC-AC converter to obtain the AC output. One panel with a micro-inverter is a complete system and can be used to power any AC load inside its power ratings.

Micro-inverters reduce the impact of a panel over the others and allows output parallel connections, as shown in Figure 2-4a. The parallel connection of panels reduces the design and planning of the PV system, because an arbitrary number of panels can be connected to optimize the use of the available areas and client’s budget.

Micro-inverters are an ideal solution for systems that require a small amount (<10) of panels (i.e. recreation vehicles, RV, or street lighting). As the system size increases (i.e., residence requires >22 panels), the price also increases substantially. A single micro-inverter costs 20% to 50% more than a power optimizer [39]. The increase in the price is because each PM unit requires a DC-DC converter for MPPT and an inverter for DC-AC. In addition, this topology requires phase detection and synchronization between all the panels and with the utility power grid. This requirements increase the complexity of the power quality control, sensing, and internal communication.

Parallel Power Optimizer

Another alternative of DMPPT are the power optimizers (maximizers). The power optimizers consist of a DC-DC converter per panel and a central inverter for the entire array, as shown in Figure 2-4b and c. These power optimizers are divided in two main
groups based on the conversion rate and output connection required to achieve the desired output voltage. We will refer to them as series and parallel power optimizers, based on their output voltage connection.

Figure 2-4b shows the configuration of the parallel power optimizer architecture. In this configuration, the converters maximize the output of the individual panels, and boost the input voltage to achieve the required voltage for the inverter input (1:11 normal conversion ratio). This technique allows parallel connection of the distributed PM units. Similar to the micro-inverter case, the design of a parallel power optimizer provides the flexibility to be adjusted to the available area and customer budget [13] [21]. In addition, by increasing the output voltage, the current is decreased, allowing a reduction in the DC wiring cost.

The high step-up ratio requires converter topologies that include transformers to achieve the desired output voltage level [13], [21]. This causes an increase of the converter size. In case of partial shading on the panel the bypass diodes short the shaded portion of the panel resulting power lost, similar to the centralized case.

Series Power Optimizer

The series power optimizer architecture is shown in Figure 2-4c. This architecture has a DC-DC converter per panel and a central inverter for the entire array, like the parallel power optimized architecture. Similar to the connection of PV arrays for centralizes systems, the output voltages of the converters are combined in series to build up the voltage level required for the central inverter [13], [22], [23]. Therefore, in this technique, the conversion rate of the DC-DC converters is small (commonly 1:1).
The series power optimizer provides single panel power optimization as well as panel monitoring and control. The connection of the outputs in series causes a dependency of output current on all the series-connected converters [13]. If just one converter cannot provide the required current the others will be affected.

Series power optimizer adds complexity to the system design, because many panels have to be connected in series to achieve the required voltage. If the customer wants to increase the system power, an entire row has to be installed reducing the flexibility to upgrade the system.

**Sub-Panel Power Optimizer**

The most recent development in DMPPT converters is the sub-panel power optimizer. This architecture uses three DC-DC converters instead of bypass diodes (avoiding the diodes to turn ON under partial shading), as shown in Figure 2-5a. The converters are used to separately optimize the power of the sub-panels [2, 24-28]. This topology is similar to the series power optimizer, but, in this case, the series converters are internal to the panel.

The DC-DC converters used in published works produce low conversion rates (i.e., 1:1, buck or buck-boost) [2, 24, 25]. The resulting output after the combination of the three converters give the typical voltage of a panel (i.e., 36V), as shown in Figure 2-5a. Replacing the bypass diodes by sub-panel MPPT converter gives two main advantages: (1) the power of a shaded sub-panel is optimized instead of bypassed and (2) eliminate the multiple maximum power points under partial shading.

This architecture improves the energy production under partial shading by around 14.6%, compared to the centralized MPPT [1] [2]. The sub-panel power optimizer
architecture results in a reduction of power stress on each converter, improves the energy production under partial shading and removes the local maximum power points allowing simpler MPPT algorithms.

The combination of several panels in series, to achieve the voltage required for the central inverter (Figure 2-5b), increases the design complexity and limits the flexibility of the array.

![Diagram of DC-DC Converters](image)

Figure 2-5: Distributed sub-panel DC-DC with centralized inverter. (a) Single panel configuration. (b) System configuration.

**Comparison of PV System Architectures**

This section compares the three methods for PV power management discussed above: central, distributed and sub-panel level. The study compares the three PV PM architectures in the same system and shading circumstances. The comparison is based on the residential system shown in Figure 2-6a.
Figure 2-6: Residential system affected by partial shading. (a) Drawing of the shaded system. (b) Schematic view of the system.

The example consists of 22 PV panels (4kW) located on a residence roof with elements such as chimney, pipes and satellite dish [40]. The case under study is at 3:00pm where shading reaches some of the panels producing partially shading. At that time of the day the expected incident irradiance is 600kW/m² and shaded irradiance is
200kW/m² [1]. The analysis for the central power management system will be explained in detail and the others methods wills be calculated similarly.

Figure 2-6b shows the panels connected in a centralized PV system configuration. The system contains two rows (strings) of 11 panels each (396 V). When the two sub-circuits (String 1 and String 2) are matched (no shading), they have a common maximum power point, as shown in Figure 2-7a. When the system is exposed to shades (Figure 2-7b), the shaded sub-circuits operate at a different operating point. As result, the combined maximum power point (1.7 kW) differs from the combined operating points of the individual sub-circuits (0.82 kW + 1.069 kW = 1.89 kW).

Centralized power management suffers a power loss of 27% from the non-shaded case. If the power of the individual strings is maximized, 11% of that power loss in central PM can be recovered. Table 2-1 illustrates the power improvement for the different levels of distributed MPPT. The sub-panel power optimization represents a substantial power improvement with a 20% additional power. This makes it a viable alternative for improved power maximization.
Table 2-1: Power loss and recovered for four PV system architectures.

<table>
<thead>
<tr>
<th>MPPT Level</th>
<th>Power (kW)</th>
<th>Loss from no-shade (%)</th>
<th>Improve from Central (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Central</td>
<td>1.70</td>
<td>27.6</td>
<td>0.0</td>
</tr>
<tr>
<td>String</td>
<td>1.89</td>
<td>19.6</td>
<td>11</td>
</tr>
<tr>
<td>Panel</td>
<td>1.93</td>
<td>18.0</td>
<td>13.2</td>
</tr>
<tr>
<td>Sub-Panel</td>
<td>2.05</td>
<td>12.6</td>
<td>20.7</td>
</tr>
</tbody>
</table>

2.2 CURRENT SENSOR

Power metering for MPPT allows the PM unit to obtain the optimum power from the solar panels. In power sensing, two quantities are required: voltage and current. The voltage sensing can be easily obtained with ADCs. Current sensing is more challenging, because there is not a direct method to sense current. The goal in this research is to find a current sensor which is compact, easy to integrate to an integrated circuit (IC) and uses standard CMOS even for high voltage levels. This section discusses three current sensing alternatives for MPPT: (1) resistor, (2) Hall Effect, and (3) current transformer.

Resistive Current Sensor

The most common current sensing approach uses a series resistor to convert the current into a voltage, and digitize the signal using an ADC as shown in Figure 2-8 [41-48]. This method is simple to implement and consumes a small area compared to other methods. The additional series resistance has several disadvantages in terms of efficiency, accuracy, heat dissipation, and requires high voltage CMOS process.

A variant to this method is to replicate a scaled version of the current of the triode device (switch). Then, the scaled current flows through a sensing resistor to be converted to voltage [49],[50]. However, due to the high current that flows through the triode
device, external FETs are required. Therefore, this method is not a viable alternative for high currents PV systems.

![Diagram](image)

Figure 2-8: Resistive current sensor block diagram.

**Current Transformer Sensor**

The current transformer sensor is a better alternative for high current environments [48, 51, 52]. This method used a 1:N current transformer to couple the current to an isolated circuit in the secondary, as shown in Figure 2-9. This isolated circuit converts the current into a voltage and digitize the value using an ADC. The circuit in the secondary can now use standard CMOS process to digitize the signal. However, a transformer in the signal path adds inductance to the path, increases the noise, sensor size, electromagnetics emission, design complexity, and require additional ADC circuit.
The Hall Effect current sensor uses a concept similar to the current transformer [48, 51, 52]. The sensor couples the magnetic field produced by the current to a piezoelectric material and a magnet. The secondary of the circuit contains an isolated circuit which converts the current back to voltage and uses an ADC for digitization as shown in Figure 2-10. The Hall Effect sensor does not introduce any additional parasitic to the primary current path and standard CMOS process can be used at the secondary. The main disadvantages of this sensor are the increase in size, complexity, the sensor is sensitive to temperature variations and it is inaccurate at low current levels.
CHAPTER 3

PROPOSED MPPT PHOTOVOLTAIC ARCHITECTURE

Solar power systems are continuously evolving to achieve an affordable and durable solution to fossil fuel sources. This research is an effort to contribute and improve current technologies. The system proposed in this chapter combines the advantages of two of the architectures presented in section 2.2 (Parallel Power Optimizer and Sub-Panel Power Optimizer). This new topology optimizes the power of the sub-panels and boosts the output voltage to achieve parallel panels’ connection. The result is a reduction in design complexity, installation costs, size, and partial shading effect.

3.1 PARALLEL SUB-PANEL DC–DC CONVERTER (PSPDC)

The proposed architecture is shown in Figure 3-1. The high level view is similar to the Parallel Power Optimizer. Each sub-panel MPPT box contains four converters: one for the MPPT at each sub-panel (3 in total) and one for the output voltage regulation. This architecture will allow flexible design and installation which can fit the customer requirements and budget.

Parallel sub-panel converter maximizes each individual sub-panel to allow higher output power under partial shading or other mismatch conditions, compared to a panel MPPT. The voltages stress for each MPPT converter is reduced to 33% of the voltage of one panel (~ 12V). This reduction allows the use of more efficient, smaller, cheaper and reliable components in the design of the converter. To optimize area, the four converters are in the same board and a single digital controller is used for all of them.
Figure 3-1: Proposed distributed parallel sub-panel DC-DC converter system.

The sub-panel structure can be implemented with reduced modifications to the panel architecture. In the back of the panel, the bypass diodes are placed in a junction box, as shown in Figure 3-2. That junction box gives access to the three individual sub-panels.

Figure 3-2: Bypass diodes in a commercial panel. The figure illustrates the access points to each sub-panel in a commercial panel.
3.2 ARCHITECTURE OF THE CONVERTER

The proposed architecture takes advantage of the structure of a typical monocrystalline panel that contains three sub-panel circuits (24 cells each), as illustrated in Figure 3-2. Each sub-panel circuit generates 12 V and 5 A (~60 W). Figure 3-3 shows the detailed configuration of this sub-panel MPPT structure.

![Diagram showing the architecture of the converter](image)

Figure 3-3: Internal architecture of distributed sub-panel DC-DC converter.

The MPPT converters (DC-DC 1 to 3) have a step-up ratio of 1:10 (12V to 120V). The regulating DC-DC converter (DC-DC 4) uses a simple partial power processing topology to efficiently regulate the output voltage. The outputs of the three MPPT converters are combined in series to build up 360V. Then, the partial processing converter produce 40V, which will increase and decrease as the 360V of the MPPT converters change, due to mismatch, to ensure a 400V regulated system output.
By employing the sub-panel MPPT, the voltage and power processed by each converter is reduced (compared to panel or central MPPT). This allows the use of components with lower losses and more reliable, such as, surface mount ceramic capacitors. Converters with high voltage step can be implemented with simpler circuits (i.e., remove bulky transformers). MPPT is local to each sub-panel and remove the interaction between sub-panels to improve the power generated. The system regulates the output voltage to ensure efficient parallel connection of the panels.

3.3 SYSTEM SPECIFICATIONS

The specifications in Table 3-1 have to be addressed to ensure the system performance is comparable with current products. These specifications were taken from commercial products as well as from state of the art research [2] [4, 5] [21] [18].

Table 3-1: Distributed sub-panel DC-DC converter specifications.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Efficiency</td>
<td>90% - 93%</td>
</tr>
<tr>
<td>Maximum Input Voltage</td>
<td>14.7V</td>
</tr>
<tr>
<td>Nominal Input Voltage</td>
<td>12V</td>
</tr>
<tr>
<td>Maximum Output Voltage</td>
<td>140V</td>
</tr>
<tr>
<td>Nominal Output Voltage</td>
<td>120V</td>
</tr>
<tr>
<td>Maximum Input Current</td>
<td>5.5A</td>
</tr>
<tr>
<td>Nominal Input Current</td>
<td>4.77A</td>
</tr>
<tr>
<td>Nominal Output Current</td>
<td>0.5A</td>
</tr>
<tr>
<td>Conversion Rate</td>
<td>1:10</td>
</tr>
<tr>
<td>Frequency of Operation</td>
<td>100k–400kHz</td>
</tr>
<tr>
<td>Transistor Type</td>
<td>GaN</td>
</tr>
<tr>
<td>Input Ripple</td>
<td>&lt;8.5% of Vmpp</td>
</tr>
<tr>
<td></td>
<td>~ (5% of 11V = 0.55V)</td>
</tr>
<tr>
<td>Output Ripple</td>
<td>&lt;0.5% ~ 1.2V</td>
</tr>
<tr>
<td>Topology</td>
<td>Double lift boost converter</td>
</tr>
</tbody>
</table>
3.4 MPPT CONVERTER

The main requirements for the converters are small component values, reduced number of components and low voltage stress for the switches. Figure 3-4 shows the schematic of one possible topology, called boost double-lift converter [53]. It is a boost converter with two additional switches and capacitors that achieves double of the conventional boost voltage.

![Schematic of boost double-lift converter](image)

Figure 3-4: Boost double-lift converter for sub-panel MPPT.

The design equations for the converter are as follows:

- Output voltage \( V_0 \):
  \[
  V_0 = \frac{2V_{in}}{1 - D}
  \]  
  \[\text{(1)}\]

- Inductor \( L \) size for a given load:
  \[
  L = \frac{R_L \times D \times (1 - D)^2}{8 f_s}
  \]  
  \[\text{(2)}\]

- Output capacitor \( C_0 \) for a given output voltage ripple \( \Delta V_0 \):
  \[
  C_0 = \frac{V_0 \times D}{f_s \times \Delta V_0 \times R_L}
  \]  
  \[\text{(3)}\]

- Input capacitor \( C_{in} \) for a given input voltage ripple \( \Delta V_{in} \):
\[ C_{in} = \frac{\Delta I_L}{8 f_s \Delta V_{in}} = \frac{V_{in} \times D}{8 \times \Delta V_{in} \times f_s^2 \times L} \]  \hspace{1cm} (4)

- Internal capacitor \((C_1, C_2)\) for a given voltage ripple \((\Delta V_1, \Delta V_2)\):

\[ C_{1,2} = \frac{V_0 \times D}{f_s \times \Delta V_{1,2} \times R_L} \]  \hspace{1cm} (5)

where \(V_{in}\) is the input voltage, \(D\) is the converter duty cycle, \(f_s\) is the switch frequency, and \(R_L\) is the load of the converter.

### 3.5 OUTPUT DC-DC CONVERTER

The fourth converter in the proposed architecture ensures a constant output voltage of 400V. This converter should handle only part of the power to reduce the losses. One possible technique is the feed forward buck-boost shown in Figure 3-5. This architecture connects its output \((V_{01})\) in series to the input \((V_{in})\) to generate only the voltage, that combined with the input, achieve the desired output (i.e., \(V_0 = 400V\)).

![Feed forward buck-boost converter](image)

Figure 3-5: Feed forward buck-boost converter. Partial power processing DC-DC converter used for the output regulation.
The output voltage $V_{01}$ of the converter is given by:

$$V_{01} = V_{\text{in}} \frac{D}{1-D}. \quad (6)$$

The output voltage of the total sub-panel DC-DC converter ($V_0$) will be given by:

$$V_0 = V_{\text{in}} + V_{01}, \quad (7)$$

where $V_{\text{in}}$ is the voltage that results from the combination of the outputs of the three MPPT converters.

Even with the sub-panel optimizer advantages, the MPPT converters need to process an input current of 5 to 9 A. Efficient sensing of this current represents a challenge due to its high value. High voltage process or bulky magnetic coupling devices are typically used to sense the current at high voltage levels (12V – 400V). The next chapter proposes a current sensor which can sense currents at any common mode voltage with a standard CMOS process and produces a direct digital output, reducing additional components requirements.
CHAPTER 4

PROPOSED CURRENT SENSOR

The proposed current-to-digital (IDC) sensor along with MPPT control circuit is shown in Figure 4-1. As shown in Figure 4-1a, the sensor measures the average output current and provides a digital output signal [54]. The application of the current sensor for DC-DC converter maximum power point tracking (MPPT) is shown in Figure 4-1b. The IDC sensor is a CMOS circuit and can be used for other high-voltage applications.

Figure 4-1: Block diagrams of the proposed current sensing. (a) Current sensor. (b) System.
including DC motor control, buck/boost converters, regulators, rectifiers, and inverters without the need for high-voltage process. The MPPT and the DC-DC converter consists of a boost converter with output filter capacitor $C_L$, load $R_L$, boost MPPT controller, connected to the voltage and current sensor to measure the voltage and current $i_L$ flowing through the load $R_L$ respectively.

The proposed IDC sensor shown in Figure 4-1a is a charge based circuit and consists of two input capacitors $C_1$ and $C_2$, a one-bit comparator, current source $I_{sink}$ and a digital timing circuit. The capacitors are switched by the clock phases $\phi_1$, $\phi_2$, and $\phi_3$. The input voltage is sampled across the capacitors $C_1$ and $C_2$. The current $i$ of a capacitor can be estimated by analyzing the charge transfer $\Delta Q$ in a period of time $\Delta t$, which is represented by:

$$i = \frac{\Delta Q}{\Delta t}. \quad (8)$$

If the time $\Delta t$ is fixed (i.e. sampled in a determined period), the current can be estimated by measuring the charges transferred to/from the capacitor. For a given $\Delta V$, the charge can be measured by,

$$\Delta Q = C \cdot \Delta V \quad (9)$$

The IDC sensor estimates the charges transferred and produce a digital representation of the current. The charge-based method can accurately measure the input current using low-voltage standard CMOS process for high-voltage applications.

The IDC circuit operation can be described by examining the voltage characteristics of the boost DC-DC converter waveforms shown in Figure 4-2. The boost converter MPPT shown in Figure 4-1b samples the DC-DC output voltage and current to
determine the maximum power operation. Given the sampled output voltage and current, the MPPT varies the pulse-width modulated (PWM) controller duty cycle $D$ (period $T_s$) to vary the pulse width and the output voltage. During the time switch $S_1$ is closed ($S_2$ open) the input voltage $V_{in}$ charges the inductor while the capacitor $C_L$ supplies the load current. During the cycle time when $S_2$ is closed ($S_1$ is open), the output $V_0$ is charged and is given by:

$$V_0 = V_{in} \frac{1}{1-D} \quad (10)$$

An output filter capacitor $C_L$ is used to average the output voltage and reduce the output voltage ripple within the desired range. The output voltage ripple ($\Delta V_0$) can be expressed as:

$$\Delta V_0 = \frac{V_0}{R_L C_L} DT_s = i_L \frac{DT_s}{C_L} \quad (11)$$

where $DT_s/C_L$ is a known constant for a given $D$ [55]. From (11), the load current $i_L$ can be found by measuring $\Delta V_0$. 

Figure 4-2: Boost DC-DC converter timing diagram.
In general, if a capacitor is linearly charging or discharging, the current can be estimated using the slope in a given time. For example, for the output of a boost converter shown in Figure 4-3, the capacitor is linearly discharging, and the current can be determined by:

\[ i_C(t) = C_L \frac{\Delta V}{\Delta t} \]  

(12)

where \( \Delta V \) is the voltage drop (\( \Delta V = V_1 - V_2 \)) in the time interval \( \Delta t = t_2 - t_1 \) and \( C_L/\Delta t \) is a constant for a fixed \( \Delta t \). In this case, the current in the capacitor can be estimated by sampling the output voltage in two fixed instances of time, \( t_1 \) and \( t_2 \) to obtain \( \Delta V \) and the current can be estimated using either analog techniques or digitized for digital processing.

The sampling and digitization for this current sensing technique is performed by the IDC circuit. The operation of the proposed IDC is similar to an integrating analog-to-digital converter method that compares the rate of discharge across a capacitor with a reference voltage [56-59]. The IDC circuit (Figure 4-1a) samples the DC-DC boost converter output voltage \( V_0 \) using the capacitors \( C_1 \) and \( C_2 \) (Figure 4-4a). The capacitor \( C_1 \) is discharged by a constant current source \( I_{\text{sink}} \) while the voltage across \( C_2 \) is held...
constant as a reference voltage, as shown in Figure 4-4b. The discharge time is then measured with a 1-bit comparator and a counter until the voltage across capacitor \( C_1 \) reaches the same value as the voltage in \( C_2 \). The IDC circuit measures and provides the digital representation of the load current using (12).

![AC model of the IDC](image)

**Figure 4-4: AC model of the IDC: (a) Switched capacitor sampling circuit. (b) Digitalization circuit.**

### 4.1 CURRENT TO DIGITAL CONVERTER OPERATION

The current sensor basic operation is illustrated in Figure 4-4 (the DC \( C_{\text{block}} \) capacitor and common mode resistors are ignored for simplicity) with the signal and timing diagram in Figure 4-5. The following steps describe the current to digital conversion process:

1- At time \( t_0 \) the switches \( \phi_1 \) and \( \phi_2 \) are closed and capacitors \( C_1 \) and \( C_2 \) are charged to initial value of \( V_0 \).
2- At time $t_1$ the switch $\phi_1$ is opened and the voltage level $V_0(t_1) = V_1$ is sampled and held by the capacitor $C_1$.

3- At time $t_2$ the switches $\phi_2$ will opens and $\phi_3$ closes.

   a. As $\phi_2$ opens, $V_0(t_2) = V_2$ is sampled and held at the capacitor $C_2$. During the time frame $\Delta t = t_2 - t_1$, the boost output has reduced from $V_1$ to $V_2$. The time $\Delta t$ has to be less than 10% of the boost period to ensure a normal dynamic range to the boost.

   b. As $\phi_3$ closes, the capacitor $C_1$ will discharge through a constant current source $I_{\text{sink}}$ at a linear and constant rate with slope $I_{\text{sink}}/C_1$ (Figure 4-4b).
c. At time $t_2$, the counter is enabled and will start counting the discharge time with clock frequency $f_{\text{clk}} (f_{\text{clk}} \neq f_s)$.

4- The time $t_3$ is determined when the voltages at $C_1$ and $C_2$ are equal. Thus, as $C_1$ discharges with a constant rate $I_{\text{sink}}/C_1$, the comparator is comparing the voltages of $C_1$ and $C_2$. Once these two values are equal, the counter is disabled. The discharge time $t_{\text{discharge}} = t_3 - t_2$ is expressed as:

$$t_{\text{discharge}} = \frac{\Delta V}{I_{\text{sink}}/C_1} = K \cdot T_{\text{clk}}$$

(13)

where $t_{\text{discharge}}$ is the time that takes the voltage in $C_1$ to drop from $V_1$ to $V_2$, $K$ is the counter binary output and $T_{\text{clk}}$ is the sensor clock period ($1/f_{\text{clk}}$). The resolution of the measurement ($K$) can be controlled by adjusting the values of $I_{\text{sink}}, \text{counter clock } T_{\text{clk}}$ and the sampling capacitor $C_1$. Based on (12) $\Delta V$ can be calculated with:

$$\Delta V = \frac{I_{\text{sink}} (K \cdot T_{\text{clk}})}{C_1}.$$  

(14)

During $S_1$ time, the load current is supplied by $C_L$, thus, $\Delta V$ can be also expressed as:

$$\Delta V = \frac{i_L(t)}{C_L} \Delta t.$$  

(15)

Now, substituting (14) in (15) gives:

$$i_L(t) = C_L \cdot \frac{I_{\text{sink}} (K \cdot T_{\text{clk}})}{C_1 \cdot \Delta t}.$$  

(16)

DC block capacitors are used to isolate the DC voltage level of the DC-DC converter and the current sensor to be able to use a low voltage process to sense high voltage applications. This is possible because the sensor uses only the voltage ripple information (AC signal) to estimate the current. To obtain an accurate value of current, it
is required to pay attention to the comparator offset and the voltage divider between the DC block capacitor and the sampling capacitor. Adding the voltage divider to the formula results in the following relation:

$$i_L(t) \cong C_L \frac{I_{\text{sink}}(K \cdot T_{\text{clk}})}{C_1 \cdot \Delta t} \left( \frac{C_{\text{block}} + C_1}{C_{\text{block}}} \right)$$

where $C_1 = C_2$ (any mismatch have to be calibrated at the assembling of the system). In addition, the hold capacitor has to be selected so that $kT/C_1$ is less than the minimum desired input offset. The comparator offset tuning can be done by just employing the auto zero technique used in [56] or output offset storage technique as implemented in this work. In addition to this, all the values in (17) are constant, except $K$. Therefore, for applications that require only a value proportional to the flowing current, (10) can be reduced to:

$$i_L(t) \propto K .$$

4.2 SENSOR POWER LOSSES

The power losses of the IDC are be divided in two groups: (1) sensing losses and (2) quiescent losses. The sensing losses, is the power consumed in the sensing operation and depend on the sensed current level. The quiescent losses are associated to the power used to bias the comparator and digital circuits. The quiescent losses are not related to the sensed current level.

For the sensing losses, when the cycle start at $t_0$ both switches $\phi_1$ and $\phi_2$ are closed to follow the output voltage. If the connection of $\phi_1$ and $\phi_2$ is performed when the output
voltage is close to $V_2$, the boost’s output voltage and the sampling capacitors voltage will be similar. Therefore, the power loss to charge the sampling capacitors can be neglected.

After sampling ($t_2$ to $t_3$) the capacitor $C_1$ is discharged by a constant current source ($I_{\text{sink}}$) until the voltage at $C_1$ becomes $V_2$. This energy loss of the capacitor $C_1$ can be represented as follows [60]:

$$E_{C1,\text{loss}} = \int_{t_2}^{t_3} V_{C1}(t)I_{\text{sink}} \, dt = \frac{(V_2 - V_1)I_{\text{sink}}}{2} t_{\text{discharge}}$$ (19)

The value of (19) is normally in the order of the 1 to 2 pico-Joule with the proper selection of components. The reminder of the power dissipated on the sensor circuit can be considered quiescent power. In the IDC circuit the quiescent power losses dominated the power consumption of the devise. Table 4-1 show the total power, size and breakdown voltage of the IC used for a sample of the typical current sensors for a current of 830mA sitting at 12V. To use a standard CMOS IC (5V or less) in a 12V system, the size of the sensor typically increases, but the IDC achieves this function with a minimum size and power consumption.

Table 4-1: Comparison of current sensors for a maximum current of 830mA sitting at 12V.

<table>
<thead>
<tr>
<th>Method</th>
<th>Power (mW)</th>
<th>Size (mm$^2$)</th>
<th>CMOS Process Voltage</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resistor</td>
<td>~ 60.3 – 107.4</td>
<td>78</td>
<td>&gt;20V</td>
<td>20mΩ resistor</td>
</tr>
<tr>
<td>Current Transformer</td>
<td>~ 41.3 – 82.8</td>
<td>140</td>
<td>5</td>
<td>1:20 turn ratio</td>
</tr>
<tr>
<td>Hall Effect</td>
<td>~ 187 – 379</td>
<td>420</td>
<td>5</td>
<td></td>
</tr>
<tr>
<td>IDC</td>
<td>~ 18.1</td>
<td>8</td>
<td>5</td>
<td></td>
</tr>
</tbody>
</table>
CHAPTER 5

CIRCUITS AND SIMULATION

This chapter discusses the circuits used to implement the sub-panel MPPT and the IDC. The discussion contains the specifications, design and simulation of the individual parts of the system. For safety, the power level of the panels and the system are smaller than the typical panels used for residences. The next sections will give the details on the circuits design: (1) photovoltaic source, (2) DC-DC converter and (3) the current sensor.

5.1 PHOTOVOLTAIC SOURCE

The goal of this research is to power the system with a solar panel. For testing, low power panels were selected to reduce the risks and hazards during the testing process. The panels used are rated for 5V and 1A at MPP, but higher current was desired to increase the test range of the current sensor. Therefore, the converter was designed for two panels in parallel (twice current). The I-V curve of the two combined panels for the test is presented in Figure 5-1. A summary of the parameters of the solar panels is given in Table 5-1. Based on these parameters the converter was designed.

![I-V curve for two parallel panels (each rated at 5V and 1A).](image)

Figure 5-1: I-V curve for two parallel panels (each rated at 5V and 1A).
Table 5-1: Characteristics of two parallel panels.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Efficiency</td>
<td>16.5%</td>
</tr>
<tr>
<td>Maximum Power Point Voltage ($V_{MPP}$)</td>
<td>4.00V</td>
</tr>
<tr>
<td>Maximum Power Point Current ($I_{MPP}$)</td>
<td>2.05A</td>
</tr>
<tr>
<td>Open Circuit Voltage ($V_{OC}$)</td>
<td>5.20V</td>
</tr>
<tr>
<td>Short Circuit Current ($I_{SC}$)</td>
<td>2.31A</td>
</tr>
<tr>
<td>Size</td>
<td>7.87 x 6.38 in</td>
</tr>
</tbody>
</table>

5.2 DC-DC CONVERTER

The converter was designed to test the sub-panel MPPT architecture and the current sensor. The specifications are displayed in Table 5-2. They were selected in accordance with the solar panel described in Section 5.1 and the requirements of a typical PV system. A 12V output will give power to most portable electronic as well as to automotive applications. In addition, the behavior recorded for this power level can be easily scaled for higher powers.

Table 5-2: Sub-panel system specifications.

<table>
<thead>
<tr>
<th>No.</th>
<th>Parameter</th>
<th>Value</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Power Supply ($V_{DD}$)</td>
<td>5V</td>
<td>Based on Agilent Power Supply in Lab.</td>
</tr>
<tr>
<td>2</td>
<td>Input Voltage ($V_{in}$)</td>
<td>5V</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Maximum Input Voltage ($V_{in_{max}}$)</td>
<td>6V</td>
<td>Based in $V_{OC}$</td>
</tr>
<tr>
<td>4</td>
<td>Input Voltage Ripple ($\Delta V_{in}$)</td>
<td>0.25V</td>
<td>5% $V_{in}$ at MPPT</td>
</tr>
<tr>
<td>5</td>
<td>Output Voltage ($V_{0}$)</td>
<td>12V</td>
<td>2.4X Boost</td>
</tr>
<tr>
<td>6</td>
<td>Frequency ($f_s$)</td>
<td>200kHz</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Input Current ($I_{in}$)</td>
<td>2A</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Inductor Current Ripple ($\Delta I_{L}$)</td>
<td>1.45A</td>
<td>71% of $I_{in}$</td>
</tr>
<tr>
<td>9</td>
<td>Maximum Input Current ($I_{in_{max}}$)</td>
<td>3A</td>
<td>Based in $I_{SC}$</td>
</tr>
<tr>
<td>10</td>
<td>Output Current ($I_{out}$)</td>
<td>0.833A</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>Output Voltage Ripple ($\Delta V_{0}$)</td>
<td>1.34V</td>
<td>11% of $V_{0}$</td>
</tr>
</tbody>
</table>
Converter Topology

The converter requirements are: small component values, few components and low voltage stress for the switches. Figure 5-2 shows the schematic of the selected topology: a boost convert. Boost converters requires few components as well as provides a simple design. The step up range is small for this case, but it will help to show the advantages of the sub-panel topology (compared to Figure 3-4).

![Converter Circuit Schematic](image)

Figure 5-2: Boost converter circuit schematic.

The design equations for the converter are as follows:

- **Output Voltage** ($V_0$):

  \[ V_0 = \frac{V_{in}}{1 - D} \]  \hspace{1cm} (20)

- **Inductor** ($L$) size for a given load:

  \[ L_{max} = \frac{R_L \times D \times (1 - D)^2}{2 f_s} \]  \hspace{1cm} (21)

  or:

  \[ L_{min} = \frac{V_0 \times D \times (1 - D)}{\Delta I_L \times f_s} \]  \hspace{1cm} (22)

- **Output Capacitor** ($C_0$) for a given output voltage ripple ($\Delta V_0$):

  \[ C_0 = \frac{V_0 \times D}{f_s \times \Delta V_0 \times R_L} \]  \hspace{1cm} (23)
Input Capacitor ($C_{in}$) for a given input voltage ripple ($\Delta V_{in}$):

$$C_{in} = \frac{\Delta I_L}{8 \times f_s \times \Delta V_{in}} = \frac{D \times V_{in}}{8 \times f_s^2 \times \Delta V_{in} \times L}$$

(24)

where, $V_{in}$ is the input voltage, $D$ is the duty cycle, $f_s$ is the switch frequency, and $R_L$ is the load of the converter.

**Converter Simulation**

The final step of the converter design was the selection of specific component values and simulation. In the process, the inductance $L$, input capacitor $C_{in}$ and output capacitor $C_L$ values were selected.

To select the inductance, its value was varied to test the effect on the efficiency and input current ripple, as shown in Figure 5-3. The simulations show that a good efficiency is maintained for inductances above 10 $\mu$H, because the ripple is maintained low. As the inductance increases more than 10 $\mu$H, the efficiency continues increasing but the increase rate is negligible. Therefore, a good tradeoff between high efficiency and small inductor value can be achieved for a 10 $\mu$H. The capacitors $C_L$ and $C_{in}$ were calculated using (23) and (24), respectively, based on the values displayed in Table 5-2.

The next step was to fix the expected maximum current and voltage at the output of the converter. The converter will be used to maximize the power of a solar panel. The maximization creates a peak in the output voltage that corresponds to the PV maximum power point (for linear load). The level of the peak voltage varies with the load value. Figure 5-4a illustrates how the converter output voltage varies for different load values. From these simulations, a maximum output voltage of 32V was obtained with a load of
100Ω. In addition, it can be observed that if the load value is small, as in the case of 1Ω, the MPP cannot be achieved by the circuit. Figure 5-4b shows the load current for small values of loads. In this case, the components have to be selected to handle at least 2A.

Figure 5-3: Effect of inductance. (a) Efficiency. (b) Input current ripple. (c) Match efficiency and ripple at 10µH.
Table 5-3 shows the values of the components calculated for the converter. The frequency of operation for the converter was selected as 200kHz to reduce the components size. This frequency provides a small value for the components and good efficiency.

Table 5-3: Components values calculated for $V_{in} = 5V$, $V_0 = 12V$, $I_{in} = 2A$, and $I_0 = 0.83A$

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_{in}$</td>
<td>3.63 µF</td>
<td>$\Delta V_{in} = 0.25V$</td>
</tr>
<tr>
<td>$L$</td>
<td>10 µH</td>
<td>$\Delta I_L = 1.45A$</td>
</tr>
<tr>
<td>$C_L$</td>
<td>1.81 µF</td>
<td>$\Delta V_0 = 1.34V$</td>
</tr>
<tr>
<td>$R_L$</td>
<td>14.4 Ω</td>
<td></td>
</tr>
</tbody>
</table>
The converter was simulated, using the parameters in Table 5-3. In the simulation, a PV sub-panel was used as input source. Power FETs of 8mΩ ON resistance were used. Losses due to effective series resistance (ESR) from the capacitors and inductor were included. The test results are shown in Figure 5-5. The figure demonstrates that all the parameters stay inside the desired specifications. The input voltage waveform shows a ripple of 25mV with a DC value of 5V. The inductor current is 2A with a ripple of 1.45A and the output voltage is approximately 12V with a ripple of 1.34V.

![Graphs of Input Voltage, Inductor Current, and Output Voltage](image)

Figure 5-5: Transients results of the boost converter using the values in Table 5.3.

5.3 CURRENT SENSOR CIRCUIT

The current-to-digital converter (IDC) sensor was implemented in a 5V, 0.7μm, 3 level-metal CMOS technology. The top level diagram of the current sensor is shown in
Figure 5-6. This current sensor architecture can be divided in two sections: the front end (switches, capacitors and current source) and the comparator (pre-amps, latch).

Figure 5-6: Top level schematic of the current sensor.

Sensor Specifications

The IDC was implemented to sense the output current of the boost converter (output parameters of 12V and 832mA). The target specifications are listed in Table 5-4. The sensor will provide an 8 bits output that represent a sensed current range of 832 mA with a minimum sensed value of 3.25 mA. The converter is driven by a PWM signal with frequency \( f_s = 200\text{kHz} \). The sampling time (\( \Delta t_{\text{sample}} \)) used for the sensor is 10% of the period (500\( \mu \text{s} \)). Finally, the minimum detectable voltage change (\( \Delta V \)) is targeted to be 1 mV.

Table 5-4: Specifications of the Current-to-Digital converter circuit.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>8 bits</td>
</tr>
<tr>
<td>Full Scale Current</td>
<td>832 mA</td>
</tr>
<tr>
<td>LSB</td>
<td>3.25 mA</td>
</tr>
<tr>
<td>DNL</td>
<td>&lt; 1 LSB</td>
</tr>
<tr>
<td>INL</td>
<td>&lt; 1 LSB</td>
</tr>
<tr>
<td>Clock Frequency (f_{clk})</td>
<td>10 MHz</td>
</tr>
<tr>
<td>Sampling time (( \Delta t_{\text{sample}} ))</td>
<td>500 ns</td>
</tr>
<tr>
<td>Minimum (( \Delta V ))</td>
<td>1 mV</td>
</tr>
</tbody>
</table>
Sensor Front End

The sensor front end is composed by the sample stage and the current source as shown in Figure 5-6. At the input of the IDC, two DC block capacitors are used. For this design, the DC block capacitors are external to the IC. External capacitors allow the selection of devices with dielectric breakdown voltage above the boost output voltage. The value of these capacitors is considerably larger than the internal sampling caps ($C_{\text{block}}$ is much larger than $C_1$ and $C_2$) to decrease the effect of the voltage divider between the caps.

In the process of sampling, feed-through will occur. The feed-through is the result of the fast transient in the digital sampling signal. To decrease this effect, CMOS transmission gates were used. The transmission gates use complementary control signals that result in a reduction of the feed-through effect. The capacitors are differentially connected to the comparator. If the sampling switches are matched, the same amount of additional charges will enter both caps. Therefore, feed-through will be rejected as common mode noise.

The sampling capacitors and current source ($I_{\text{sink}}$) were selected based in the equations presented in Chapter 4 and the specifications in Table 5-4. A cascaded current source was used to reduce the voltage dependence on the current value. The current source is enabled/disabled by controlling the biasing point of the cascaded transistor. The selected capacitors and current source values are shown in Table 5-5.
Synchronous Comparator

The comparator architecture used for the current sensor is shown in Figure 5-7. The comparator controls the counter and the conversion time. As can be observed from the figure, it is composed of two stages: (1) offset compensated pre-amplifier and (2) the decision stage (latch). The pre-amplifiers are used to increase the gain and to reduce the input referred offset of the latch. This preamp uses an output storage offset cancelation to minimize the input referred offset. The latch circuit provides large gain to the comparator.

![Block diagram of comparator used for the current sensor.](image)

The latch is a positive feedback circuit that produces high gain. Latch comparators produce a fast large output variation (typically rail-to-rail). This fast swing occurs in the internal nodes and, typically, couples through the parasitic capacitance of the transistors to the input of the latch. Since the circuit preceding the latch does not have

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>$C_1$</td>
<td>10 pF</td>
</tr>
<tr>
<td>$C_2$</td>
<td>10 pF</td>
</tr>
<tr>
<td>$C_{\text{block}}$</td>
<td>1 μF</td>
</tr>
<tr>
<td>$I_{\text{sink}}$</td>
<td>100 nA</td>
</tr>
</tbody>
</table>
zero output impedance, the signal couples back to its input. This distortion is called kickback and it affects the accuracy of the comparator.

Figure 5-8 shows the latch circuit used in this design. This circuit contains a pre-amp, a positive feedback stage and a differential to single ended buffer. Transistors mismatches are present in the different stages of this latch circuit. These mismatched results in an offset in the comparator. The offset of the designed latch was simulated using a Monte Carlo simulation (see Figure 5-9). This simulation indicates that the designed latch has an offset of \( V_{\text{OS-Latch}} = 64 \text{ mV} \) (3 sigma). To decrease the input referred offset of the comparator a pre-amplifier has to be added.

The pre-amplifier gain is selected to maintain the input referred offset below the spec of 1mV. The calculation of the input referred offset (\( V_{\text{OS}} \)) is as follows:

\[
V_{\text{OS}} = V_{\text{OS-Pre-Amp}} + \frac{V_{\text{OS-Latch}}}{A_{\text{Pre-Amp}}}
\]  

(25)

where \( V_{\text{OS-Pre-Amp}} \) and \( A_{\text{Pre-Amp}} \) are the offset voltage and gain of the pre-amplifier, respectively. The offset of the pre-amplifier is compensated with the offset storage technique; thus it is neglected for the analysis (\( V_{\text{OS-Pre-Amp}} \approx 0V \)). To reduce the latch offset voltage below 1mV the gain of the pre-amplifier has to be above 64 V/V.
Figure 5-8: Latch circuit with pre-amplification [61].

Figure 5-9: Monte Carlo simulation to test the offset of the latch. The 3 sigma offset is 64 mV.

The pre-amplifier design targets a gain above 70V/V. The output offset cancelation requires a low gain amplifier to avoid saturation on the offset storage cycle (A < 10 V/V). For the offset cancelation, a 10MHz clock is used, which requires a large bandwidth amplifier. Figure 5-10 shows the amplifier selected for the pre-amplifier. This circuit provides a fully differential amplifier with internal common mode feedback and easy gain control. To achieve the bandwidth, the gain of the pre-amplifier was decreased.
to 3 V/V as shown in Figure 5-11. Due to the low gain, four pre-amplifiers are cascaded reaching a gain of approximately 81 V/V. From equation (25), the combined input referred offset of the comparator (pre-amp + latch) is 0.79 mV.

![Pre-amplifier circuit schematic.](image)

**Figure 5-10:** Pre-amplifier circuit schematic.

![Gain and phase of the pre-amplifier.](image)

**Figure 5-11:** Gain and phase of the pre-amplifier.

The input of the pre-amplifier has switches for the output offset storage. In every offset cancelation cycle, the switches inject charges to the sampling capacitors distorting
the stored voltage. To avoid this distortion, an instrumentation amplifier with gain of 3V/V was used to buffer, or isolate, these two nodes (Figure 5-12). This stage (instrumentation amplifier) will now dominate the comparator offset. The offset of the instrumentation amplifier depends on the matching of the transistors, current, resistor, etc. This offset is difficult to be reduced under the desired specs. Figure 5-13 shows the offset obtained after optimization of the instrumentation amplifier.

Figure 5-12: Instrumentation amplifier schematic.

Figure 5-13: Monte Carlo simulation to test the instrumentation amplifier’s offset.
A board with the boost DC-DC converter and current sensor IC was implemented to characterize the performance of the proposed system, as shown in Figure 6-1. A panel of 15W was used for the test (15V and 1A). The boost converter performs the MPPT at the sub-panel level (5V). The specifications of the boost converter are listed in Table 6-1. The current sensor IC is connected to the output of the converter to sense the output current, as illustrated in Figure 6-1c. The proposed current-to-digital converter was designed and fabricated on a 5V, 0.7 μm, 3 metallization-layer CMOS technology (Figure 6-1b). The testing was divided in three parts:

1. **Current sensor characterization:** In this test, the current sensor performance was tested under a controlled environment (voltage, temperature and boost converter load were controlled). This allows the correct characterization of the linearity, offset and other parameters of the IDC.

2. **Indoor PV test:** This test characterizes the PV system on the lab. Performing the test in a lab allows controlling the shading and temperature of the panels. The board was connected to do MPPT to a panel with two sub-panels as well as for the individual sub-panels.

3. **Outdoor PV Test:** The system was tested under real environment to verify it can provide the correct power optimization. In this test, the panel and sub-panel optimization were examined and compared in real conditions.

The test, results and analysis will be explained in the following sections.
Figure 6-1: Prototype board used to characterize the IDC IC and test MPPT. (a) Block diagram of the board. (b) Photo of the IDC IC. (c) Photo of the Board.
Table 6-1: Specifications of the prototype boost converter.

<table>
<thead>
<tr>
<th>No.</th>
<th>Parameter</th>
<th>Value</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>Power Supply ($V_{DD}$)</td>
<td>5V</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>Input Voltage ($V_{in}$)</td>
<td>5V</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>Output Voltage ($V_{out}$)</td>
<td>12V</td>
<td>2.4x Boost</td>
</tr>
<tr>
<td>4</td>
<td>Frequency ($f$)</td>
<td>200kHz</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>Input Current ($I_{in}$)</td>
<td>2A</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>Input Current Ripple ($\Delta I_{in}$)</td>
<td>1 – 4A</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>Output Current ($I_{out}$)</td>
<td>0.833A</td>
<td></td>
</tr>
<tr>
<td>8</td>
<td>Output Voltage Ripple ($\Delta V_{out}$)</td>
<td>1.34V</td>
<td>Based on Current sensor IC</td>
</tr>
</tbody>
</table>

6.1 CURRENT SENSOR CHARACTERIZATION

The current sensor characterization uses an input DC source for the boost converter. The use of a DC source allows a controlled characterization of the current sensor and the DC-DC converter. The converter circuit was designed to boost 5V to 12V with a switching frequency of 200 kHz, $C_L = 1.8$ µF and a load of 14.4 Ω. For the IDC, a clock of 10MHz was used in the comparator and in the 8 bits counter. The values of the DC block ($C_{block}$) and sensing ($C_1$, $C_2$) capacitors were 1uF and 10pF, respectively. The sampling time was 500ns from the sampling in $C_1$ to $C_2$. The selected values allows a least-significant-bit (LSB) resolution of 3.24 mA.

Two DC sources were connected to the input of the current sensor to characterize the offset of the comparator. The characterization consists in keeping a constant voltage at the non-inverting input of the comparator and varying the voltage of the inverting input until the output state changes. This test was repeated for supply voltages of 4.5V to 5.5V, as shown in Figure 6-2. The offset of the comparator is 3 mV for a power supply voltage of 5V. This offset can be now compensated later on the digital controller.
The next step was to test the current sensor, using the boost converter with an input DC source. In this test, the input of the boost converter is set to 5V and the duty-cycle is adjusted to get an output voltage of 12V with a load of 14.4Ω (i_L = 833mA). Figure 6-3 shows the measured waveforms of the current sensor. Figure 6-3a shows the voltage ripple at the output of the DC block capacitor (C_{block}, 2.5V common mode). This ripple contains the information of the load current of the DC-DC converter. Figure 6-3b illustrates the sampling signals \( \phi_1 \) and \( \phi_2 \). The time difference between these two signals define the time \( \Delta t = 500\text{ns} \), where the voltage ripple is sampled. The sampling of the voltage ripple in the capacitors (\( C_1 \) and \( C_2 \)) and the discharge time of capacitor \( C_1 \) are shown in Figure 6-3c. The comparator changes state to stop the counter 28\( \mu \text{s} \) after \( \phi_2 \) (when the voltages at \( V_{C1} = V_{C2} \)), as shown in Figure 6-3d.
Figure 6-3: Transient measurement of the current sensor. (a) Voltage ripple after the DC block capacitor (2.5V common mode). (b) Sampling signals ($\phi_1$ and $\phi_2$). (c) Voltage on the capacitors $C_1$ and $C_2$. (d) Output signal of the comparator.
Then, the load current \( (i_L) \) was varied from 0A to full-scale (FS = 830mA). The output digital code was recorded to test the linearity of measurements. The measured and estimated currents versus the digital output code are presented in Figure 6-4. Based on these results, the differential non-linearity (DNL) of the converter was extracted. Figure 6-5a demonstrates that a DNL of less than half LSB is achieved by the proposed current to digital converter. The IDC achieves an integral-non-linearity (INL) of less than one LSB as shown in Figure 6-5b. This result verifies that the converter maintains an accurate output over the FS.

![Figure 6-4: Response of the 8 bits counter output due to variation in current. The figure compares the measured results and the values estimated using an ideal output.](image)

The small error in the DNL and INL metrics are due to the quantization errors of the discrete sampling time, the time constant (between the sampling capacitor and the switch ON resistance), switches charge injection, and other random measurement errors.
Figure 6-5: Measured IDC performance. (a) DNL. (b) INL

After that, the sensing power consumption of the IDC (capacitor charge transfer) was compared to the resistor based method ($I^2R$ losses), excluding any peripheral (ADC, amplifiers, etc.), as shown in Figure 6-6. As shown in Figure 6-6, the power consumed by sensing with the IDC is in the order of the nW, while the resistor sensor consumption is in mW (around 5 orders of magnitude larger).
Figure 6-6: Power dissipation of current sensor using a 20 mΩ resistor sensor and the IDC (Note: y-axis is in logarithmic scale).

The total power dissipation of the IDC (including peripherals) was measured for various boost regulator’s output voltage and current levels. A constant power of 27mW was dissipated for all the cases. This result shows that the power dissipation of the proposed sensor is dominated by the quiescent power and is not dependent on the sensed system’s voltage or current levels, which is not the case of other current sensors (i.e., resistor sensor).

6.2 INDOOR PV TEST

In the indoor PV test, DC sources and controlled light were used to characterize the board and MPPT control. An indoor controlled environment allows debugging the system to ensure a constant and predictable behavior. Two main measurements were performed in this test: (1) boost DC-DC converter efficiency, (2) MPPT for two series connected sub-modules.
To test the efficiency of the boost converter, the input was connected to a constant 5V power supply. The load of the converter was varied to sweep the power processed by the device from full load to no-load. Figure 6-7 shows the measured efficiency. The efficiency stays above 94% for load greater than 5W.

![Efficiency vs Power](image)

Figure 6-7: Efficiency of the boost DC-DC converter.

The configuration used to test the MPPT control is shown in Figure 6-8. In this test, the MPPT is performed using the output parameters of the converter, as shown in Figure 6-8a. The system consists of the PV panel, boost DC-DC converter, voltage and current sensors, and the digital control. The test setup shown in Figure 6-8b consists in the artificial light source, dimmer (to simulate shading), solar panel and prototype board.
The processing for this MPPT circuit consists of a perturb-and-observe (P&O) method, shown in Figure 6-8a [62, 63]. The output parameters \( V_0(n) \) and \( I_0(n) \) are measured and the power \( P_0(n) \) is calculated. The calculated power and duty cycle are
compared with their respective previous states [i.e., \( P_0(n) > P_0(n-1) \) and \( D(n) > D(n-1) \)]. Based on the present state, the algorithm decides the new duty-cycle \([D(n-1) + \Delta D\) or \(D(n-1) - \Delta D]\) to optimize the output power of the system.

The system was tested to ensure it can correctly perform the MPPT. Figure 6-9 displays the results of the output MPPT algorithm using the proposed current sensor. The I-V curves were taken using a Daystar DS-100C I-V Curve Tracer [64] and the power operating point of the converter was captured using an oscilloscope (Tektronix TDS7104). The graph includes the I-V curve of the panel for two incident light intensities (0% shade and 50% shade). The yellow cloud shows the operating point achieved by the system. In the two cases, the proposed system tracks correctly the maximum power points of the PV input.

![Graph showing I-V curves for two incident light intensities](image)

Figure 6-9: Test of the output MPPT algorithm using the proposed current sensor.

The sub-panel MPPT was tested using two sub-panels. The two configurations under test are shown in Figure 6-10. Two tests were used to compare the MPPT at both
levels of optimization. The first test provides the full light to both sub-panels and is called no-shade. The second test shades the sub-panel PV 1 by 50% and is called shade. Figure 6-11 shows the results for this test.

For the case of no shade, the Panel level optimization gives more power than the sub-panel one. This result is because the PV is giving the same power to both configurations, but the sub-panel optimization has more losses (two converters). However, the difference in power between both configurations is only 0.01W (~ 0.12%).

For the second case (shade), the sub-panel level optimization provides 38% more power than the panel level optimization. The reason is that the sub-panel level optimization is able to optimize the power in the shaded sub-panel (PV 1) and the panel level optimization just bypasses the shaded PV, losing all its power.

Figure 6-10: Indoor MPPT test. (1) Panel optimization. (b) Sub-panel level optimization.
Figure 6-11: Measured result of indoor MPPT test. (a) Panel level optimization. (b) Sub-panel level optimization.

6.3 OUTDOOR PV TEST

The system was characterized under a real environment to validate the results obtained in the lab. The test setup for this test is shown in Figure 6-12. The setup has a PV panel that contains three sub-panels, the converter and the test equipment. The test will demonstrate how the output MPPT works under real conditions and will also compare the panel and sub-panel level optimization systems. The outdoor test will include various shading levels to ensure the system can follow the maximum power point.

Figure 6-12: Outdoor MPPT test setup. (a) Panels and test equipment. (b) Optimizer prototype boards.
The prototype board was used to test the MPPT control with the proposed current sensor. Four shading patterns were used for this test (0%, 13%, 40% and 50% shade). Figure 6-13 shows the I-V curves and the measured output power for each shading condition. The results show that the proposed system accurately follows the maximum power point under various shading conditions.

Figure 6-13: Prototype measurements using output MPPT employing the IDC sensor over five shading cases. (a) I-V curve. (b) Power vs. voltage curve.
A panel with three sub-panels was used to test and compare the performance of the proposed system outdoor. The two setups used in this test were the panel level optimization and the proposed sub-panel level optimization (similar to the indoor setup), as shown in Figure 6-14. The panel level uses a single converter to optimize the power of the entire panel. The sub-panel level system removes the bypass diodes and optimizes the power of each sub-panel circuit.

![Diagram](image)

Figure 6-14: Outdoor MPPT test setup. (a) Panel level MPPT. (b) Sub-panel level MPPT.

Five shading patterns were used to test the two PV optimization systems, as shown in Figure 6-15. The maximum output power was recorded for both systems under each case. The cases under study were the following:

1. No-shade: This means that the three sub-panels were unshaded.
2. Sub-Panel 1 (25% Shade): This test shades only sub-panel 1 by 25%. Sub-panels 2 and 3 are unshaded.
3. **Sub-Panel 2 (65% Shade):** This test shades only sub-panel 2 by 65%. Sub-panels 1 and 3 are unshaded.

4. **Sub-Panel 3 (50% Shade):** This test shades only sub-panel 3 by 50%. Sub-panels 1 and 2 are unshaded.

5. **Sub-Panel 1 (25%) & Sub-Panel 3 (50%) Shade:** This test shades sub-panel 1 by 25%, sub-panel 3 by 50%. Sub-panel 2 unshaded.

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![Graphs showing I-V curves](image)

**Figure 6-15:** I-V curve of the three sub-panels. The graphs show the I-V curves of the three sub-panels under no shade and shade conditions.
The results for the five shading patterns were recorded for both optimization systems. Figure 6-16 shows the results of the panel level optimization. When shading is applied to the panel level system, the shaded sub-panel limits the performance of the unshaded sub-panels. If the shading is high enough the bypass diodes short the shaded sub-panels. This causes the power of the shaded sub-panel to be lost.

Figure 6-16: Results of the panel level optimization for all the shading patterns. (a) IV curve. (b) Power vs. voltage curve.
The transient output power levels for the panel and sub-panel optimization systems (for all the test cases) are shown in Figure 6-17. These measurements show that as the shading increases the sub-panel level MPPT produce higher power than the panel level MPPT. The information in Figure 6-17 is summarized in Figure 6-18. The summarized information shows that in an unshaded system the panel optimization has fewer losses (~ 2% more output power) than the proposed system. But, as the shading increases the additional power overcome the losses and gives an improvement of up to 20% more output power.

![Image](a)

![Image](b)

Figure 6-17: Results of optimization under partial shading. (a) Panel level optimization. (b) Sub-panel level optimization.
Figure 6-18: Output power for the panel and sub-panel optimization systems for different shading patterns. (a) Comparison of output power. (b) Power as shading increase in a single sub-panel and percentage of improvement of sub-panel vs. panel MPPT.
CHAPTER 7

CONCLUSIONS AND RECOMMENDATIONS

This dissertation introduces an improved MPPT system and a low loss standard CMOS current sensor. The system was tested in a low power PV panel, which can easily be scaled to high power applications. In this chapter, the conclusion and the recommendations for future improvements of the system and tests will be discussed.

7.1. CONCLUSIONS

A sub-panel level optimization system and a current to digital converter were presented. These two combined systems represent a step toward the integration of the power optimizer for PV systems to a single IC. The sub-panel level optimization reduces the power levels per converter and the current sensor was integrated and tested for this application.

The proposed current-to-digital sensor uses standard CMOS, dissipates low power and allows high common mode range sensing. This fully integrated circuit uses a charge based current sensing method that allows high voltage sensing with standard CMOS process. The sensor produces accurate sensing output, has high efficiency and requires a small number of components and area. The IDC gives a direct digital output and can be integrated to a digitally controlled system without the need of complex ADC. The sensor is a standard CMOS circuit that can be used for DC-DC converters and other high-voltage applications including DC motor control, buck/boost converters, regulators, rectifiers, and inverters without the need for high-voltage process. Measurements for a current range from 0 to 830mA showed accuracy of 99.6% with DNL of less than half
The sensor was successfully integrated to a PV system for MPPT.

The sub-panel level optimization together with the proposed current sensor improves the optimization under partial shading by up to 20%. The sub-panels produce lower power compared to the panel. This power reduction allows relaxing the power stress of the system components. The boosting of the output voltage allows the reduction of the output current and parallel connection of the panels. The sub-panel level MPPT follows closely the maximum available power with a converter efficiency of around 90% to 95%.

The use of this architecture enables: (1) use of relaxed specifications for the individual converters (eliminate transformers and electrolytic capacitors.), (2) reduction in voltage/power stress for components, (3) improve the power generated under partial shading and other mismatches, (4) allows the parallel connection of panels for simpler and modular system expansion, (5) improve the reliability of each converter, and (6) improve the availability of the system (if one converter fails, only 1/3 of the panel’s power is lost).

The converter and current sensor presented in this research provide a first step toward the integration of the PV system. They accurately sense and follow the MPPT of the panels and reduce the power handling to facilitate this integration.

7.2. RECOMENDATIONS

This research proposed a sub-panel level MPPT system which reduces the complexity and power stress on each converter. The used prototype proves the concept
with a low power panel. A current sensor was also introduced and tested to verify its performance. To improve the system and the testing, few more steps are recommended:

1. Build the complete system with the boost double lift converter and the partial power processing converter in a single board. This will allow having the correct conversion ratio and regulated output.

2. This new system will allow a comprehensive cost and efficiency analysis.

3. Design and test the sub-panel MPPT converter for the typical residential panels (180 W).

4. Second step of integration of the sub-panel system. Integration of the drivers, control, sensors and peripherals in the same IC. This will result in a significant reduction of the sizes and price of each converter.

These steps will allow the optimization of the system to reduce its area and costs. The reduction in costs and size will make this system economically affordable for future commercialization.
REFERENCES


