DC Optimizer for PV Module

by

Daniel Luster

A Thesis Presented in Partial Fulfillment
of the Requirements for the Degree
Master of Science

Approved November 2014 by the
Graduate Supervisory Committee:

Raja Ayyanar, Chair
Bertan Bakkaloglu
Sayfe Kiaei

ARIZONA STATE UNIVERSITY

December 2014
ABSTRACT

As residential photovoltaic (PV) systems become more and more common and widespread, their system architectures are being developed to maximize power extraction while keeping the cost of associated electronics to a minimum. An architecture that has become popular in recent years is the “DC optimizer” architecture, wherein one DC-DC converter is connected to the output of each PV module. The DC optimizer architecture has the advantage of performing maximum power-point tracking (MPPT) at the module level, without the high cost of using an inverter on each module (the "microinverter" architecture). This work details the design of a proposed DC optimizer. The design incorporates a series-input parallel-output topology to implement MPPT at the sub-module level. This topology has some advantages over the more common series-output DC optimizer, including relaxed requirements for the system’s inverter. An autonomous control scheme is proposed for the series-connected converters, so that no external control signals are needed for the system to operate, other than sunlight. The DC optimizer in this work is designed with an emphasis on efficiency, and to that end it uses GaN FETs and an active clamp technique to reduce switching and conduction losses. As with any parallel-output converter, phase interleaving is essential to minimize output RMS current losses. This work proposes a novel phase-locked loop (PLL) technique to achieve interleaving among the series-input converters.
# TABLE OF CONTENTS

<table>
<thead>
<tr>
<th>LIST OF TABLES</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>v</td>
</tr>
<tr>
<td>LIST OF FIGURES</td>
<td>vi</td>
</tr>
<tr>
<td>CHAPTER</td>
<td></td>
</tr>
<tr>
<td>1 INTRODUCTION AND THESIS OUTLINE</td>
<td>1</td>
</tr>
<tr>
<td>1.1 Introduction to Photovoltaic Energy Conversion</td>
<td>1</td>
</tr>
<tr>
<td>1.2 Thesis Objective and Outline</td>
<td>7</td>
</tr>
<tr>
<td>2 PV CELL MODELING</td>
<td>9</td>
</tr>
<tr>
<td>2.1 Brief Description of PV Cell Operation</td>
<td>9</td>
</tr>
<tr>
<td>2.2 Modeling PV Cell</td>
<td>11</td>
</tr>
<tr>
<td>2.3 Bypass Diodes and 72-Cell PV Module</td>
<td>17</td>
</tr>
<tr>
<td>3 ARCHITECTURES FOR RESIDENTIAL PV SYSTEMS</td>
<td>20</td>
</tr>
<tr>
<td>3.1 Introduction</td>
<td>20</td>
</tr>
<tr>
<td>3.2 Common Architectures for Residential PV Systems</td>
<td>20</td>
</tr>
<tr>
<td>3.3 Recent Developments in DC Optimizers</td>
<td>24</td>
</tr>
<tr>
<td>4 SUB-MODULE MPPT</td>
<td>26</td>
</tr>
<tr>
<td>4.1 Introduction to Sub-Module MPPT</td>
<td>26</td>
</tr>
<tr>
<td>4.2 Calculation of Power Gain for Real Module</td>
<td>28</td>
</tr>
<tr>
<td>5 PROPOSED DC OPTIMIZER AND CONTROL ARCHITECTURE</td>
<td>32</td>
</tr>
<tr>
<td>5.1 Proposed DC Optimizer</td>
<td>32</td>
</tr>
<tr>
<td>5.2 Derivation of Proposed Converter</td>
<td>33</td>
</tr>
<tr>
<td>5.3 Effect on System</td>
<td>39</td>
</tr>
</tbody>
</table>
CHAPTER 5.4 Proposed Control Circuit Architecture ............................................. 41

6 EFFICIENCY IMPROVEMENT WITH ACTIVE CLAMP ................................. 45

   6.1 Energy Loss in Flyback Converter ....................................................... 45
   6.2 Steady-state Operation of Active Clamp Flyback Converter ................. 47
   6.3 Derivation of Design Constraints ....................................................... 54
   6.4 Stability of Clamp Voltage ............................................................... 60

7 EFFICIENCY IMPROVEMENT WITH GAN FETS ....................................... 65

   7.1 Introduction ...................................................................................... 65
   7.2 eGaN FET Properties ................................................................. 67
   7.3 Design of Gate Driver for Q1 ......................................................... 67
   7.4 Design of Gate Driver for Q2 ......................................................... 70

8 POWER STAGE CALCULATIONS ................................................................. 71

   8.1 Outline of Calculations ................................................................. 71
   8.2 Input Voltage and Current Change .............................................. 71
   8.3 Choice of Switching Frequency, Duty and Turns Ratio ............. 70
   8.4 Selection of Leakage Inductance Llk and Magnetizing Inductance Lm .... 73
   8.5 Selection of Ccl ............................................................................. 77

9 MODELING AND SIMULATION OF ACTIVE CLAMP FLYBACK ............ 79

   9.1 Discussion on Modeling and Simulation ................................... 79
   9.2 PWL Model of PV Sub-Module ..................................................... 79
   9.3 Model of GaN FET ........................................................................ 83
   9.4 Model of Flyback Transformer .................................................. 86
<table>
<thead>
<tr>
<th>CHAPTER</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>9.5 Model of PWM Block and Gate Driver</td>
<td>87</td>
</tr>
<tr>
<td>9.6 Complete Circuit</td>
<td>88</td>
</tr>
<tr>
<td>9.7 Simulation Waveforms</td>
<td>89</td>
</tr>
<tr>
<td>10 PHASE-LOCKED LOOP FOR CONVERTER INTERLEAVING</td>
<td>95</td>
</tr>
<tr>
<td>10.1 Desire for Phase Interleaving</td>
<td>95</td>
</tr>
<tr>
<td>10.2 Typical Interleaving Technique with PWM Synchronization</td>
<td>98</td>
</tr>
<tr>
<td>10.3 Timing Pin on ISL8130</td>
<td>98</td>
</tr>
<tr>
<td>10.4 Proposed Phase-Locked Loop</td>
<td>99</td>
</tr>
<tr>
<td>10.5 Simulation of PLL</td>
<td>101</td>
</tr>
<tr>
<td>11 DISCUSSION AND CONCLUSIONS</td>
<td>106</td>
</tr>
<tr>
<td>REFERENCES</td>
<td>108</td>
</tr>
</tbody>
</table>
# LIST OF TABLES

<table>
<thead>
<tr>
<th>TABLE</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>2.1 Solar Module Specifications</td>
<td>12</td>
</tr>
<tr>
<td>2.2 Comparison of Actual and Modeled PV Values</td>
<td>17</td>
</tr>
<tr>
<td>6.1 Summary of Design Constraints</td>
<td>64</td>
</tr>
</tbody>
</table>
## LIST OF FIGURES

<table>
<thead>
<tr>
<th>FIGURE</th>
<th>Page</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.1 Worldwide PV Capacity (Taken from [2])</td>
<td>1</td>
</tr>
<tr>
<td>1.2 Agua Caliente Solar Project</td>
<td>2</td>
</tr>
<tr>
<td>1.3 United States PV Installations by Sector (Taken from [4])</td>
<td>3</td>
</tr>
<tr>
<td>1.4 Neighborhood with PV Installations</td>
<td>4</td>
</tr>
<tr>
<td>1.5 PV System Architectures (a) Central Inverter, (b) String Inverters, (c) Microinverters, (d) DC Optimizers</td>
<td>5</td>
</tr>
<tr>
<td>1.6 Tigo Energy DC Optimizer for Smart Modules</td>
<td>6</td>
</tr>
<tr>
<td>1.7 Major Companies in the MLPE Sector (Taken from [7])</td>
<td>7</td>
</tr>
<tr>
<td>2.1 Operation of PV Cell</td>
<td>10</td>
</tr>
<tr>
<td>2.2 Diode Model (a) Using Ideal Diode Equation, (b) Using Modified Gummel-Poon Model</td>
<td>13</td>
</tr>
<tr>
<td>2.3 PV Cell Schematics</td>
<td>14</td>
</tr>
<tr>
<td>2.4 Power Versus Voltage for PV Cell Models</td>
<td>15</td>
</tr>
<tr>
<td>2.5 Current Versus Voltage for PV Cell Models</td>
<td>16</td>
</tr>
<tr>
<td>2.6 Hotspot Heating</td>
<td>18</td>
</tr>
<tr>
<td>2.7 72-Cell PV Module with Three Bypass Diodes</td>
<td>19</td>
</tr>
<tr>
<td>3.1 Central Inverter</td>
<td>20</td>
</tr>
<tr>
<td>3.2 String Inverter</td>
<td>21</td>
</tr>
<tr>
<td>3.3 Microinverter</td>
<td>22</td>
</tr>
<tr>
<td>3.4 DC Optimizers with (a) Series-Connected Outputs, (b) Parallel-Connected Outputs</td>
<td>23</td>
</tr>
<tr>
<td>3.5 Tigo’s Patented Impedance Matching DC Optimizer</td>
<td>24</td>
</tr>
<tr>
<td>FIGURE</td>
<td>Page</td>
</tr>
<tr>
<td>---------------------------------------------------------------------</td>
<td>------</td>
</tr>
<tr>
<td>3.6 Parallel-Ladder Current-Shuffling DC Optimizer</td>
<td>25</td>
</tr>
<tr>
<td>3.7 Synchronous Buck Converters at Sub-Module Level</td>
<td>25</td>
</tr>
<tr>
<td>4.1 Using Simplified Diode Model to Visualize Mismatch of Series Cells</td>
<td>26</td>
</tr>
<tr>
<td>4.2 Power extraction from Two Series Strings of PV Cells with (a) Minimum Current, (b) Use of Bypass Diode, (c) Sub-Module MPPT</td>
<td>27</td>
</tr>
<tr>
<td>4.3 Power Extraction from Three Series Strings of PV Cells (a) at Minimum Current, (b) One Bypass Diode Conducting, (c) Two Bypass Diodes Conducting, (d) Using Sub-Module MPPT</td>
<td>28</td>
</tr>
<tr>
<td>4.4 Power Extraction During Mismatch Scenario 1</td>
<td>29</td>
</tr>
<tr>
<td>4.5 Power Extraction During Mismatch Scenario 2</td>
<td>30</td>
</tr>
<tr>
<td>5.1 Series-Input Parallel-Output Flyback Converter</td>
<td>32</td>
</tr>
<tr>
<td>5.2 Input Voltage Shorted to (a) Output Voltage, (b) Ground</td>
<td>34</td>
</tr>
<tr>
<td>5.3 Series-Input Isolated Converters with (a) Series-Connected Outputs, (b) Parallel-Connected Outputs</td>
<td>35</td>
</tr>
<tr>
<td>5.4 Stages of Converter Turn-Off. (a) Normal Conditions, (b) Capacitor Forced to Zero, (c) Capacitor Forced Negative, (d) Output Diode Forward Biased</td>
<td>38</td>
</tr>
<tr>
<td>5.5 DC Optimizers connected in parallel</td>
<td>40</td>
</tr>
<tr>
<td>5.6 Control Architecture</td>
<td>41</td>
</tr>
<tr>
<td>5.7 Using UVLO to Turn On/Off Converter with Sunlight</td>
<td>43</td>
</tr>
<tr>
<td>6.1 Flyback Converter</td>
<td>45</td>
</tr>
<tr>
<td>6.2 Flyback Converter with RCD Clamp</td>
<td>46</td>
</tr>
<tr>
<td>6.3 Active Clamp Flyback Converter with (a) High-Side Clamp, (b) Low-Side Clamp</td>
<td>47</td>
</tr>
<tr>
<td>FIGURE</td>
<td>Page</td>
</tr>
<tr>
<td>--------</td>
<td>------</td>
</tr>
<tr>
<td>6.4</td>
<td>48</td>
</tr>
<tr>
<td>6.5</td>
<td>49</td>
</tr>
<tr>
<td>6.6</td>
<td>50</td>
</tr>
<tr>
<td>6.7</td>
<td>50</td>
</tr>
<tr>
<td>6.8</td>
<td>51</td>
</tr>
<tr>
<td>6.9</td>
<td>52</td>
</tr>
<tr>
<td>6.10</td>
<td>53</td>
</tr>
<tr>
<td>6.11</td>
<td>54</td>
</tr>
<tr>
<td>6.12</td>
<td>55</td>
</tr>
<tr>
<td>6.13</td>
<td>56</td>
</tr>
<tr>
<td>6.14</td>
<td>57</td>
</tr>
<tr>
<td>6.15</td>
<td>57</td>
</tr>
<tr>
<td>6.16</td>
<td>59</td>
</tr>
<tr>
<td>6.17</td>
<td>61</td>
</tr>
<tr>
<td>6.18</td>
<td>62</td>
</tr>
<tr>
<td>7.1</td>
<td>65</td>
</tr>
<tr>
<td>7.2</td>
<td>66</td>
</tr>
<tr>
<td>7.3</td>
<td>68</td>
</tr>
<tr>
<td>7.4</td>
<td>68</td>
</tr>
<tr>
<td>7.5</td>
<td>69</td>
</tr>
<tr>
<td>7.6</td>
<td>70</td>
</tr>
<tr>
<td>8.1</td>
<td>73</td>
</tr>
<tr>
<td>FIGURE</td>
<td>Page</td>
</tr>
<tr>
<td>-----------------------------------------------------------------------</td>
<td>------</td>
</tr>
<tr>
<td>8.2 EPC2001 (a) Output Capacitance Curves (b) with Equivalent Coss Values</td>
<td>74</td>
</tr>
<tr>
<td>9.1 24 Series Cells in Simetrix.........................................................</td>
<td>80</td>
</tr>
<tr>
<td>9.2 24-Cell V/I Measurement..................................................................</td>
<td>81</td>
</tr>
<tr>
<td>9.3 Values for PWL Model of PV Sub-Module..........................................</td>
<td>81</td>
</tr>
<tr>
<td>9.4 EPC2001 Capacitance Curves............................................................</td>
<td>82</td>
</tr>
<tr>
<td>9.5 PWL Capacitance Calculations..........................................................</td>
<td>83</td>
</tr>
<tr>
<td>9.6 Body Diode Curve..............................................................................</td>
<td>83</td>
</tr>
<tr>
<td>9.7 PWL Body Diode Values.....................................................................</td>
<td>84</td>
</tr>
<tr>
<td>9.8 Approximation of Threshold Voltage and Gain....................................</td>
<td>84</td>
</tr>
<tr>
<td>9.9 PWL Resistor to Model Gate Current...............................................</td>
<td>85</td>
</tr>
<tr>
<td>9.10 EPC2001 Subcircuit Text...............................................................</td>
<td>86</td>
</tr>
<tr>
<td>9.11 Schematic Symbol for EPC2001........................................................</td>
<td>86</td>
</tr>
<tr>
<td>9.12 Flyback Transformer Model..............................................................</td>
<td>87</td>
</tr>
<tr>
<td>9.13 PWM and Gate Drive Block.............................................................</td>
<td>88</td>
</tr>
<tr>
<td>9.14 Complete Power Stage Model...........................................................</td>
<td>88</td>
</tr>
<tr>
<td>9.15 POP Trigger in Simplis....................................................................</td>
<td>89</td>
</tr>
<tr>
<td>9.16 Vin and Ipv.................................................................................</td>
<td>90</td>
</tr>
<tr>
<td>9.17 Current Waveforms and Clamp Voltage Waveform...................................</td>
<td>90</td>
</tr>
<tr>
<td>9.18 Q1 Voltages and Currents...............................................................</td>
<td>91</td>
</tr>
<tr>
<td>9.19 ZVS on Q1......................................................................................</td>
<td>92</td>
</tr>
<tr>
<td>9.20 Q2 Waveforms...............................................................................</td>
<td>93</td>
</tr>
<tr>
<td>9.21 ZVS on Q2......................................................................................</td>
<td>94</td>
</tr>
<tr>
<td>FIGURE</td>
<td>Page</td>
</tr>
<tr>
<td>----------------------------------------------------------------------</td>
<td>------</td>
</tr>
<tr>
<td>10.1 Parallel-Connected Flyback Converters</td>
<td>96</td>
</tr>
<tr>
<td>10.2 Output Currents Added Without Interleaving</td>
<td>97</td>
</tr>
<tr>
<td>10.3 Output Currents Added With Interleaving</td>
<td>97</td>
</tr>
<tr>
<td>10.4 Typical Synchronization Method (Taken from [26])</td>
<td>98</td>
</tr>
<tr>
<td>10.5 Timing Resistance from ISL8130 Datasheet</td>
<td>99</td>
</tr>
<tr>
<td>10.6 Proposed PLL</td>
<td>100</td>
</tr>
<tr>
<td>10.7 PLL Schematic in Simplis</td>
<td>101</td>
</tr>
<tr>
<td>10.8 Transformation of Timing Graph into PWL Resistor Model</td>
<td>102</td>
</tr>
<tr>
<td>10.9 Zoomed in Schematic of Equivalent Non-Linear VCO</td>
<td>103</td>
</tr>
<tr>
<td>10.10 Delay Block in Simplis</td>
<td>103</td>
</tr>
<tr>
<td>10.11 PLL During Lock</td>
<td>104</td>
</tr>
</tbody>
</table>
CHAPTER 1. INTRODUCTION AND THESIS OUTLINE

1.1 Introduction to Photovoltaic Energy Conversion

Photovoltaic (PV) energy conversion involves direct conversion of sunlight into electricity. This form of energy conversion, once used primarily for providing power to remote places such as space satellites, has become a popular source of electric energy for a variety of reasons. PV is a low-maintenance energy source as it involves no moving mechanical parts, but the high cost of producing a PV cell had kept PV an impractical source of energy for many years. Things have changed in recent years, as dropping production costs for PV cells and modules have coincided with government initiatives to promote the use of PV. The government initiatives have been a big reason for PV’s recent proliferation; one example is the U.S. Residential Renewable Energy Tax Credit, which provides a tax credit in the amount of 30% of the cost of installation [1]. This boost makes PV a competitive option for power generation; the result has been a massive growth in PV use worldwide over the last ten years [2], as seen in Figure 1.1.
The utility sector has seen the most growth. In the United States, California represents the biggest contributor to the utility sector as it ramps up the use of renewable energy to meet the California Renewables Portfolio Standard, which states that the utilities shall have 33% of their retail sales derive from renewable energy sources by the end of 2020 [3]. Agua Caliente Solar Project, seen in Figure 1.2, has a peak capacity of 290 MW and ships all of this electricity to California from Dateland, AZ.
The residential sector has seen tremendous growth as well. Figure 1.3 shows the PV installations by sector in the United States over the last four years [4].

![Figure 1.3 United States PV Installations by Sector (Taken from [4])](image)

Each of the sectors has more installations every single year, and the residential sector comprises a significant portion of these installations. The fact that there has been significant growth in the residential sector speaks to the scalability of PV projects, which can be as small as one rooftop module. Figure 1.4 shows an example of a neighborhood with a high use of PV.
As the PV installations grow in the residential sector, there are more and more companies competing in the market, and they are developing new methods of installation to optimize the balance between system cost and system efficiency. In particular, the architectures for these rooftop systems have been evolving. Central inverters are the baseline architecture used in commercial-scale and utility-scale PV installations, but are not commonly used in residential installations. String inverters have been used for many years in the residential sector, but recently module-level power electronics (MLPE) have been added to systems to increase the amount of power extracted. MLPE comes in two flavors: microinverters and DC optimizers. These architectures are shown below in Figure 1.5.
Figure 1.5 PV System Architectures (a) Central Inverter, (b) String Inverters, (c) Microinverters, (d) DC Optimizers

Microinverters and DC optimizers allow for greater power extraction, but they come at a higher system cost due to the proliferation of electronics. This higher cost has not stopped the MLPE industry from growing rapidly [5]. Over the last two years, MLPE companies have been partnering with original equipment manufacturers (OEMs) to embed DC optimizers and microinverters into the PV modules (typically in the junction box) so that the consumer can purchase a so-called “smart module” directly from the
OEM. A big player in this market is Tigo Energy, whose DC optimizer (shown below in Figure 1.6) can be found embedded in modules from at least nine different OEMs [6].

Figure 1.6 Tigo Energy DC Optimizer for Smart Modules

A GTM Research study on the MLPE sector found that, by the end of 2013, approximately 2GW of installed PV capacity used MLPE. Figure 1.7 below shows the major companies in the sector, with Tigo Energy, SolarEdge, and Enphase representing about 88% of 2013 installed capacity [7].
1.2 Thesis Objective and Outline

The objective of this thesis work is the detailed design of a DC optimizer (DC-DC converter) appropriate for a residential-scale PV module. The converter is tailored for modules in the 150-200W range, based on panels that were donated to the LightWorks research initiative at Arizona State University.

The outline of the thesis is as follows: Chapter 2 describes the operation of the PV cell, with the goal of deriving the concept of maximum power-point tracking (MPPT) and deriving a PV cell model appropriate for circuit-level simulations. Chapter 3 introduces the three popular types of residential PV architectures. Chapter 4 introduces the concept of sub-module MPPT and its potential for efficiency gains. Chapter 5 presents the proposed topology, a series-input parallel-output flyback converter, as well as the architecture used for its control circuitry. Chapter 6 describes an improvement in
efficiency by using an active clamp technique. Design constraints for the active clamp
circuit are derived for steady-state conditions. Chapter 7 describes the design of the
converter’s gate drive circuitry, which uses gallium-nitride (GaN) FETs to improve
efficiency. Chapter 8 details the complete power stage calculations. Chapter 9 details the
modeling and simulation of the active clamp flyback converter. Chapter 10 describes a
phase-locked loop circuit developed to achieve interleaving in the outputs of the parallel-
connected converters.
CHAPTER 2. PV CELL MODELING

2.1 Brief Description of PV Cell Operation

Every semiconductor material has a “bandgap”, which refers to the energy difference between the valence energy band and conduction energy band. Electrons in the valence band are attached to nuclei and cannot move freely, while at room temperature a very small of electrons will be thermally excited to the conduction band and are free to move about the material [8].

If a photon of light collides with a valence electron, and if the photon has energy greater than the bandgap, it can transfer its energy to the electron and create an electron-hole pair. This electron-hole pair will wander briefly and then recombine.

A pn junction is used to separate the electron-hole pair. If the photon transfers its energy in the vicinity of the pn junction’s depletion region, the electron and hole may wander into the depletion region and quickly be swept into the n- and p-regions, respectively. Here they become majority carriers and can contribute to current flow. If the pn junction, aka diode, is open-circuited, then the majority carrier buildup will lead to a higher diffusion current. The voltage across the depletion region will grow until the diffusion and drift currents balance. Conceptually we may think of the light as a current source, and with no external connection, all of that current is dissipated in the diode, or it is forward-biased. This is referred to as the open circuit voltage of the PV cell. On the other hand, if we apply a short across the cell terminals, the drift current will have the potential to move all the way through the diode to the external wire. In this case, the voltage across the depletion region will reduce to zero. This is referred to as the short
Somewhere between these two cases is the point where the maximum possible power can be extracted from the cell. This is called the maximum power-point (MPP). It occurs at the so-called “knee” of the diode. The operation is summarized in Figure 2.1 below.

Silicon is the most commonly used material for PV cells, due to its ubiquity (for many years solar cells were made from scrap wafers from the IC industry), and due to the fact that it has a “native oxide”: SiO2 will grow naturally on heated Si, and acts as a very good insulator. Silicon also has a bandgap which lies very close to the peak of the Shockley-Quiesser limit, which theoretically derives the maximum efficiency of a solar cell based on its bandgap [9].
When photons reach the surface of the semiconductor, they will penetrate a certain depth before generating an electron-hole pair. Typically, most of the generation happens very close to the surface, and the rate of generation quickly decays exponentially into the material [10]. For this reason the pn junction is placed very close to the surface, on the order of a few micron. Unfortunately, recombination is also highest at the surface. The dangling bonds of the lattice edge allow electrons to quickly recombine, therefore the surface is passivated, usually with a layer of SiO2 [11]. As it turns out, the n-type material is easier to passivate, so the n-type material is placed on top, facing the sun. The current must flow through metal wires to reach an external circuit, so conductors are connected to the top and bottom of the cell. The conductors on the top use thin fingers, as a tradeoff between resistance and blocking sunlight.

2.2 Modeling PV Cell

Since a PV cell is essentially a diode, modeling the PV cell begins with the ideal diode equation:

\[ I_{pv} = I_s (1 - e^{\frac{q}{nkt}}) \]

Here, \( I_s \) is the reverse saturation current, also called the dark saturation current, which arises from the very small amount of thermally generated conduction electrons. \( kT/q \) is the so-called thermal voltage, which is 25.8mV at room temperature. \( I_{pv} \) therefore has a logarithmic change with temperature. "n" is the ideality factor, which is used to model the ideality of the diode. The ideality factor \( n \) is equal to 2 at very low bias voltages in
the mV range, and it is due to the high-level of generation-recombination current inside the depletion region at low biases [12]. Since PV cells are always biased near the “knee” of the diode, we may assume n=1. Apart from the ideal diode equation, each cell has series resistance, due to the finger connectors and external wiring, and shunt resistance, which is due to defects in the cell itself. Because the cells are large in area, having some small defects is an accepted part of their construction [13].

Solar modules were donated to ASU’s LightWorks research group, and their specifications are shown below in Table 2.1.

<table>
<thead>
<tr>
<th>Manufacturer</th>
<th>Jiawei</th>
<th>Baisheng</th>
<th>Silicon Solar</th>
</tr>
</thead>
<tbody>
<tr>
<td>Rated power</td>
<td>175W</td>
<td>175W</td>
<td>180W</td>
</tr>
<tr>
<td>Voltage @ MPP</td>
<td>36.8V</td>
<td>35.7V</td>
<td>36.2V</td>
</tr>
<tr>
<td>Current @ MPP</td>
<td>4.77A</td>
<td>4.9A</td>
<td>4.97A</td>
</tr>
<tr>
<td>Open-circuit voltage</td>
<td>44.1V</td>
<td>44V</td>
<td>44.3V</td>
</tr>
<tr>
<td>Short-circuit current</td>
<td>5.49A</td>
<td>5.27A</td>
<td>5.76A</td>
</tr>
<tr>
<td>Number of cells</td>
<td>72</td>
<td>72</td>
<td>72</td>
</tr>
</tbody>
</table>

Table 2.1 Solar Module Specifications

A figure-of-merit for solar modules is the fill factor (FF), which is the ratio of maximum power to the product of open-circuit voltage and short-circuit current. For these panels, we get the following fill factors:

\[
\text{Jiawei: } FF = 36.8 \times \frac{4.77}{44.1 \times 5.49} = 0.725
\]
Baisheng: \( FF = 35.7 \times \frac{4.9}{44 \times 5.27} = 0.754 \)

Silicon Solar: \( FF = 36.2 \times \frac{4.97}{44.3 \times 5.76} = 0.705 \)

For this thesis work, the Jiawei panel was chosen to model because its FF lies in the middle of these three panels.

A model was derived in Simetrix, using the ideal diode equation from above with \( n=1 \) and with series and shunt resistances added. Values were tuned to match well with the Jiawei panel.

Figure 2.2  Diode Model (a) Using Ideal Diode Equation, (b) Using Modified Gummel-Poon Model
Figure 2.2 shows two approaches to modeling the diode. In Fig.2.2 (a), the ideal diode equation is used as a voltage-controlled current source, with the only parameters being temperature and saturation current, which was tuned to 200pA. In Fig.2.2 (b), a standard library model using a Gummel-Poon charge-based model [14] has all of its parameters set to default (by being blank) except $I_s=200pA$. The schematics for these two diode models in the full PV cell model are shown in Figure 2.3 below.

Figure 2.3  PV Cell Schematics
Here we can see the tuned values. $I_{sc} = 5.49\, \text{A}$ (per module specifications), $R_{series} = 0.006\, \text{ohm}$, $R_{shunt} = 1.2\, \text{ohm}$. $R_{shunt}$ is a small value which accurately represents the average defects in the cells, and accounts for the low fill factor of 0.725. Higher-quality modules (as well as new ones from Jiawei) have fill factors from 0.8 to 0.85.

The voltage sources on the right side of the schematic perform a voltage sweep, and the boxes calculate the power for plotting. The results of both voltage sweeps are plotted on top of each other below, to demonstrate the good matching between the models.

![Figure 2.4 Power Versus Voltage for PV Cell Models](image-url)
From Figure 2.4, we see that both cells reach MPP at 0.514V, and in Figure 2.5, at a voltage of 0.514V we have a current of 4.75A. Also, we see that the current crosses zero at a voltage of 0.6166V. This is the open-circuit voltage.

To compare the PV cell model to the actual Jiawei panel, we must divide the voltage ratings on the panel by 72 to get the numbers for a single cell. The numbers are compared below in Table 2.2.
<table>
<thead>
<tr>
<th></th>
<th>Jiawei</th>
<th>Simetrix model</th>
</tr>
</thead>
<tbody>
<tr>
<td>Isc (input to model)</td>
<td>5.49A</td>
<td>5.49A</td>
</tr>
<tr>
<td>Voc</td>
<td>0.613V</td>
<td>0.617V</td>
</tr>
<tr>
<td>Imp</td>
<td>4.77A</td>
<td>4.75A</td>
</tr>
<tr>
<td>Vmp</td>
<td>0.511V</td>
<td>0.514V</td>
</tr>
</tbody>
</table>

Table 2.2  Comparison of Actual and Modeled PV Values

We see that the models match very well. This can allow us to examine different operating points of the PV module to better design the conversion circuitry.

2.3 Bypass Diodes and 72-Cell PV Module

The modules studied in this work are a typical size for residential use, with 72 series cells and three bypass diodes. The bypass diodes are installed for the module’s safety, to prevent so-called “hotspot heating” in the cells. This condition arises under mismatch conditions, where one cell is unable to pass current while the other cells are highly illuminated. If the output voltage is low enough, the shaded cell can reverse bias, from KVL around the loop. The situation is shown in Figure 2.6. Hotspot heating occurs when the shaded cell becomes reverse biased and dissipates the energy generated in the other cells. If the output voltage is held low this can be a problem, as:

\[ V_m = V_{string} - V_1 - V_2 - \cdots - V_n \]
The solution is to use bypass diodes. In the case of extreme mismatch, the current has the ability to bypass a cell or string of cells. Figure 2.7 shows the modules under study, of which we have chosen the Jiawei module to model closely. There are three bypass diodes, which cover 24 cells each. These diodes are connected in the module’s junction box.
Figure 2.7 72-Cell PV Module with Three Bypass Diodes
CHAPTER 3. ARCHITECTURES FOR RESIDENTIAL PV SYSTEMS

3.1 Introduction

In this chapter we discuss the architectures commonly employed for residential PV systems. Comparing the different architectures is not a simple task, as there are many factors to balance when designing a PV system, among them cost of installation, cost of maintenance, system efficiency, solar power extraction, and system reliability. After a brief comparison of architectures, the DC optimizer architecture is discussed in further detail to set the appropriate background for the design in this work.

3.2 Common Architectures for Residential PV Systems

3.2.1 Central Inverter

![Figure 3.1 Central Inverter](image)
Figure 3.1 shows the schematic of a central inverter. They historically have been used in large installations, where it is convenient to have all of the electronics in one location. Strings of panels are connected in series to add to large voltages, and these strings are connected in parallel using blocking diodes as shown in Figure 3.1. Although central inverters are usually the most practical option for large-scale systems due to the ease of maintenance, they become less practical as PV systems become smaller, due to the fact that mismatch in the PV modules can severely restrict power output. Each string of modules will source the current of its weakest module, and the total system voltage will be determined by the weakest string. However, if mismatch problems are not deemed a problem, the central inverter can be a practical solution [15].

3.2.2 String Inverter
Figure 3.2 shows the schematic of a pair of string inverters. The string inverter has historically been the most popular option for residential PV systems, where one inverter can support a rooftop system on the order of 1-10 kW. MPPT is performed at the string level, and multiple strings can easily be added in parallel. Similar to central inverters, the major disadvantage is that mismatch effects within each string will force the string to either operate at the weakest module’s current, or bypass that module entirely. Bypass diodes can lead to local power maxima, so global MPPT algorithms must be implemented [16]-[18].

3.2.3 Microinverter

![Microinverter diagram](image)

Figure 3.3 Microinverter

The microinverter architecture, as shown in Figure 3.3, involves using a single inverter for each PV module. This structure allows for MPPT at the module level, so that mismatch effects will not affect power extraction of the producing modules. This architecture is also popular for its plug-and-play flexibility; since each microinverter will output an AC voltage, a system can use as many or as little modules as desired.
Microinverters involve a lot of electronics—the most of any PV architecture. For this reason, initial costs for a system are higher. Moreover, maintenance can be costly, as the microinverters can be hard to access once installed.

3.2.4 DC Optimizer

![Diagram of DC Optimizers with (a) Series-Connected Outputs, (b) Parallel-Connected Outputs](image)

Figure 3.4 DC Optimizers with (a) Series-Connected Outputs, (b) Parallel-Connected Outputs

Figure 3.4 shows the DC optimizer architecture. “DC optimizer” is a trade name for a DC-DC converter that performs MPPT. They strike a balance between the distributed MPPT of the microinverter architecture and the centralized inversion of the string inverter architecture. Here we still make use of a string inverter, except that mismatch effects are no longer a problem. The DC optimizer has emerged as a good alternative to the microinverter architecture due to the reduced parts count, and the design of efficient DC optimizers has become a very active area of research.
3.3 Recent Developments in DC Optimizers

Tigo Energy, as mentioned in the introduction, makes DC optimizers as add-on circuitry for PV modules. Tigo Energy has a patent on a circuit topology that they use in their DC optimizers. The patent can be found online [19], and the circuit’s equivalent schematic is reproduced below in Figure 3.5. It uses an impedance matching circuit to perform MPPT.

![Figure 3.5 Tigo’s Patented Impedance Matching DC Optimizer](image)

Figure 3.6 shows a novel topology proposed in [20]. It uses resonant switched-capacitor DC-DC converters, connected in a parallel-ladder structure as shown, to regulate at MPP via a current shuffling method. In this method, the converters only handle mismatch current. Therefore, if the modules are all operating under equal conditions, the converter will shut off and 100% efficiency is achieved.
In [21], the approach taken is to maximize cost and efficiency of the DC-DC converters, and they propose using cheap and efficient synchronous buck converters and achieving voltage gain by using series-connected modules. The miniature design is shown in Figure 3.7 below.
CHAPTER 4. SUB-MODULE MPPT

4.1 Introduction to Sub-Module MPPT

The last two circuits mentioned in Chapter 3 make use of sub-module MPPT, which is a growing trend among new DC optimizers. Sub-module MPPT involves performing DC-DC conversion on portions of the cells in a DC module. With current module construction, there are typically four electrical connections to the cells, and the bypass diodes are connected there. Therefore the connections can be used to place three DC-DC converters. To convert at a finer scale would require changes to PV module construction. To understand sub-module conversion, it helps to consider the V/I curve for series cells using the simplified diode model. In Figure 4.1, two strings of PV cells with different short circuit current levels are connected in series. The series connection means that we add the values on the V/I plots horizontally.

![Figure 4.1 Using Simplified Diode Model to Visualize Mismatch of Series Cells](image)

With this simplified model, local MPP maxima occur at the “knees” of the simplified diodes. If we imagine that the module has no bypass diodes, the converter will regulate at the local MPP of the smaller current. Having a bypass diode gives the option of
regulating at the other local maximum, at the knee of the higher current. With sub-module more power is extracted, as shown in Figure 4.2.

Figure 4.2 Power Extraction from Two Series Strings of PV Cells with (a) Minimum Current, (b) Use of Bypass Diode, (c) Sub-Module MPPT

With sub-module MPPT we can extract the power represented by the areas in Figure 4.2 (c). Not only to we gain power extraction using this method, but the MPPT algorithm can be simplified, as there is no longer a need to search for a global maximum. The local maximum is the global maximum for a single string of cells.

The situation in our case is three series strings of PV cells, and in this case the typical MPPT algorithm will have up to three local maxima to choose from, depending on how many bypass diodes are conducting. Sub-module MPPT avoids this problem while extracting power from all three segments, as shown in Figure 4.3.
4.2 Calculation of Power Gain for Real Module

By using the accurate PV cell model derived in Chapter 2 (based on the panel by Jiawei), we can examine the power gains during various operating conditions. A key part of the calculations is observable in Figure 4.3. If we are operating at the knee of the diode for the minimum current, the voltage at that point is equal to Vmp for the weak string plus the voltage of the other strings at that current. We must measure these points on our PV diode model.
A MATLAB script was created to calculate power extraction under different lighting scenarios. Values of short circuit current $I = 5.5A, 3A,$ and $1A$ were used with the diode model derived in Chapter 2 to calculate precisely what the voltages and currents are at the local maxima, and during sub-module MPPT.

In one scenario, we suppose the three strings are operating at $I_{sc1} = 5.5A,$ $I_{sc2} = 3A,$ and $I_{sc3} = 1A.$ An excerpt from the MATLAB script showing the calculations is shown below.

```matlab
% first scenario. one sub-module at each Isc: 5.5A, 3A, 1A
P_min_current = Imp3*(Vmp3 + V1_at_Imp3 + V2_at_Imp3);
P_single_bypass = Imp2*(Vmp2 + V1_at_Imp2);
P_double_bypass = Imp1*Vmp1;
P_submodule_mppt = Imp1*Vmp1 + Imp2*Vmp2 + Imp3*Vmp3;
```

The results are plotted in Figure 4.4 below.
Figure 4.4  Power Extraction During Mismatch Scenario 1

In the next scenario, we let Isc1 = 5.5A, Isc2 = Isc3 = 1A.

An excerpt from the MATLAB script is shown below.

```matlab
% second scenario. one sub-module at Isc = 5.5V, the others at 1A
P_min_current2 = Imp3*(Vmp3 + Vmp3 + V1_at_Imp3);
P_double_bypass2 = Imp1*Vmp1;
P submodule_mppt2 = Imp1*Vmp1 + 2*Imp3*Vmp3;
```

The results are shown below in Figure 4.5 (note that there is one less local maximum due to Isc2 and Isc3 being equal).

![Figure 4.5  Power Extraction During Mismatch Scenario 2](image)
In scenario 2, the double bypass power is close to the sub-module MPPT power due to the fact that two of the strings are sourcing very little power, and bypassing them gains almost all the power. This is a useful tool for analyzing power gains with sub-module MPPT, but its accuracy is limited by the accuracy of the PV diode model used.
CHAPTER 5. PROPOSED DC OPTIMIZER AND CONTROL ARCHITECTURE

5.1 Proposed DC Optimizer

The proposed DC optimizer is shown in Figure 5.1. It is a series-input parallel-output flyback converter. The output voltage is in the range of 200V, appropriate for the input voltage of a single-phase inverter. Conceptually, we may think of removing each
bypass diode from the original module and replacing it with a flyback converter, and then placing the outputs of these flyback converters in parallel. In the following sections we discuss the derivation of the converter and its advantages over a typical DC optimizer.

5.2 Derivation of Proposed Converter

5.2.1 Input Capacitors

As we have seen, the voltage/current characteristics of a PV cell (or string of cells) approach those of a DC current source. We desire to maintain the cells operating at or near their MPP, but if we attach a DC-DC converter to the cells’ terminals, we can expect to draw discontinuous currents from the cells, or currents with large amounts of ripple. During segments of the switching period where input current is zero, the cells are briefly open circuited, and the PV current will be absorbed in the cells as it forward biases the diodes.

What we desire is to decouple the DC PV power from the switching action of the DC-DC converter. The solution is to use large capacitors, which will supply the discontinuous and/or ripple current to the converter, while allowing the DC current to flow from the cells. If the capacitors are large enough, the voltage across the cells’ terminals will stay roughly constant over a switching period. Essentially, this converts a current source to a voltage source, from which we can theoretically use any well-known DC-DC converter.

For a properly rated capacitor, there is no danger of overvoltage conditions, due to the fact that the cells can only supply current up to their Voc limit. If the DC-DC
converter is shut off during daylight conditions, the PV current source will continue to charge the capacitors until Voc is reached, when all of the current will then flow through the PV diodes. Therefore the value of Voc can be used to select the voltage rating of the capacitors.

5.2.2 Necessity for Isolation

As a first attempt to select an appropriate DC-DC converter, we may consider using a simple boost converter, as we will be stepping up the PV voltage to 200V. This leads to a huge problem, as shown below in Figure 5.2.

![Figure 5.2 Input Voltage Shorted to (a) Output Voltage, (b) Ground](image)

Here we see the result of stacking two boost converters. The problem comes from the fact that the inputs are connected together. In Fig. 5.2 (a), the outputs of the converters are connected in series. This leads to the input voltage of the lower converter being shorted to its own output, as a result of the ground node of the upper converter. In Fig. 5.2 (b), the outputs are connected in parallel. Here the result is different but equally devastating, as the upper converter’s ground node shorts the lower converter’s input to
ground. This problem does not exist in the typical DC optimizer scheme, where there is one converter per module, and nothing forcing us to connect together the inputs of the modules.

This same problem exists for all of the major non-isolated DC-DC converters, due to the existence of the ground node. This forces us to use transformer isolation.

5.2.3 Series Versus Parallel Outputs

Next, we consider the differences between series-connected and parallel-connected outputs, given the fact we will be using isolated converters. Figure 5.3 shows the two configurations.

![Diagram](image)
These two options both solve the problem encountered with non-isolated converters. For the series-connected converters, the output voltages sum to 200V, and the output currents are all equal. For the parallel-connected converters, the output voltages are all equal to 200V, and the output currents sum to equal $I_{out}$ for the whole converter. At first glance, the series-connected configuration might seem better due to the smaller turns ratio. The input voltages will be in the 12V range, and in the parallel case they will be stepped up to 200V, where in the series-connected case, the voltages will ideally be stepped up to $200V/3 = 67V$. A smaller turns ratio will improve efficiency, but there are some problems with the series-connected output configuration which makes it less attractive in this application.

5.2.4 Problems with Series-Connected Outputs

Using series-connected outputs is advantageous when all converters are operating under similar lighting conditions. However, we are using sub-module conversion in order to gain power output, so we must consider cases where there are mismatch effects. For example, consider a case where sub-module 1 receives full sunlight, with $I_{mp} = 5A$, $V_{mp} = 12V$, and the other two modules receive much less sunlight, on the order of $I_{mp} = 1A$, $V_{mp} = 11V$. We can calculate the output voltage of converter 1 as follows:

$$Total\ power = \sum (V_{mp} * I_{mp}) = 5 * 12 + 1 * 11 + 1 * 11 = 82W$$
Output current \( = \frac{82W}{200V} = 410mA \)

Converter 1 output voltage \( = V_{mp} \times \frac{I_{mp}}{I_{out}} = 5 \times \frac{12}{0.41} = 146.3V \)

We see that under mismatch conditions, the converter with more power will be forced to regulate at a much higher output voltage than under ideal conditions. In the extreme case of two converters being completely cut off from sunlight, one converter will regulate at the full output voltage of 200V. Each converter must be designed to regulate over a very wide range. This will lead to the converters having a much smaller duty ratio at the ideal operating point where \( V_{out} = 67V \).

There is another problem with using series-connected outputs for this application. When sunlight is low, the converters will eventually turn off. It is desirable, for the purpose of maximum power extraction, that the converters be able to turn on and off independently. If one converter is receiving sunlight, we would like to receive power from it, regardless of the other converters. However, we encounter a problem when one converter turns off. It is explained in Figure 5.4.
Figure 5.4 Stages of Converter Turn-Off. (a) Normal Conditions, (b) Capacitor Forced to Zero, (c) Capacitor Forced Negative, (d) Output Diode Forward Biased

Figure 5.4 (a) shows the output capacitors of two series-connected converters during normal operating conditions. I_{out} is flowing negatively through both capacitors, and therefore each converter supplies I_{out} to the output caps, such that charge balance is achieved and V_{out} is constant in both cases.

When one of the converter turns off, it can no longer supply the current needed to equal I_{out}. I_{out} will decrease the voltage across the capacitor, while the other converters increase their output voltages to equal 200V. Very quickly, the output capacitor of the off converter can reach 0V, as in Fig. 5.4 (b), and then go negative, as in Fig. 5.4 (c).
Once the capacitor reaches a voltage of -0.7V, it will forward bias the converter’s output diode, as seen in Fig. 5.4 (d) (shown here is a flyback converter, but a forward converter will see the same effect). Conduction of the diode may or may not be a problem, but it is certainly a problem for the capacitor to swing negative, as this limits the type of capacitor that can be used. Electrolytics and tantalums cannot be used during this condition. The alternative is to force all converters to shut down as soon as a minimum voltage is reached by any of the output capacitors. This will greatly restrict the range of conditions over which the DC optimizer is useful.

Given the preceding discussion, the parallel-output topology is chosen for this design. All that remains is to choose an isolated converter. The flyback converter is appropriate for this design based on the requirements for high output voltage and low output current, and its low parts count will help to minimize cost.

5.3 Effect on System

The parallel-output converter can be hooked directly to the input of an inverter. The ground of the output capacitor will then be tied to the inverter’s input ground. Additionally, other optimizers can be connected in parallel, as shown in Figure 5.5. The total number of parallel converters is only limited by the capacity of the inverter.
Figure 5.5  DC Optimizers Connected in Parallel

The optimizers’ output capacitors will all add up so that the inverter has a large effective input capacitance. If interleaving is used in the converters, this output current can be very smooth.

The proposed DC optimizer relaxes the requirements for the system’s inverter. Recall that for a typical DC optimizer, each optimizer performs local MPPT while the inverter performs global MPPT. In our case, since there is one fixed inverter input voltage of 200V, the local MPPT of the optimizers suffices, and the inverter only needs to regulate the 200V. The fact that the inverter regulates the input at 200V also simplifies its design, since it can be optimized for a fixed input voltage, unlike the typical DC optimizers, which require handling a wide current and voltage input range.
5.4 Proposed Control Circuit Architecture

Figure 5.6 shows the proposed control circuit architecture for this design. The Vdd and ground traces for the IC’s are shown.

Each of the three flyback converters has its own dedicated circuitry, which is powered directly from the PV source. The three circuits are floating relative to each other. The input voltage for the bottom converter is the ground for the middle converter,
and so on. By using local control, we eliminate the need for isolated signal lines and floating/bootstrap gate drivers.

The microcontroller performs voltage and current measurement, and executes the MPPT algorithm. There are many microcontrollers suitable for this application, and the choice should be based on cost. Ideally the microcontroller would have just enough memory to hold the algorithm. Here we assume that the microcontroller contains an ADC as well. Once a new value of PV voltage is chosen by the algorithm, the microcontroller sends this value to a DAC which converts it to an analog voltage on the Vref pin of the PWM controller. The PWM controller performs voltage-mode control based on the value of Vref, and the value of Vin (feedback pin not shown in the above schematic). The gate driver (included in the PWM IC in the above schematic) supplies current to the gate of the FET. The gate driver is a heavier power dissipator than the other IC’s, and by using the PV voltage to directly supply the gate driver, the LDO size can be minimized, and voltage dips on the LDO output can be minimized. By connecting the gate driver to the PV voltage, we will drive the FET harder as power levels increase. It is a nice coincidence in this case that the PV voltage (6-14V) is the perfect range to drive a typical power MOSFET.

The LDO linear regulator provides power to all of the IC’s. Some LDO IC’s have the option to add undervoltage lockout (UVLO) by adding a couple resistors, and we take full advantage of that feature here. By using UVLO on the PV voltage, we can choose at what light intensity level the converter will turn on and off. The idea is for the converter to naturally turn on and off with the sun, with no need for external control.
The daily cycle is as follows, as illustrated in Figure 5.7. Before sunrise, the converter is off, and as the sun rises, the PV cells will start to conduct while the converter is still turned off. Therefore the module will be operating at Voc. At a certain Voc determined by the UVLO circuit (point A), the converter will turn on. The MPPT algorithm will search for the MPP (point B), which will be a lower voltage than Voc. The voltage can decrease, and the UVLO circuitry will prevent the converter from shutting off. The circuit will continue to operate under all normal light conditions (point C). As the sunlight is waning, the MPP voltage will eventually start to drop. When the MPP voltage reaches the lower limit of the UVLO circuit, the converter will turn off (point D). Because there is always a little bit of light, the cells will return to Voc after being turned off (point E). Therefore the UVLO values must be chosen such that the
converter turns off at a lower light intensity than where the converter turns on (point E <
point B), otherwise the converter could enter a hiccup mode at turn off, where the
converter reaches its UVLO threshold, turns off, the cell voltages increase to Voc, the
converter turns on, decreases to MPP, and so on. In chapter 8 we will choose values for
the UVLO circuit as we perform the power stage calculations.
6.1 Energy Loss in Flyback Converter

Figure 6.1 shows the basic flyback converter. When the FET is on, Vin charges the flyback transformer’s magnetizing inductance, and when the FET turns off, the stored energy transfers to the output. In continuous conduction mode (CCM), the magnetizing inductance maintains an average current, although the input and output currents are discontinuous.

The discontinuous currents are sources of energy loss. The primary winding’s leakage inductance (not shown above) shares the magnetizing current during the FET’s on time, but when the FET turns off the energy stored in the leakage inductance will dissipate its energy in the FET, while it resonates with the FET’s output capacitance. This can be a significant source of energy loss, as well as dangerous for the FET, as the ringing at FET turnoff can reach very high voltages.

To protect the FET, an RCD clamp is frequently used. This circuit is shown in Figure 6.2.
When the FET turns off, the leakage inductance will discharge into the R-C network through the diode. This limits the ringing voltage at the FET’s drain, but does not eliminate it completely [22]. Also, the leakage energy is still the same and is still a significant source of loss. Another major contributor to loss is the reverse recovery energy of the secondary diode. When the FET turns on, the diode is forced to abruptly stop current flow and reverse bias at a level of $V_{out} + (n_2/n_1)V_{in}$. The combination of discontinuous current and large reverse bias voltage makes the diode’s $Q_{rr}$ another large contributor to circuit loss.

It is desirable to reduce or eliminate these losses to maximize the converter’s efficiency. The solution is to use an active clamp circuit.

Figure 6.2 Flyback Converter with RCD Clamp
Figure 6.3 shows the addition of an active clamp to the flyback converter. Here the magnetizing inductance $L_m$ and leakage inductance $L_{lk}$ are explicitly shown. The operation of the circuit is the same for the high-side and low-side configurations. There are a few subtle differences between the two converters, which we will discuss in a later section. The differences will lead us to choose the high-side active clamp for this application.

6.2 Steady-State Operation of Active Clamp Flyback Converter

In this section we describe the steady-state operation of the active clamp flyback converter. The switching period can be described as seven different segments. The switching waveforms are shown below in Figure 6.4, which is adapted from [23].
Figure 6.4 Active Clamp Flyback Waveforms (adapted from [23])
T0-T1:

The equivalent circuit topology during T0-T1 is shown in Figure 6.5 below.

![Figure 6.5 T0-T1](image_url)

This is the main energy transfer state, as Vin charges Lm and Llk through Q1’s Rdson. This state is the same in the regular flyback converter, and lasts for duration approximately D*Ts (where Ts is the switching time period). At the end of this period, current Im reaches its maximum, which we call Ipk.

T1-T2:

The equivalent circuit during T1-T2 is shown in Figure 6.6.
This state begins at the instant Q1 turns off. It is assumed that due to Q1’s large output capacitance, Q1 achieves zero-voltage switching (ZVS) at turnoff. When Q1 turns off, Ipk will quickly charge Coss1 from 0V while discharging Coss2, which is initially charged to approximately Vin+nVo.

T2-T3:

The equivalent circuit during T2-T3 is shown in Figure 6.7.
Figure 6.7 T2-T3

Ipk charges Coss1 and discharges Coss2 until Coss2 reaches -0.7V and its diode conducts. This marks the instant T2. During the brief interval T2-T3, current is almost constant at Ipk. The resonance between Lm and Vcl is much too slow to play a role here. Since Q2’s diode is conducting, Q2 may turn on after T2 with ZVS.

T3-T4:

The equivalent circuit during T3-T4 is shown in Figure 6.8.

Figure 6.8 T3-T4

At T3, Vcl has increased enough such that V(Lm) reaches –nVo, and becomes clamped there. This marks the beginning of the resonant period, as Llk resonates with Ccl. Ilk initially charges Ccl, but becomes negative around halfway through this time interval. Initially, Ilk = Im = Ipk, so the output current begins ramping up from zero, instead of the abrupt edge as in the regular flyback. As Ilk decreases, more of the magnetizing current goes to the output. When Ilk becomes negative, both the magnetizing and leakage currents flow to the output. Therefore Iout has a peak level
higher, almost double, than the regular flyback. Note that the deadtime between Q1 turning off and Q2 turning on is flexible, as Q2 has until Ilk changes direction to turn on with ZVS.

T4-T5:

The equivalent circuit during T4-T5 is shown in Figure 6.9.

![Figure 6.9 T4-T5](image)

At T4, Q2 turns off. Ilk has reached its negative peak, and this current discharges Coss1 while charging Coss2. The energy stored in Coss1 is delivered to the output. This is a brief time interval, governed by the time constant from Llk and (Coss1 || Coss2). For Q1 to achieve ZVS, Llk must have enough energy to completely discharge Coss1 and charge Coss2. In the event that Llk cannot completely discharge Coss1, Q1 should turn on at the minimum voltage possible. We will have more to say about this when we derive design constraints for the converter.
T5-T6:

The equivalent circuit during T5-T6 is shown in Figure 6.10.

![Figure 6.10 T5-T6](image)

Once \( I_{lk} \) has completely discharged \( C_{oss1} \), and reaches -0.7V, Q1’s body diode will conduct. Q1 can turn on with ZVS during this interval. The leakage current decays at a constant rate, due to being clamped at \( V_{in} + nV_o \). The output current, equal to \( n(I_m + I_{lk}) \), decays as well.

T6-T7:

The equivalent circuit during T6-T7 is shown in Figure 6.11.
Q1 is on and leakage current becomes positive again. The voltage across the magnetizing inductor remains clamped at \(-nV_o\) while the output current ramps down at a rate due to \(L_{lk}\). This soft decay will reduce the effect of reverse recovery once \(I_{out}\) becomes zero at T7. At T7, leakage current equals magnetizing current and we start the cycle again.

6.3 Derivation of Design Constraints

We mentioned that T2 begins when Q2’s body diode forward conducts. This situation is shown again in Figure 6.12 (a), with an alternative scenario in Figure 6.12 (b).
As Coss1 increases and Coss2 decreases, the diode will conduct before Vm is clamped to \(-nVo\), but why? We know that Vcl is roughly equal to nVo, so the answer is not obvious. The alternative scenario in Figure 6.12 (b) shows what happens if Vm becomes clamped to \(-nVo\) first. Ipk will continue to charge Coss1 and discharge Coss2, but with a very fast resonant time segment, due to the capacitances Coss1 and Coss2, and leakage inductance Llk. This brief resonant period will increase the noise of the circuit and the RMS current losses. It is desired to avoid this scenario. This leads us to the first design constraint. For Q2’s body diode to conduct first, the ratio of leakage inductances must be constrained to the following:

\[
\frac{Llk}{Lm} > \frac{0.7}{nVo}
\]

Another design constraint arises at T4, which is shown again below for convenience.
We will derive the design constraint to achieve ZVS on Q1, by comparing the energy in Coss1 and Coss2 to the energy contained in Llk at Q2 turnoff.

We know that the initial energy in Llk is given by:

$$E_{Lk} = \frac{1}{2} \times L_{lk} \times I_{lk}^2$$

However, calculating the energy in Coss1 and Coss2 is not as simple, because FET output capacitance is non-linear over voltage, and we are completely discharging Coss1 (and completely charging Coss2) during this interval. If we use the value of capacitance at Vin+nVo, we could be quite a bit off of the actual value. Some typical Coss versus voltage curves are shown in Figure 6.14.
A simple solution to this problem is to calculate the total charge contained in the capacitors using $Q = CV$, and use this number to calculate the total energy. We achieve this by finding two capacitances that will give us the same total charge, as shown in Figure 6.15.

Figure 6.15 Modified Coss Curves to Approximate Total Charge
We use this square approximation, knowing that the total charge is the area under the curve from 0V to $V_{in+nVo}$. We choose two values, $Cossa$ and $Cossb$, such that the following hold:

$$\text{Area 1} = \text{Area 2} \text{ (for curves such as 6.15 (a))}$$

$$\text{Area 1} + \text{Area 3} = \text{Area 2} + \text{Area 4} \text{ (for curves such as 6.15 (b))}$$

To calculate the energy, we start by calculating total charge, which is the area underneath the straight lines:

$$Q_{total} = C_{ossa} \cdot V_{dsa} + C_{ossb} \cdot (V_{ds} - V_{dsa})$$

Then we use this to find the equivalent capacitance at a given value of $V_{ds}$.

$$C_{eq} = \frac{Q_{total}}{V_{ds}}$$

This gives us the energy in $Coss$:

$$E = \frac{1}{2} C_{eq} \cdot V_{ds}^2 = \frac{1}{2} \frac{Q_{total}}{V_{ds}} \cdot V_{ds}^2 = \frac{1}{2} Q_{total} \cdot V_{ds}$$

$$= \frac{1}{2} (V_{dsa} (C_{ossa} - C_{ossb}) + V_{ds} \cdot C_{ossb}) \cdot V_{ds}$$

Now we are ready for the design constraint, which is that the minimum leakage inductance energy be greater or equal to the total $Coss$ energy:

$$I_{min} \geq \sqrt{\frac{2(E_{Q1} + E_{Q2})}{Llk}}$$
The next design constraint is regarding the length of time between T4 and T7. During this time the output current is decaying and the leakage current is returning to equalling the magnetizing current. This time interval decreases the effective duty of the converter, and although the slower decay of output current will reduce reverse recovery, we should keep this interval to some minimum percentage of Ts. Figure 6.16, taken from [24] shows how we can simplify to three time intervals, with the interval in question lasting time a*Ts.

![Figure 6.16 Simplification into Three Time Intervals (Taken from [24])](image)

The slope during (0,aTs) is determined by the input and output across the leakage inductance. We will choose a maximum value for “a” which leads to a constraint on Llk:

\[
a \leq 2 \times \text{Im}\text{(maximum)} \times \frac{Llk}{Ts \times (Vin + nVout)}
\]

The final design constraint is regarding deadtime between Q2 turnoff and Q1 turnon. Because deadtime is something we cannot change, we must turnon Q1 when Vds
reaches its minimum. In the event that there is not enough energy to forward bias the diode, this deadtime will minimize energy loss.

The minimum will occur at $\frac{1}{4}$ the resonant time period between $L_{lk}$ and $(C_{oss1} \parallel C_{oss2})$.

$$\text{Deadtime} = \frac{\pi}{2} \sqrt{\frac{L_{lk}}{C_{eq1} + C_{eq2}}}$$

6.4 Stability of Clamp Voltage

An assumption has been implicitly made about the voltage across the clamp capacitor. Looking at the waveform for $V_{cl}$ in Figure 6.4, we notice that $V_{cl}$ always peaks in the middle of the resonant period, and returns to its initial value. It is constant over a switching cycle. Consider the fact that $L_{lk}$ and $C_{cl}$ have a given resonant frequency, with a given period. Since the duty in our converter can vary over a moderately wide range, how do we know $V_{cl}$ will always return to its original value? If, at the beginning of the resonant period, $I_{lk}$ is at the peak of a cosine waveform, then $V_{cl}$ will be at the middle of a sine wave, and will only return to its initial value if the duty is exactly half of the resonant period. Clearly this cannot be the case.

As it turns out, when the resonant period begins and $I_{lk} = I_{pk}$, the current begins between the peak of a cosine and the zero crossing. The peak of the cosine then corresponds to all of the energy being contained in $L_{lk}$, and none of it in $C_{cl}$ (here we refer to the differential voltage across $C_{cl}$ with respect to $nVo$). For a given duty, the converter will quickly stabilize such that the following hold:
1. Clamp capacitor voltage peaks at the middle of the resonant interval

2. Leakage inductor current crosses zero at the middle of the resonant interval

3. Leakage inductor current begins the resonant interval at \( I_{pk} \), and ends the resonant interval at \(-I_{pk}\)

   The only necessary condition is that the resonant interval (Q1 off time) be less than half of the resonant period due to \( C_{cl} \) and \( L_{lk} \):

   \[
   T_{OFF} < \pi \cdot \sqrt{L_{lk} \cdot C_{cl}}
   \]

   A MATLAB script was written to verify this analysis, which proves to be too cumbersome to prove in a closed form.

   Figures 6.17 and 6.18 show the results of the MATLAB script.
In Figure 6.17, for various lengths of Toff with respect to the resonant period, we calculate and plot the phase difference between the center of the interval and the pi/2 point on the cosine (current) and sine (voltage) waves, over sequential cycles. Here we see that they rapidly converge, verifying the plot of Vcl in Figure 6.4.

Figure 6.18 shows the stabilization of the clamp voltage (actually voltage difference to nVo) over sequential cycles. This convergence implies that any off time will be stable in the converter, as long as the maximum off time is less than half the resonant frequency (although oscillations take more time to settle when Toff approaches half the resonant frequency).
Since we have shown that the leakage inductor crosses zero at the middle of the resonant interval (middle of the main FET’s off time), we can use this result to calculate the steady-state voltage of the clamp capacitor. Specifically, we will calculate the difference between the clamp capacitor voltage and $nV_o$. This additional clamp voltage can be used for another design constraint, specifically minimum off time, or maximum duty, as the clamp voltage will grow larger with smaller off times.

We use the fact that the initial energy in the clamp capacitor and leakage inductor is the total energy in the resonant circuit, and define $I_{max}$ to be the peak of the cosine, where all of the energy has transferred to the inductor:

$$I = I_{max} \cos (2\pi ft)$$

When the cosine reaches $I_m$, the time is as follows:

$$t = \frac{\pi}{2} \sqrt{Llk \cdot Ccl} - (1 - d)Ts/2$$

We use this time to calculate $I_{max}$, and use $I_{max}$ to calculate $\Delta V_{cl}$:

$$I_{max} = \frac{I_m}{\cos \left( \frac{\pi}{2} - \frac{(1 - d)Ts}{2\sqrt{LlkCcl}} \right)}$$

$$\Delta V_{cl} = \frac{Llk}{Ccl} \sqrt{I_{max}^2 - I_m^2}$$

This can be used to balance the tradeoff between maximum duty and clamp capacitor voltage.
6.5 Summary of Design Constraints

Our derived design constraints are collected below in Table 6.1.

<table>
<thead>
<tr>
<th>Constraint</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>( \frac{L_{lk}}{L_m} \geq 0.7 ) ( nV_o )</td>
<td>Eliminate resonance between ( L_{lk} ) and ( C_{oss} )</td>
</tr>
<tr>
<td>( I_{min} \geq \sqrt{2(E_{Q1} + E_{Q2})/L_{lk}} )</td>
<td>ZVS on Q1 over operating range</td>
</tr>
<tr>
<td>( a \leq 2 \times I_m(\text{maximum}) )</td>
<td>Limits effective duty</td>
</tr>
<tr>
<td>( \frac{L_{lk}}{T_s \times (V_{in} + nV_{out})} )</td>
<td></td>
</tr>
<tr>
<td>( \text{Deadtime} = \frac{\pi}{2} \sqrt{L_{lk} \times (C_{eq1} + C_{eq2})} )</td>
<td>FETs turn on at minimum voltage</td>
</tr>
<tr>
<td>( T_{OFF} &lt; \pi \times \sqrt{L_{lk} \times C_{cl}} )</td>
<td>Stability of clamp voltage</td>
</tr>
<tr>
<td>( \Delta V_{cl} = \frac{L_{lk}}{\sqrt{C_{cl} \times (I_{max}^2 - I_m^2)}} )</td>
<td>High duty increases clamp voltage</td>
</tr>
</tbody>
</table>

Table 6.1 Summary of Design Constraints
CHAPTER 7. EFFICIENCY IMPROVEMENT WITH GAN FETS

7.1 Introduction

Gallium Nitride (GaN) has in recent years become a popular material for making FETs. First used for RF transistors, GaN-on-Si devices exhibit a unique property of a 2-dimensional electron gas (2DEG) which allows electrons to flow at a very high conductance. In the last ten years, the attractive 2DEG property led researchers to try to develop FETs appropriate for power conversion. The first company to sell GaN FETs for power conversion applications is Efficient Power Conversion (EPC), a company founded by Alex Lidow, former CEO of International Rectifier. The GaN FETs sold by EPC (called eGaN FETs) used a recessed gate structure to block the 2DEG until the gate voltage goes high, creating a normally-off FET. Figure 7.1 shows the structure of a lateral silicon MOSFET alongside the eGaN FET. The structures are very similar, where the 2DEG acts as the channel.

Figure 7.1 Structure of (a) Lateral Si MOSFET, (b) eGaN FET
The 2DEG allows very high ratios of Rdson/Vbd to be achieved, making them an immediate competitor with power MOSFETs. Figure 7.2 shows a comparison of Qg/Rdson for the two materials [25].

Figure 7.2 Qg/Rdson for eGan and Si FETs (Taken from [25])

Figure 7.2 is slightly misleading. All of the eGaN FETs have a fully enhanced channel with a gate drive of 5.5V, and they cannot be driven harder, as they breakdown at 6V. The low gate charge in Figure 8.2 is due to the fact that the drive voltage is always 5.5V, and not 15V as in a fully enhanced MOSFET channel. Advantage can be taken of the low Rdson to either save power in charging the gate, or in Rdson conduction loss, or both.
7.2 eGaN FET Properties

eGaNs can be used similarly to power MOSFETs, but there are a couple issues for the circuit designer to be aware of.

- eGaNs have a very low threshold voltage of around 0.7V. This means that the gate’s turn off resistor should be very small to avoid phantom turn on during the FETs turn off instant. Also, inductance should be minimized between gate and source; excessive ringing can also lead to phantom turn on.
- As previously mentioned, eGaNs should be driven between 5-5.5V, but never reach 6V. This is a constraint but also an advantage as less gate charge is required.
- eGaNs have a positive tempco of Vgs across the entire range. This means that they can be operated in the linear region if desired, with no risk of thermal runaway as in vertical power MOSFETs.
- The body diode of the GaN FET does not arise from a parasitic BJT as in vertical MOSFETs, but it still exists due to the drain’s ability to reverse-bias the channel. A benefit is that there is no reverse recovery loss.

7.3 Design of Gate Driver for Q1

In this work we will use eGaN FETs to gain efficiency. Recall from Chapter 5 that we can drive the FET harder by using the available PV voltage. It is more advantageous to use GaN FETs and add a separate gate drive IC and associated 5V linear regulator, as shown in Figure 8.3.
The LM5113 is a gate drive IC designed specifically for driving GaN FETs, providing separate outputs for the on current and off current, so that resistance can be optionally added for the on path, and not for the off path. We can quickly calculate the gained efficiency for this new configuration:

Figure 7.4 Driving a MOSFET (a) On, (b) Off

Figure 7.4 shows the current paths for driving a MOSFET from the PV voltage. During turn on, \( R_{on} \) will dissipate \( 1/2CV^2 \) joules and during turn off, \( R_{off} \) will
dissipate 1/2CV^2 joules, where C = Cgs and V = Vp. The total energy dissipated over one switching cycle:

$$E_{total} = CgsVp^2$$

Figure 7.5 Driving GaN FET (a) On, (b) Off

Figure 7.5 shows the current paths during turn on and turn off of the GaN FET. During turn on, we may think of the current as coming from Vp through the pass transistor of the LDO at the same time the LDO is providing the current to Cgs. We can calculate the power dissipated in the pass transistor by realizing that it shares the same current as Ron:

$$E(R_{pass}) = \int P(R_{pass})
= \int (Vp - Vgs) \frac{Vgs}{Ron} e^{-\frac{t}{RCgs}} = (Vp - Vgs) \frac{Vgs}{R} RCgs$$

$$= CgsVpVgs - Vgs^2$$

We add to this the energy dissipated in Ron and Roff:

$$E_{total} = CgsVpVgs - Vgs^2 + Vgs^2 = CgsVpVgs$$
We see that as the PV voltage increases, the energy savings in the gate driver will increase.

7.4 Design of Gate Driver for Q2

As Q2 is a high-side FET, we will need to use a floating gate driver. A common method is shown in Figure 7.6 (a), where an isolation transformer is used. We have chosen to use a GaN FET for the high-side FET as well. The LM5113 is equipped to drive the high-side FET in a half-bridge configuration, but the active clamp FET is positioned the same as in a half-bridge so we may use it here. The LM5113 uses a bootstrap capacitor to supply 5.2V Vgs to Q2. Using this method will reduce the parts count for our design, not to mention the benefit of using GaN with its low Rdson.

Figure 7.6 High-Side Gate Driver (a) With Isolation Transformer, (b) Using LM5113
CHAPTER 8. POWER STAGE CALCULATIONS

8.1 Outline of Calculations

This chapter details the calculations for the power stage. The procedure begins with choosing at what minimum sunlight the converter should operate at. This gives us the range for input voltage and current, and allows us to choose values for the UVLO circuit. Given these values, we choose magnetizing inductance $L_m$, leakage inductance $L_{lk}$, and clamp capacitor $C_{cl}$ based on the design constraints derived in Chapter 6.

8.2 Input Voltage and Current Range

The input voltage range follows directly from the input current range, based on the operating points of the PV cells. We choose a minimum light intensity of 10% rated $I_{mp}$, or 0.549A. Using the PV cell model, this gives us the following values at minimum light intensity:

$\begin{align*}
I_{sc} &= 0.55A; & I_{mp} &= 0.223A; & V_{mp} &= 7.92V; & V_{oc} &= 12.46V \ (at \ minimum \ light) \\
\end{align*}$

Recall from Chapter 5 that the UVLO works if the converter turns off at a higher voltage than at turn on. We choose a higher value of light intensity for the converter to turn on at:

$\begin{align*}
I_{sc} &= 0.8A; & I_{mp} &= 0.313A; & V_{mp} &= 10.46V; & V_{oc} &= 13.1V \ (at \ sunrise) \\
\end{align*}$

The maximum voltage and current occur at the rated MPP (voltage will be higher at $V_{oc}$, but the MPPT algorithm will maintain $V$ closer to $V_{mp}$):
\[ Isc = 5.49A; \quad Imp = 4.77A; \quad Vmp = 12.27V; \quad Voc = 14.7V \quad (at \ peak \ sunlight) \]

The converter should be designed to operate at currents as high as Isc and voltages as high as Voc, if not for safety then for derating of the converter. This gives us the range for input voltage and current:

\[ Vin: \ 7.92 - 14.7V; \quad lin: \ 0.223 - 5.49A \quad (input \ voltage \ and \ current \ range) \]

8.3 Choice of Switching Frequency, Duty and Turns Ratio

The switching frequency is chosen to be \( fs = 200kHz \), a good tradeoff between size and switching losses.

The tradeoff between duty and turns ratio for most DC-DC converters will be optimum at around \( d=0.5 \), which balances RMS currents on the primary and secondary and the voltage stress on the primary MOSFET. In our case, the input voltage varies over a small range as power varies over a wide range. It is desirable to have as wide a range of duty as possible, to increase the resolution of the MPPT algorithm. To this end, we plot the range of duty versus turns ratio \( n \) in MATLAB, using the flyback converter equation:

\[
\frac{V_{out}}{Vin} = \frac{1}{n} \cdot \frac{D}{D - 1}; \quad (n = \frac{n1}{n2})
\]

The plots below in Figure 8.1 show how duty varies with \( n \), at maximum input voltage, minimum input voltage, and MPP voltage. (note that Dmax in the figure refers
to duty at maximum input voltage, not the maximum duty)

![Figure 8.1 Duty Ratio Versus Turns Ratio](image)

Figure 8.1 Duty Ratio Versus Turns Ratio

We see that at \( n = 0.05 \), the variation in duty is the highest. We choose this to be the turns ratio. At this point, the duty at MPP is around 0.45, as seen in Figure 8.1 (a).

\[
\text{turns ratio } n = \frac{n_1}{n_2} = 0.05
\]

8.4 Selection of Leakage Inductance \( L_{lk} \) and Magnetizing Inductance \( L_m \)

\( L_{lk} \) and \( L_m \) are selected based on meeting the design constraints from Chapter 6. The first constraint comes from the time interval \( aT_s \), when the output current is decaying while \( L_{lk} \) returns to \( L_m \). We would like this interval to not be too big. We will select a value of 0.15 for “a”, which gives an upper bound for \( L_{lk} \):
\[ L_{1k} \leq a \cdot T_s \cdot \frac{V_{in} + nV_{out}}{2I_m} = 0.15 \cdot 5 \cdot \frac{12 + 0.05 \cdot 200}{2 \cdot 4.77} = 1.7 \mu H \]

The second constraint is used for a lower bound on \( L_{lk} \), but it is a little more involved:

\[ L_{lk} \geq 2(E_{Q1} + E_{Q1})/l_{pkmax}^2 \]

To compute this we need the values of \( E(Q1) \) and \( E(Q2) \), the energy stored in the output capacitances of \( Q1 \) and \( Q2 \) as they swing from \( 0V \) to \( V_{in} + nV_{out} \). Below are the capacitance curves from the EPC2001 datasheet:

![Figure 8.2 EPC2001 (a) Output Capacitance Curves (b) with Equivalent Coss Values](image)
We use the approximation derived in Chapter 6 to calculate $E(Q_1)$ and $E(Q_2)$ as they swing from 0V to $V_{in+nV_{out}}$:

$$E = E_{Q1} + E_{Q2} = 2 \times \frac{1}{2} C_{eq} \times V_{ds}^2 = \frac{Q_{total}}{V_{ds}} \times V_{ds}^2 = Q_{total} \times V_{ds}$$

$$= (V_{ds \alpha} (C_{ossa} - C_{ossb}) + V_{ds} \times C_{ossb}) \times V_{ds}$$

Plugging the values in from Figure 8.2 (b),

$$(V_{ds \alpha} (C_{ossa} - C_{ossb}) + V_{ds} \times C_{ossb}) \times V_{ds} = (14 \times (1.35 - 0.4) + 24 \times 0.4) \times 24$$

$$= 549 \text{ nJ}$$

We may now use the above formula for the design constraint:

$$Llk \geq \frac{2(E_{Q1} + E_{Q2})}{I_{pkmin}^2} = 2 \times \frac{549}{0.223^2} = 22 \mu H$$

This constraint will be unwieldy, just for achieving ZVS at minimum input current. If we look at the lower bound given previously as 1.7µH, we can see at what minimum current we will achieve ZVS:

$$I_{min \ for \ ZVS \ at \ (Llk = 1.7 \mu H)}: \quad \sqrt{\frac{2(E_{Q1} + E_{Q2})}{Llk}} = \sqrt{\frac{2(549)}{1.7}} = 0.80 \text{ A}$$
Since 0.80A is sufficiently low, we can consider 1.7uH to be a good estimate for \( L_{lk} \). We choose a round value of \( L_{lk} = 2uH \):

\[
L_{lk} = 2uH
\]

\( L_m \) is selected based on \( L_{lk} \) using the following design constraint:

\[
\frac{L_{lk}}{L_m} > \frac{0.7}{nV_{out}} \quad \Rightarrow \quad L_m < \frac{nV_{out} \cdot L_{lk}}{0.7} = 0.05 \times 200 \times 2/0.7 = 28.6uH
\]

We choose \( L_m = 27uH \). Using a standard value component can give potential to use an off-the-shelf part (although not optimized for efficiency). As a check, we can use this value of \( L_m \) to look at the magnetizing current ripple at MPP:

\[
\Delta I_m = \frac{V_{mp}}{L_m} \times D_{mp} \times T_s = \frac{12.26}{27} \times 0.45 \times 5 = 1.02A
\]

The magnetizing current at MPP is:

\[
I_m = \frac{I_{mp}}{D_{mp}} = \frac{4.77}{0.45} = 10.6A
\]

Therefore the ripple represents \( 1.02/10.6 = 9.6\% \) change in current. This will reduce RMS current losses versus the usual accepted value of 20\% current ripple.
8.5 Selection of Ccl

In general, Ccl should be large as to minimize its voltage swings during the resonant interval. A strict lower bound comes from the design constraint:

\[
\text{maximum } T_{off} < \pi \sqrt{\frac{L_{lk} C_{cl}}{}}
\]

Plugging in our value of \( L_{lk} = 2 \mu \text{H} \),

\[
C_{cl} > \frac{(T_{off} \times \pi)^2}{L_{lk}} = \frac{(0.558 \times 5 \times \pi)^2}{1.7} = 45.2 \mu \text{F} \quad \text{(lower bound for } C_{cl})
\]

To approximate the voltage swing on Ccl during the resonant period, we note that the leakage current \( I_{lk} \) will roughly follow a sawtooth waveform from \( I_{pk} \) to 0 in the first half of the resonant interval. Therefore we can measure the voltage ripple on Ccl by looking at the charge delivered from Llk:

\[
\Delta V_{cl} = \frac{Q}{C_{cl}} = I_{pk} \times \frac{(1 - D)T_s}{4 \times C_{cl}}
\]

For \( C_{cl} = 68 \mu \text{F} \), at MPP we have:

\[
\Delta V_{cl} = \frac{Q}{C_{cl}} = I_{pk} \times \frac{(1 - D)T_s}{4 \times C_{cl}} = 4.77 \times \frac{0.55 \times 5}{4 \times 68} = 48 \text{mV}
\]

Since the steady-state voltage across \( V_{cl} \) is \( nV_0 = 10 \text{V} \), a ripple of 48mV is acceptable.
Therefore we choose $C_{cl} = 68\mu F$.

The remaining components will be chosen in the following chapter as we perform open-loop simulations to verify the converter’s operation.
9.1 Discussion on Modeling and Simulation

In this section, we will model the various components of the flyback converter and put them together to perform simulations of the converter. Simulation of power electronics converters is not trivial, as it involves capturing circuit behavior for widely ranging time constants. We would like to observe switching behavior as well as low-frequency transient behavior. We will use Simplis as the circuit simulator for this section. Simplis and Simetrix are packaged together, and use the same schematic entry GUI, but Simetrix is a SPICE-based simulator whereas Simplis is specifically made for switching circuits such as power converters. Simplis uses piecewise-linear (PWL) models to approximate the behavior of circuit elements. This approximation allows for faster simulation times. In the following sections, we will develop PWL models for the PV sub-module and for the GaN FET. We will use simplified models for the flyback transformer and PWM IC to perform open-loop simulations which accurately depict the switching behavior of the circuit.

9.2 PWL Model of PV Sub-Module

We will begin by modeling the string of 24 PV cells. In Chapter 2, we used Simetrix to develop a very accurate PV cell model, based on the module made by Jiawei. We can place 24 of these cells in series in Simetrix, and by measuring various points on the V-I curve we describe the sub-module as a PWL resistor. We adjust the value of Isc
to extract PWL models at any desired illumination level. The 24-cell schematic is shown in Figure 9.1.

![24 Series Cells in Simetrix](image)

**Figure 9.1 24 Series Cells in Simetrix**

The circuit on the right of the schematic performs a voltage sweep of the cells and measures current and power. The current waveform for the case of \( \text{Isc}=5.49 \) is shown in Figure 9.2.
Figure 9.2  24-Cell V/I Measurement

Figure 9.3 Below Shows the Values of Voltage and Current Used to Construct the PWL Model.

<table>
<thead>
<tr>
<th>X(V)</th>
<th>Y(A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>5.463</td>
</tr>
<tr>
<td>10</td>
<td>5.11</td>
</tr>
<tr>
<td>11.01</td>
<td>5.05</td>
</tr>
<tr>
<td>11.59</td>
<td>4.98</td>
</tr>
<tr>
<td>12.05</td>
<td>4.88</td>
</tr>
<tr>
<td>12.38</td>
<td>4.76</td>
</tr>
<tr>
<td>12.8</td>
<td>4.5</td>
</tr>
<tr>
<td>13.62</td>
<td>3.47</td>
</tr>
<tr>
<td>14.23</td>
<td>2.06</td>
</tr>
<tr>
<td>14.85</td>
<td>0.019</td>
</tr>
</tbody>
</table>

Figure 9.3  Values for PWL Model of PV Sub-Module
9.3 Model of GaN FET

The GaN FET is modeled using a Level 2 PWL FET model, which involves PWL capacitors for $C_{gs}$, $C_{gd}$, and $C_{ds}$, a PWL body diode, and specified values of threshold voltage, gain, and saturation resistance. These values are taken from the EPC2001 datasheet.

The PWL capacitance models are defined in the voltage-charge domain. We accomplish this by integrating over constant-capacitance approximations. The capacitance curves are shown in Figure 9.4.

![Figure 9.4 EPC2001 Capacitance Curves](image)

The extracted values of charge and voltage are shown below in Figure 9.5.
Figure 9.5  PWL Capacitance Calculations

The body diode is modeled as a PWL resistor, as shown in Figure 9.6.

The PWL values for the body diode are shown in Figure 9.7.
The threshold voltage and gain are also taken from the datasheet, as shown in Figure 9.8. This approximation is common to all Level 2 FET models, and is appropriate since we are using the FET in switch mode. For a linear mode FET, a more accurate model would be used.

Figure 9.7  PWL Body Diode Values

<table>
<thead>
<tr>
<th>X (V)</th>
<th>Y (A)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0.7</td>
<td>1.00E-09</td>
</tr>
<tr>
<td>1.5</td>
<td>0.5</td>
</tr>
<tr>
<td>1.8</td>
<td>4</td>
</tr>
<tr>
<td>2.1</td>
<td>10</td>
</tr>
<tr>
<td>2.4</td>
<td>26</td>
</tr>
<tr>
<td>3.1</td>
<td>100</td>
</tr>
</tbody>
</table>

Figure 9.8  Approximation of Threshold Voltage and Gain
The GaN FETs have substantial gate leakage current, and we model this with a PWL resistor between gate and source (this is not modeled in other Level 2 FETs). The datasheet curve is shown below in Figure 9.9.

![Figure 9.9 PWL Resistor to Model Gate Current](image)

All that remains is the ON resistance of the FET, which we read directly from the datasheet.

The complete model exists as text, which we paste into Simplis’ command window. The complete text is pasted below in Figure 9.10 for reference.
A schematic symbol is made for the EPC2001, which is shown below in Figure 9.11.

9.4 Model of Flyback Transformer

The flyback transformer is modeled using the magnetizing inductance, with the ideal transformer turns implemented by a voltage-controlled voltage source and current-
controlled current source, as shown in Figure 9.12. Small series resistances are added to simulate the resistances of the copper windings.

![Flyback Transformer Model](image)

**Figure 9.12  Flyback Transformer Model**

9.5 Model of PWM Block and Gate Driver

A simple PWM block is implemented with a 1V sawtooth wave and comparator, with duty being an externally controlled voltage. This allows us to directly control duty and observe the circuit’s behavior. The ISL8130 provides roughly 20ns of deadtime for the PWM signals. In Chapter 8, we calculated 96ns to be the optimum deadtime. Here we use a non-linear delay block to provide 96ns of deadtime. This could be practically implemented in a number of ways.

The separate ON/OFF gate drive signals of the LM5113 are modeled here by using a current-controlled switch to add a parallel resistance during turn OFF. We have added a five ohm resistor to the turn ON branch and added nothing to the turn OFF branch, as per recommendations from EPC’s application notes. The PWM and gate drive block is shown in Figure 9.13.
9.6 Complete Circuit

The complete active clamp flyback converter model is shown in Figure 9.14.

There are a few notes to be made on the final values chosen in the switching model. The duty at MPP is higher than the desired value of 0.45; it is closer to 0.55. This is due to the limiting duty from the variable “a”. The leakage inductance is much smaller here than derived in Chapter 8: 510nH instead of 2uH. This is because the value of “a” was changing the desired duty of the converter too much. Schottky diodes are
added in parallel with the GaN FETs. This is because the body diodes have a knee around 1.7V, which is very high considering we use the body diodes to achieve ZVS on both switches. Schottkys with a forward voltage of 0.5V alleviate this problem. One final note: series ESR resistances are added throughout, including between the output capacitance and the 200V output voltage (regulated by the inverter), which simulates the effect of wiring between the optimizer outputs.

9.7 Simulation Waveforms

Use is made of Simplis’ periodic operating point (POP) simulation mode, where a trigger is added to look for periodicity at a point. When a very small tolerance is reached, waveforms are plotted. This has the effect of a transient analysis, except the simulator automatically waits until the circuit has reached its operating point. The POP trigger schematic symbol is shown in Figure 9.15, where it is attached to the high-side gate drive signal.

![Figure 9.15 POP Trigger in Simplis](image-url)
The waveforms of $V_{in}$ and $I_{pv}$ are shown in Figure 9.16. An input capacitance of 1000uF is chosen, and voltage ripple is around 20mV.

![Figure 9.16  Vin and Ipv](image)

Next we show the clamp capacitor voltage, as it rises and returns to its steady-state value, along with output current, magnetizing current, leakage inductance current, and clamp current in Figure 9.17. The currents all have the expected shapes.

![Figure 9.17  Current Waveforms and Clamp Voltage Waveform](image)
To show ZVS on Q1, Figure 9.18 shows the drain voltage, gate voltage, and drain current of Q1, and Figure 9.19 shows a zoom view of the waveforms at ZVS.
We see the drain voltage drop coincide with the drain current going negative. Then the gate of Q1 goes high while the current is still negative, indicating ZVS. The glitch on the gate voltage is an artifact of the simulation, due to the high $dI/dt$ as Q2 turns off.

Similarly, we plot Q2’s Vds, Vgs, and current as shown in Figure 9.20.
A zoomed in view in Figure 9.21 shows that Q2 undergoes ZVS. The gate voltage sees the same glitch at Q1’s turnoff.
Figure 9.21 ZVS on Q2
CHAPTER 10. PHASE-LOCKED LOOP FOR CONVERTER INTERLEAVING

10.1 Desire for Phase Interleaving

Phase interleaving is frequently used when multiple power converters are added together in parallel. Assuming the converters are operating at the same switching frequency, their switching cycles are phase shifted with respect to each other. The benefit is lower RMS current (lower ripple) at the output.

To demonstrate the necessity for interleaving, we use the circuit model derived in Chapter 9 and add the three output currents in parallel, just like it would be in the proposed system. The schematic is shown in Figure 10.1 on the following page. Following in Figures 10.2 and 10.3, we first look at the output currents summing when the converters are in phase with each other, and then when the converters are phase-shifted 120 degrees apart from each other. Both results give the same average output current of 836mA, but the case with interleaving has an RMS output current of 870mA, while without interleaving the output RMS current is 1.3A. This difference of 1.3-0.87=430mA is all AC current which is absorbed in the output capacitances’ ESRs. Clearly we want to use phase interleaving if it is practical.
Figure 10.1 Parallel-Connected Flyback Converters
Figure 10.2  Output Currents Added Without Interleaving

Figure 10.3  Output Currents Added With Interleaving
10.2 Typical Interleaving Technique with PWM Synchronization

Interleaving is a common task, and is typically performed via synchronization of the PWM controllers. A typical PWM controller has a timing pin, which outputs a ramp waveform in sync with converter’s output drive pulses. To synchronize the PWM controller, an external pulse discharges the timing capacitor, forcing the ramp waveform to start with the external pulse. A central controller can then be used to synchronize multiple converters however is pleased. This method is shown in Figure 10.4, which is taken from [26].

![Typical Synchronization Method (Taken from [26])](image)

10.3 Timing Pin on ISL8130

Unfortunately, the PWM controller chosen for this work, the ISL8130, does not have the capability to use the normal synchronization method. This is because the frequency of the controller is set with a single external resistor, and instead of a ramp waveform, the resistor draws a steady (and small) DC current, which sets the frequency.
of the controller according to a datasheet figure. This figure is shown below in Figure 10.5.

![Figure 10.5 Timing Resistance from ISL8130 Datasheet](image)

The author spoke with Intersil’s technical staff, who confirmed that the ISL8130 cannot be synchronized. Measurements show that a DC voltage of 0.7V is output on the pin, regardless of Rt. The current drawn by Rt then sets the controller frequency.

10.4 Proposed Phase-Locked Loop

A phase-locked loop (PLL) is proposed to synchronize the ISL8130, specifically for the application of this work’s three series-input converters. The proposed schematic is shown in Figure 10.6.
The PLL for one converter is shown. In red are the blocks of a general PLL. A resistor network at the timing pin varies the equivalent resistance between 80 kohm (transistor OFF) and 60 kohm (transistor saturated). This corresponds to a frequency range of 180-220kHz. This PLL uses as its reference a delayed gate drive signal from the converter just above. The highest converter is free running at 200kHz, and the middle converter runs phase-shifted to the highest converter, etc. Although the converters are floating relative to each other, there is a maximum voltage of around 14V that any of the converters will see. We use this fact to choose a capacitor to translate the upper converter’s gate drive signal to the voltage of the lower converter. The lower Schottky prevents the input of the digital circuitry from going negative. A typical digital phase detector circuit is used, followed by a charge pump. The NPN transistor acts as an amplifier with changing operating point. This allows its output impedance to change.
over a wide range. To this end, capacitors are used to bias the NPN, and the charge pump adds to and takes away charge from the bias caps to change the NPN’s operating point. There are a few resistors which are not shown in the schematic to improve readability of the schematic, but they are important, specifically between the transistors of the charge pump (to prevent large current spikes) and between the charge pump and the bias capacitors (to limit the rate of voltage rise and decay as a loop filter).

10.5 Simulation of PLL

The PLL circuit was successfully simulated. The converter locks to the reference signal within a couple milliseconds over the 180-220kHz range. The schematic in Simplis is shown below in Figure 10.7.

![PLL Schematic in Simplis](image)

Figure 10.7 PLL Schematic in Simplis

To model the non-linear VCO characteristic of the ISL8130, a PWL resistor was used based on the datasheet’s figure, as shown in Figure 10.8.
Figure 10.8 Transformation of Timing Graph into PWL Resistor Model

We use the fact that the ISL8130 outputs 0.7V on its timing pin to first transform the graph from frequency/resistance to frequency/current. Then we transform frequency into voltage, which we input into an ideal VCO block in Simplis. The zoomed in circuit is shown in Figure 10.9 for clarity.
Figure 10.9 Zoomed in Schematic of Equivalent Non-Linear VCO

Since no digital delay blocks were readily available in the Simplis library, a delay block was made using a timer and a 100MHz clock, as shown in Figure 10.10.

Figure 10.10 Delay Block in Simplis

The waveforms at steady-state are shown in Figure 10.11.
One by one, let us describe the waveforms from the top down. First we have the pulse at the digital circuit input, which reaches 5V for a few tens of ns and briefly goes negative, as far as the Schottky forward voltage of around -0.3V. Next we see the level-shift capacitor voltage, which shifts a 0-5V signal to a 12-17V signal, with rounding of the edges being a good sign that the input pulse to the phase detector has ample width.
Next we have the voltage at the output of the charge pump. The brief pulses happen while the charge pump transistors are simultaneously conducting. This overlap period is on purpose and comes from a small delay block between the AND gate and the reset of the flip-flops. This prevents low-frequency oscillations modulating the PLL waveforms. Next we have the NPN bias voltage, which is at 0.6V, in its active region. Next we see the converter’s output pulses above the high converter’s pulses. They are phase shifted by 120 degrees, confirming operation of the circuit. The LOW and HIGH signals share a brief overlap period as mentioned. The last waveform is the delayed input pulse, which is perfectly locked to the output pulse.
CHAPTER 11. DISCUSSION AND CONCLUSIONS

We have detailed the design of an active clamp flyback converter using GaN FETs, for use in a sub-module DC converter performing MPPT. All efforts were made to maximize efficiency, to justify the additional cost of using module-level power electronics. The design in this work uses an autonomous control scheme, where the converters turn on and off naturally with the sunrise and sunset. This system can operate as an add-on for existing panels. Many manufacturers of PV modules are currently installing DC optimizers into their modules’ junction boxes, and the design in this work would be a good candidate, especially if system cost is valued over system control and monitoring, as this design uses autonomous control with the intent of avoiding external communication. Furthermore, the design consists of three equal converters; many more small converters can be manufactured to reduce the cost per unit. Although no external control is needed to operate, the system designer may desire to have an external reset signal come from the system inverter to the DC optimizers, for safety purposes. This can easily be added as an I/O input to the microcontroller.

Extensive analysis has been performed on the active clamp flyback stage, to ensure stable operation over all operating points. This is particularly important for the converter in this report, as operating points can vary widely over temperature and sunlight. We have derived a handful of design constraints. These constraints can be used as a balance to choose at which low current levels ZVS will be achieved, and to reduce converter noise. The low-side clamp was found to be advantageous over the high-side
clamp, due to a smaller clamp voltage and due to lower RMS currents on the input of the converter (where currents are highest). We have used an algorithm to demonstrate the stability of clamp capacitor voltages, which are stable for off times less than one half the resonant period.

We have modeled the EPC2001, a GaN FET, as a PWL model in Simplis, including the body diode and gate leakage, and demonstrated its operation with simulations. We used GaN FETs in the active clamp flyback converter, for both the primary switching FET and the active clamp FET. The existence of a gate drive IC tailored for eGaN (the LM5113) made the gate drive design very simple.

The PLL designed in this work is unique, insofar as it is used to synchronize PWM controllers for PV sub-module series-connected converters. The tolerable voltage difference of 12-14V between converters proved to be useful in decoupling the gate drive signals between the converters. This is a classical PLL, with the main difference being that the non-linear characteristic of the timing resistor versus frequency leads to the VCO in the PLL having a non-linear characteristic. Nonetheless, we are biasing frequencies in a small band, such that the characteristic approaches that of a linear VCO.

Future work includes the implementation of this converter onto a PV module, for extensive testing over weather conditions. For testing it may be necessary to add additional data logging circuitry. After extensive data is taken, the design can further be tuned for efficiency, and for cost.
REFERENCES


