Highly Integrated Switched-Mode Power Converters Employing CMOS and GaN

Technologies for Distributed MPPT

by

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ABSTRACT

The photovoltaic systems used to convert solar energy to electricity pose a multitude of design and implementation challenges, including energy conversion efficiency, partial shading effects, and power converter efficiency. Using power converters for Distributed Maximum Power Point Tracking (DMPPT) is a well-known architecture to significantly reduce power loss associated with mismatched panels. Sub-panel-level DMPPT is shown to have up to 14.5% more annual energy yield than panel-level DMPPT, and requires an efficient medium power converter.

This research aims at implementing a highly efficient power management system at sub-panel level with focus on system cost and form-factor. Smaller form-factor motivates increased converter switching frequencies to significantly reduce the size of converter passives and substantially improve transient performance. But, currently available power MOSFETs put a constraint on the highest possible switching frequency due to increased switching losses. The solution is Gallium Nitride based power devices, which deliver figure of merit (FOM) performance at least an order of magnitude higher than existing silicon MOSFETs. Low power loss, high power density, low cost and small die sizes are few of the qualities that make e-GaN superior to its Si counterpart. With careful design, e-GaN can enable a 20-30% improvement in power stage efficiency compared to converters using Si MOSFETs.

The main objective of this research is to develop a highly integrated, high efficiency, 20MHz, hybrid GaN-CMOS DC-DC MPPT converter for a 12V/5A sub-panel. Hard and soft switching boost converter topologies are investigated within this research, and an innovative CMOS gate drive technique for efficiently driving an e-GaN power stage
is presented in this work. The converter controller also employs a fast converging analog MPPT control technique.
DEDICATION

To my family and all my friends who supported me with patience and love all the way!!
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1. INTRODUCTION

Fossil fuels that draw on finite resources face a number of challenges like rising prices, security concerns over dependence on imports from a limited number of countries, and growing environmental concerns over the climate change. These risks have pushed governments, businesses, and consumers to support renewable energy, specifically solar. Solar energy is non-polluting, simple, and indefinitely renewable. Thomas Reuters forecasts solar power as the dominant source of power generation by 2025 [1]. This could lead to a clean environment, less money spent on utilities, and a healthier world.

1.1. Photo-Voltaic Cells

In 1839, Edmond Becquerel discovered the Photo Voltaic Effect, which is the process by which a voltage is generated when photons strike an appropriate material [2]. In 1954, the first silicon based solar cell was developed thus laying the road for decades of research. Photo-Voltaic Modules consist of solar cells that convert the solar energy falling on it into flow of electrons, which in turn constitute current. Depending upon the material used for making the solar cells, the power handling capacity of the solar cells varies [3]. Depending upon the requirements, solar cells are connected in series or parallel to form a Photo-Voltaic Panel. Photo-Voltaic cells of varying power and efficiency are available in market to suit different applications.
A typical solar power system for the residential housing market, as shown in Figure 1, consists of an array of solar panels that convert the incident solar energy to electrical energy. This electrical energy is unregulated DC power, which is then fed to an electrical system that performs a technique called “Maximum Power Point Tracking (MPPT)”. The MPPT extracts the maximum power out of the array of panels. This output of the MPP tracker is then converted from DC to AC power using an inverter. The converted AC power is either supplied to the load (residential or industrial) for consumer use or supplied to the grid for power distribution.

1.2. I-V Characteristics of Solar Cells

Solar cells have a complex relationship between solar irradiation, temperature, and total resistance, which produces a non-linear output efficiency. The I-V (Current-Voltage) and P-V (Power-Voltage) characteristics at the output of a solar cell is given in Figure 2. The I-V characteristics are denoted by the orange curve and the P-V characteristics are denoted by the blue curve. The point $I_{sc}$ is called the short circuit current, which denotes
the current when the output terminals of the solar cell are shorted together, and the point $V_{oc}$ is called the open circuit voltage, which denotes the voltage generated when the output of the solar cell is open circuit. The output power is zero at the short circuit current and open circuit voltage points. The point of the power curve where the power is maximum is called the Maximum Power Point (MPP). A solar cell has an output voltage of 0.5V and an output current of 5A. Commercial solar panels connect 72 cells in series to achieve an output of 36V at 5A. Such panels are connected in series and parallel to form the solar array shown in Figure 1.

![Characteristics of a Solar Cell](image)

**Figure 2: Characteristics of a Solar Cell**

The solar cell has complex relationship with solar irradiance and temperature.

![Electrical Model of Solar Cell](image)

**Figure 3: Electrical Model of Solar Cell**
A solar cell electrical model of a solar cell is shown in Figure 3, where the current source ($I_L$) represents the current generated due to irradiance, the diode current ($I_D$) represents the current lost due to recombination, shunt resistance ($R_{SH}$) represents the losses due to the material and series resistance ($R_s$) represents the contact losses.

The variations of the solar PV output voltage and current with irradiance and temperature are illustrated in Figure 4 and Figure 5. The $I_{sc}$ decreases almost linearly with the solar irradiance, as seen from Figure 3, but $V_{oc}$ changes only moderately in a logarithmic fashion with solar irradiance. Figure 4 shows the variation of I-V characteristic with temperature. While $V_{oc}$ decreases drastically with temperature, $I_{sc}$ increases only slightly.

![Figure 4: Variation of I-V Characteristics with Irradiance (W/m²)](image-url)
Figure 5: Variation of I-V Characteristics with Temperature

In conventional Central solar PV systems, the PV panels (36V@5A) are connected in series called a “string”, to get a very high voltage and these strings are connected in parallel to get the required power/ current, called an “array”. MPPT is performed on this array, the output of which is either used to charge a battery or converted to AC using Inverters.

A shade can be of two types: soft shade and hard shade. Soft shade is a distant obstruction where the shadow is diffused and hence reduces the amount of light reaching the solar cells (e.g. a shadow from a tree). Hard shade is an obstruction that completely blocks from the light from reaching the solar cell. Soft shade casted on a single solar cell decreases current proportionally to the reduced irradiance. Regardless of the irradiance amount, as long as there is sufficient light (~50W/m²), the voltage remains the same. The voltage of a PV cell depends more on temperature and the electron band-gap in the materials than on the light itself. When such Photovoltaic cells are connected in strings, the total current in the string is limited by the current provided by the PV that is most shaded, as it will generate the least current. Moreover the current produced by the other non-shaded
cells in series will force a current flow through the shaded cell, which generates heat and creates a hotspot within the shaded solar cell, eventually damaging it. Hence bypass diodes are connected in parallel to a series of cells, (24 cells in commercial 36V panel), which bypasses the shaded cell(s) from the main current path. The best strategy for saving power and protecting the shaded cells is to connect a bypass diode across each solar cell, but this is economically impractical, hence bypass diodes are connected across 24 cells in a panel. These 24 cells in series form the ‘sub-panel’ within a solar PV panel.

1.3. Distributed Maximum Power Point Tracking

The increased use of solar photovoltaic (PV) installations for residential purposes (sub 10KW systems) is driving the need for more compact and efficient power electronics that harvest the maximum energy available from residential PV systems. Solar PVs exhibit non-linear P-V characteristics, which facilitates the use of Maximum Power Point Tracking (MPPT) for harvesting the maximum available power. However, due to dependency of temperature and solar insulation on the material, the MPP varies non-linearly, which makes it difficult to track the MPP. Distributed Maximum Power Point Tracking (DMPPT) have proved significant efficiency increase over traditional centralized MPPT (CMPPT) by performing the MPPT control at a granular level, regardless of the power converter topology [5][8]. DMPPT can be performed at various levels of granularity, including (1) string-level, (2) panel-level, (3) sub-string-level and (4) cell-level, as shown in Figure 6, where (3) and (4) require access to intermediate voltages within the PV panel.
Matlab simulations over different levels of MPPT on a 2KW system under shading conditions are tabulated in Table 1. The system contains two rows (strings) of 11 panels each (396V). When the two strings are unshaded, they have a common MPP. But when they are shaded, each element (panel, sub-panel or cell) in the array will have different MPP. Central MPPT operates on a single MPP regardless of the difference in MPP, hence creating power loss. This shows that more granular MPPT results in higher system efficiency. The various levels of granularity are represented in Figure 6.

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<th>MPPT LEVEL</th>
<th>EFFICIENCY IMPROVEMENT (%)</th>
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<tr>
<td>CENTRAL</td>
<td>-</td>
</tr>
<tr>
<td>STRING</td>
<td>11</td>
</tr>
<tr>
<td>PANEL</td>
<td>13.2</td>
</tr>
<tr>
<td>SUB-PANEL</td>
<td>20.7</td>
</tr>
<tr>
<td>CELL</td>
<td>28.7</td>
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</table>

Table 1: Efficiency Improvement for Different DMPPT Levels [42]

Edgar has tabulated the results in his dissertation [42]. The table is reproduced here.
The trade-off in performing at a granular level is the cost and component overhead. An optimum trade-off level was found to be the sub-panel level with three MPPT converters per panel. The increased number of electronic components can be justified, if the efficiency can be increased, form-factor reduced and cost lowered. The need for smaller form-factor motivates the pursuit of increasing converter switching frequencies. Increasing switching frequency improves transient performance and reduces energy storage requirements on the passive devices, which enables miniaturization of passive components. But these advantages are limited by the power devices that can operate efficiently at the required frequency. Enhancement-mode Gallium Nitride (GaN) high electron mobility transistors (HEMTs) exhibit lower parasitic capacitances and low $R_{DS(ON)}$, which can significantly reduce transistor losses compared to Silicon (Si) metal oxide semiconductor field effect transistors (MOSFETs) [10][11]. The lower gate-drain capacitance in e-GaN HEMTs, due to the lateral structure, enables power engineers to design converters at higher frequencies. e-GaN FETs outperform state of the art Si MOSFETs with a low FOM $Q_G \times R_{DS(ON)}$ and significantly reduced size [12][13]. Implementations of high frequency buck converters using e-GaN FETs [14] shows a 20 to 30 percentage point improvement in efficiency using e-GaN FETs versus silicon MOSFETs. But, to-date, the focus for power converter efficiency has been placed on the power stage. There is still a need for efficient gate drivers at high switching frequencies for moderate power applications. This research focuses on the gate driver and controller, the power stage, and the integration of the system for solar sub-panel maximum power extraction.
1.4. MPPT Control Algorithm

Maximum power point tracking (MPPT) is a technique used to get the maximum possible power from one or more photovoltaic panels [4]. It is basically controlling the loop to track the output peak power as annotated in Figure 2 under varying atmospheric conditions (shading). For any given set of operational conditions, cells have a single operating point where the values of the current and voltage of the cell result in a maximum power output. These values correspond to a particular load resistance, which is equal to V/I as specified by Ohm's Law. A photovoltaic cell, for the majority of its useful curve, acts as a constant current source. However, at a photovoltaic cell's MPP region, its curve has an approximately inverse exponential relationship between current and voltage. From basic circuit theory, the power delivered from a device is optimized where the derivative (graphically, the slope) dI/dV of the I-V curve is equal and opposite to the I/V ratio (where dP/dV=0). This is known as the maximum power point (MPP), and corresponds to the "knee" of the curve. There are numerous algorithms currently available in literature. Esram has done an extensive comparative analysis on most of the popular architectures [25]. The paper provides a survey on 19 distinct methods, with many various implementations. The popular methods are hill climbing/perturb and observe (P&O), incremental conductance [7], fractional open circuit technique, fractional short circuit technique, ripple correlation control (RCC), fuzzy logic control [26], neural network and their derivatives [27][28]. This work implements a Ripple Correlation Control (RCC) MPPT, which is a very fast converging technique that can be completely implemented using analog circuits and consumes very low power [5].
1.5. Objectives and Strategies

The objective of this work is to develop, design, and implement a high efficiency, small form factor, CMOS-GaN MPP Tracker that converts 12V from a solar PV sub-panel to 36V output. This work employs the following strategies to achieve the above objective:

- High switching frequency (target frequency – 20MHz)
- Employs e-GaN HEMT as power switches
- Advanced power stage architectures (Class-E)
- Implement a fast, efficient analog MPPT algorithm
- Integrate the gate drivers and MPPT in a CMOS process.
- Efficient PCB layout techniques
2. SYSTEM CONFIGURATION

A commercial solar sub-panel has an output voltage of 12V at 5A. This is the available power to be efficiently converted using DMPPT. Figure 7 shows the proposed DMPPT system block diagram with the sub-panels providing the input power. Here, the bypass diodes are removed and the output of each subpanel is given as an input to an MPP power converter, which is essentially a switched mode power converter (SMPC) with a non-linear control algorithm to achieve the MPP.

![Diagram](image)

Figure 7: Proposed Configuration with Sub-Panel MPPT Converters

Each sub-panel MPPT converter, as shown in Figure 7, converts the 12V @ 5A to 36V. The output of these three converters are connected in series to achieve 108V, which is eventually boosted up to a regulated 400V at 2.2A using another voltage-mode controlled SMPC. This DC power is then converted to AC power with an inverter. The focus of this thesis is the 12V-to-36V converter highlighted in Figure 7. The system block diagram for the converter is described in the Figure 8.
The system consists of a single power source, which is the sub-panel that delivers 12V at 5A. An integrated CMOS chip senses the voltage and current and generates PWM pulses to drive the e-GaN boost power stage. The CMOS chip consists of an Auxiliary Regulator, MPPT control circuitry, and the gate drive circuitry for the e-GaN switches. The auxiliary regulator is a linear n-MOS pass transistor type regulator that converts ~12V to 5V. This power is used to supply the CMOS IC that houses the MPPT and the gate drive. The MPPT control uses is a very fast, efficient, analog technique called the Ripple Correlation Control. The gate drive is carefully designed for e-GaN HEMTs, and is optimized for minimal loss at 20MHz switching frequency.
2.1. High Frequency Switching Converters

DC-DC converters are being designed at higher frequencies in an effort to decrease the size of the passives with an inherent improvement in the transient characteristics. However, these advantages come at the cost of increased switching losses and gate drive losses. Switching losses are primarily caused by two factors; (1) $P_{Cout}$, the charging and discharging of the device output capacitance ($C_{oss}$) and (2) $P_{Ovlp}$, the overlap of the drain-source current and voltage waveforms. As the device switches on and off, the parasitic device output capacitance stores and dissipates energy every switching transition. This loss is proportional to the switching frequency and the $C_{oss}$ value [38], and is given by:

$$P_{Cout} = V_{DS(OFF)}^2 C_{oss} f_{sw}$$

This loss can be significantly reduced, if the $C_{oss}$ value is minimized. The other major loss ($P_{Ovlp}$) affected by increased frequency is the overlap of drain-source current and drain-source voltage during the turn-on and turn-off transitions.

![Figure 9: FET Turn On and Turn Off Waveforms [17]](image-url)
Figure 9 is taken from reference [17]. It can be seen from Figure 9 that region A and B are simultaneously non-zero drain-source current and voltage. At increased frequencies, these transitions become a significant portion of the time period, and hence increase loss. The turn-off and turn-on times (length of all four time intervals) are a strong function of the parasitic capacitances and the available gate driver current. A crude estimate of the switching losses [17] is calculated, using linear approximations of the gate current, drain current, and the drain voltage, as:

\[
P_{SW} = \frac{V_{DS(OFF)} * I_L}{2} \cdot \frac{(t_2 + t_3)}{T}
\]

This emphasizes the importance of an optimum gate driver design for high frequency applications, as \(t_2\) and \(t_3\) are a strong function of parasitic capacitances and the gate driver current.

2.2. Semiconductor Device Considerations

Silicon devices dominated the power electronics industry over three decades, but its fundamental limitations have stalled its use for high frequency and high power applications. This paved the way for the emergence of wide band gap devices like Gallium Nitride (GaN). Many vendors have made available e-GaN HEMTs in either enhancement mode or depletion mode variants. Due to the ease in designing with positive voltages in switched mode power conversion, this work employs enhancement mode HEMTs (e-GaN HEMTs).
Figure 10: e-GaN Device Structure [41]

Figure 10 is taken from [41], and it shows the structure of an e-GaN device. A very thin AlGaN layer is grown on top of the highly resistive e-GaN. This thin layer creates a strained interface between the GaN and AlGaN crystals layers. This interface, combined with the intrinsic piezoelectric nature of GaN, creates a plain of high conductivity, high velocity electrons known as a two dimensional electron gas (2DEG). Further processing of a portion of the 2DEG forms a depletion region. This depletion region interrupts the 2DEG and blocks conduction, and becomes the gate. A positive voltage at gate with respect to source injects electrons under the gate contact and completes the 2DEG, creating a highly conductive, bi-directional path from drain to source.

e-GaN has a lateral structure with a two-dimensional electron gas transport mechanism that allows higher mobility and hence lower RON in a thinner device dimension, while maintaining the same breakdown voltage rating. Being a lateral device has significant effect on reducing the parasitic capacitances in the device. The reduced gate-to-source and gate-to-drain capacitance ($C_{GS}$ and $C_{GD}$) significantly increases the device’s voltage switching capability. Another advantage of e-GaN HEMTs is that GaN is inert to the environment, and therefore needs no package. The package-less design
approach greatly reduces any resistive, inductive, and thermal problems. The lower parasitic inductance helps in reducing inductive (L.dI/dt) losses and ringing effects in high frequency switching converters. e-GaN HEMTs have inherent body diodes, which are different from the MOSFETs in that they are devoid of any reverse recovery losses.

![Figure 11: EPC8004 Mounting Die Snapshot [Taken from EPC8004 Datasheet]](image)

The device chosen for this work is EPC8004 from EPC Corporation. In summary, these devices have significantly lower FOM \([Q_{GXR_{DS(ON)}}]\) compared to state of the art Si MOSFETs. Apart from the advantages discussed above that are offered by e-GaN HEMTs in general, EPC8004 has features that make it suitable for high frequency operation and hence chosen for this work. As seen from the snapshot of the mounting die side of EPC8004 shown in Figure 11, the device has a separate gate return, which can help in reducing the common source inductance to the device itself. The efficiency impact of common source inductance is well documented [18]. The reduced miller ratio in these devices provides high dV/dt switching capability without the fear of miller turn-on. The gate and drain solder bars are designed so that optimal current paths are 90° with respect to each other, thus reducing the interaction of the gate circuit current with the drain circuit current and effectively reducing the common source inductance (CSI) of the device.
Figure 12: Five Key Characteristics of GaN compared to SiC and GaAs [43]

GaN devices offer five key characteristics as shown in Figure 12 (taken from www.gansystems.com): high dielectric strength, high operating temperature, high current density, high switching speed, and low on-resistance. These characteristics are due to the properties of GaN, which compared with Si, offer 10 times higher electrical breakdown, higher operating temperature, and exceptional carrier mobility. Table 2 shows the parameter values of the GaN device used in this work.

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>VALUE</th>
</tr>
</thead>
<tbody>
<tr>
<td>RDS(ON)</td>
<td>125 mΩ</td>
</tr>
<tr>
<td>QG</td>
<td>358 pC</td>
</tr>
<tr>
<td>Ciss</td>
<td>45 pF</td>
</tr>
<tr>
<td>Coss</td>
<td>17 pF</td>
</tr>
</tbody>
</table>

Table 2: EPC8004 characteristics
3. POWER CONVERTER STAGE

The e-GaN devices with their low parasitic capacitance makes them apt for hard switching applications. This work looks at two power stages, one hard switching and one soft switching architecture. The hard switching architecture is a synchronous boost converter, and the soft switching converter is a class-E based boost converter. The detailed design and operation of the boost converters are given in Sections 3.2 and 3.3. Section 3.1 describes the common losses associated with switching converters.

3.1. Switching Converter Losses

The various losses associated with switching converters are discussed below. The losses are broadly classified into frequency dependent losses and frequency independent losses [38].

- Frequency dependent losses

  1. Gate Loss

     - Energy required to charge and discharge the MOSFET parasitic gate capacitances, given as: \( P_G = Q_G V_{cc} f_{sw} \)

  2. Switching Loss

     - Occurs during switching transitions

     - Product of the switch current and drain-to-source Voltage, given as: \( P_{sw} = K (T_r + T_f) V_{ds} I_{ds} f_{sw} \), where the constant \( K \) is typically between 1/6 and 1/2

  3. Output Loss

     - \( P_{out} \) is energy lost when the switch output drain-to-source capacitance is discharged during turn on.
\[ P_{out} = \frac{1}{2} C_{ds}.V_{ds}^2 f_{sw} \]

- Non-Frequency Dependent losses
  1. Conduction losses is the energy lost due to the power dissipation on the finite on-resistance of the switch
     \[ P_{\text{cond}} = I_{dsRMS}^2 . R_{ds} \]

- Other Losses
  1. Copper loss
     - Traces and copper windings in magnetics
     - Skin effect loss
  2. Control loss
     - Control circuits and external biasing circuits
  3. Core loss
     - Hysteric loss and Eddy current loss

The *switching losses* are dominant losses at higher frequencies, which are discussed in Section 3.2.
3.2. Design of Hard Switching Boost Converter

Figure 13: Hard switching boost converter power stage

Figure 13 shows the hard switching boost converter power stage used in this work. Boost converter is a class of DC-DC converter where the output voltage is greater than the input voltage. It achieves this step-up voltage conversion using an inductor and two switches (or switch and diode device). During the on period, the switch $S_1$ turns on and the inductor $L_1$ is charged to store energy by building a magnetic field. The polarity will be positive on the left side of $L_1$. Now in the next half cycle, the switch $S_1$ turns off, and switch $S_2$ (or diode) turns on. Since the inductor doesn’t allow sudden changes in current, its magnetic field collapses and hence a back emf (electro-motive force) voltage is generated across it, with polarity of positive on the right side of $L_1$. Now the inductor voltage is in series adding with the input source voltage and hence the output voltage will be a higher voltage than the input depending on the on time of the switching pulse.

The design parameters of the hard switching boost converter is given in Table 3
<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Input Voltage, $V_{in}$</td>
<td>12V</td>
</tr>
<tr>
<td>Output Voltage, $V_{out}$</td>
<td>36V</td>
</tr>
<tr>
<td>Duty Cycle (from $V_o/V_{in} = 1/(1-D)$)</td>
<td>0.667</td>
</tr>
<tr>
<td>Switching Frequency, $f_{sw}$</td>
<td>20MHz</td>
</tr>
<tr>
<td>Input Current, $I_{in}$</td>
<td>5A</td>
</tr>
<tr>
<td>Output Current, $I_{out}$</td>
<td>1.67A</td>
</tr>
<tr>
<td>$R_L = V_o/I_{out}$</td>
<td>21.6Ω</td>
</tr>
</tbody>
</table>

Table 3: Boost Converter Design Parameters

Design of Inductor:

The equations from below are derived by applying the volt-sec balance on the input inductor.

$$L_{max} = \frac{R_L D(1-D)^2}{2f_{sw}} = 1.6\mu H$$

$$L_{min} = \frac{V_o D (1-D)}{\Delta I_L f_{sw}} = 0.08\mu H$$

$$DC\ bias = \frac{I_{o,max}}{1-D_{max}} = 5A$$

$$I_{L,peak} = I_{in,max} + \frac{\Delta I_L}{2} = 5.25A$$

$$I_{L,RMS} = \sqrt{\frac{I_{in,max}^2 + \Delta I_L^2}{12}} = 5A$$

Chosen Value: 1µH.
Design of Output Capacitor:

The equations below were derived by applying current-sec balance on the output capacitor.

\[
\text{Capacitance } C_L > \frac{V_o DT_s}{f_{sw} \Delta V_o R_L} = 0.617 \text{nF}
\]

\[
I_{C,RMS} = I_o \sqrt{\frac{D}{1-D}} = 2.36A
\]

\[
ESR < \frac{\Delta V_o}{\Delta I_{in,peak}} = 0.343 \Omega
\]

Chosen based on RMS current requirement. Verified if the ripple specification is satisfied with the chosen C and ESR. The final chosen value is 1\(\mu\)F.

3.3. Design of Class-E Boost Converter

![Class-E Boost converter diagram]

Figure 14: Class-E Boost converter

Soft switching converters use resonance to mitigate the switching losses. This work implements a Class-\(E^2\) switching converter, which consists of a Class-E inverter followed by a Class-E rectifier [31], as shown in Figure 14. Class-E inverters are derived from power amplifier topologies that rely on reactive networks to shape the switch voltage and current.
waveforms to reduce switching loss. The class-E converter enforces ZVS (Zero Voltage Switching) at device turn-on.

![Class-E Inverter Diagram](image)

**Figure 15: Class-E Inverter**

Figure 15 shows a basic class-E inverter [31-37]. The inductor $L_{fl}$ is large enough that it is approaches a very large impedance at the switching frequency, and the current through the inductor is almost DC. Since there is no DC path to the load, the energy is stored in the shunt capacitance of the e-GaN HEMT. A series resonant is tank formed by the $L_{RES}$ and $C_{RES}$. When these components are tuned, the drain voltage will return to zero as the energy in $C_P$ is converted to a pure sine wave due to the presence of the series resonant tank, and at this point, the switch may be turned on with minimal loss. As mentioned above, the input current is approximately constant, and represented by $I_L$. Figure 17 shows the waveforms associated with the Class-E converter. If the loaded Q-factor of the resonant L-C series resonant network is high ($Q > 5$), the current $I_{RES}$ will be a sine wave [32]. Therefore, the current through the parallel combination of switch $S$ and the shunt capacitor $C_1$ is the shifted sine wave $I_L - I_{RES}$. This current flows through the switch.
when it is turned on and through the capacitor when the switch is off. When the switch is off, the current through $C_1$ produces the voltage waveform that achieves ZVS. The switch turn-off is forced by the gate-source voltage but it turns-on automatically when the switch drain-source voltage crosses zero because of the presence of the body diode. Since the switch turns-on at zero voltage, the turn-on losses are negligible. ZVT can be accomplished only for load resistances from 0 to $R_{opt}$, where $R_{opt}$ is the optimum resistance. [33 – 37]. For $R_{LOAD} > R_{opt}$, ZVT cannot be achieved. This cause non-zero switching losses, thereby reducing efficiency. To avoid these undesirable conditions, the input resistance of the rectifier must be in the range $0 < R_{LOAD} < R_{opt}$ (i.e. the rectifier input must be impedance matched to the inverter output).

![Figure 16: Class-E Rectifier](image)

Class-E rectifier consists of a diode with a shunt capacitor, and a second order loss pass filter consisting of $L_{f2}$ and $C_f$, as shown in Figure 16. The input to the rectifier is a sine wave, which is the output of the Class-E inverter. The large inductor $L_{f2}$ forces the current $I_o$ to be a DC current. Hence the current through the diode and capacitor $C_2$ combination
is $I_{AC} - I_o$, which is a level shifted sine wave. This current flows through the diode when the diode is on, and flows through $C_2$ when the diode is off. The capacitor current is given by $i_{C2} = C_2 \frac{dv_D}{dt}$. Since $i_{C2}$ is zero at turn-off, the slope of $V_D$ will also be zero. Now the capacitor current, $i_{C2}$ goes negative and hence the $V_D$ decreases to a negative peak until the capacitor current reaches zero. Once the capacitor current reaches positive value, $V_D$ increases back to zero. At this instant, the diode turns on and pulls $i_{C2}$ back to zero. Hence the turn-off is at $\frac{dv_D}{dt} = 0$, while the turn-on is at small positive $\frac{dv_D}{dt}$. The waveforms in Figure 17 are taken from [31].

![Class-E Inverter and Class-E Rectifier Operating Waveforms](image)

Figure 17: Class E Inverter and Class-E Rectifier Operating Waveforms [31]
4. GATE DRIVER

The three important factors to be considered while driving an e-GaN HEMT are 1) the maximum allowable gate voltage, 2) gate threshold voltage, and 3) the body diode voltage drop [20]. The maximum gate-source voltage for an e-GaN FET is 6V, which is low compared to its Si counterparts. The gate terminal has a diode characteristic, as evident from the gate characteristics given in Figure 18. An increase in voltage beyond 6V will create a significant leakage gate current resulting in power loss. Moreover a gate-source voltage below 4V will result in a larger $R_{DS(ON)}$. Hence a voltage of 4.5V-5.5V has to be maintained to achieve low $R_{DS(ON)}$ and to reduce gate losses.

![Gate Characteristics of EPC8004](image)

Figure 18: Gate Characteristics of EPC8004 [Taken from EPC8004 Datasheet]

The e-GaN FETs have a lower threshold voltage (0.7V-2.5V) compared to Si MOSFETs, which makes it more susceptible to Miller induced turn-on losses. The factors that trigger this turn on are the gate-drain capacitance ($C_{GD}$), and the turn-off resistance of the gate driver. If these factors can be addressed, the Miller turn-on and its resultant losses can be avoided. The third factor is the body diode, which is similar in operation to Si
MOSFETs, but has an entirely different working mechanism. Being a lateral device, the e-GaN FET has no parasitic pn-junction that causes reverse conduction. When the drain voltage drops by one threshold voltage, which can happen due to the presence of the inductor at the drain node, the gate will be positively biased with respect to the drain region injecting electrons below the gate. This creates a conducting channel that facilitates the reverse conduction, or the body diode conduction. As there are no minority carriers involved, there is no reverse recovery loss. As in Si MOSFETs, this drop has to be minimized to achieve minimum loss.

Numerous architectures have been introduced for driving e-GaN FETs. The very basic configuration utilizes a divided capacitor type of structure in which the capacitor charges during the on-time period of the switch, and uses this voltage as a negative voltage to quickly turn off of the e-GaN FET. Active discharge type [21] clamps this negative voltage to 0V by the addition of a PFET and a few passives, thus reducing the reverse conduction loss. Inverted type [22] is an improvement over the active discharge type with further reduction in the reverse conduction loss and fewer passives. Capacitor-less gate drive [23] is derived from the active discharge type by introducing a MOSFET as a capacitor. This method is seen to have significant lower loss than other gate drives, and the absence of capacitors makes it the apt choice for integration. However, these architectures do not satisfy the voltage requirement for the e-GaN device, and with the exception of the capacitor type, none of these gate drives can be integrated on a chip. The diode characteristic at the gate of the device is mitigated by limiting the current drawn at the gate by introducing a large resistance in series with the gate at the instance of device turn-on and, afterwards shorted out from the driver circuitry during turn-off. Figure 19 (taken from
[23]) compares the power loss compared among the architectures discussed in the literature [23].

![Comparison of Gate Drive Architectures](image)

**Figure 19: Comparison of Gate Drive Architectures [23]**

Commercially available drivers for e-GaN FETs utilize advanced packaging techniques that exhibit very low inductance and enable low parasitic PCB inductance, but these commercial solutions are designed for larger devices and lower frequencies. The driver itself adds a significant capacitance overhead to the e-GaN FET that affects the converter’s high frequency performance. Additionally, the large capacitance across the on-chip bootstrap diode adds losses. Moreover, the gate driver requires a linear regulator outside the driver IC to supply a constant 5V to the IC.

The gate leakage current is the main factor contributing to the increased gate drive losses. This is due to the diode-like characteristic exhibited by the gate-source of the e-GaN, as shown in Figure 18. All the current architectures concentrate on reducing the leakage current by using current limiting resistors. Instead, proposed architecture operate
the gate drive around 5V to effectively reduce the gate leakage. This is achieved by using an on-chip auxiliary regulator to keep the gate driver voltage regulated at 5V. Figure 20 shows the block diagram of the proposed architecture. The auxiliary regulator generates 5V from $V_{PV}$, and this 5V is used to power all the blocks shown in Figure 20. The MPPT control output (duty-cycle control) from the MPPT block is compared with a sawtooth waveform to generate PWM pulses of varying duty-cycle. The signal is sent to a dead time control unit that generates complementary PWM signals with a dead-time inserted, which can be adjusted from outside the IC. The high side signal is level shifted to switch between 36V and 41V, which is sent to the final delay compensated gate drive. The low side has a circuit similar to level shifter to compensate for the delay in the high side. Each block in the diagram is explained in detail in the following sub-sections.

Figure 20: Block Diagram of the Proposed Gate Driver

4.1. Auxiliary Regulator

The proposed driver requires a regulated voltage to supply the 5V required to drive the e-GaN FETs with a regulated 5V. Both switching converters and linear regulators were explored as solutions to create the auxiliary regulator. A buck converter with type II
controller was designed, and gives a good response for DC loads, but when the load is switched at frequencies well above the switching frequency of the buck converter itself, the loop cannot supply the current and the regulated output voltage droops. Also, for the buck converter to work in continuous conduction mode (CCM) mode of operation, the converter requires a dc load current of at least half the current ripple. This makes it difficult to design a stable buck converter for the dynamic load requirements of the gate driver.

A linear regulator satisfies the requirements for this case, but the loop bandwidth must be sufficient to avoid droop in the output voltage, while supplying the gate driver. The gate driver consumes significant current due to transient spikes during charging and discharging the capacitance associated with the gate driver and the gate capacitance for the e-GaN device. Current spikes can be as large as 1 to 5A for a timespan of ~1 to 2 ns. Both the NMOS and PMOS pass transistor type regulators were compared for implementation. The high current requirement makes it difficult to design the PMOS type regulator without a significant droop at the output. An NMOS type regulator has the following advantages over the PMOS type 1) better PSRR, 2) higher bandwidth, 3) better stability, and 4) ease of compensation. The lower output impedance of the NMOS regulator (source follower configuration, load connects to the source) creates the dominant pole at a higher frequency compared to the PMOS regulator (common-source configuration, load connects to drain). But the disadvantages include larger dropout compared to PMOS, which can go as low as $V_{DS_{sat}}$, where $V_{DS_{sat}}$ is the minimum drain-to-source voltage required to keep the pass transistor in saturation. For the proposed topology, the output voltage of the regulator is 5V, while the input voltage is 12V, hence a large voltage of approximately 7V drops across the pass transistor. Since the average current supplied by the regulator is significantly low
compared to the transient current, this dropout doesn’t significantly affect the efficiency. Another disadvantage of the NMOS type regulator is that the voltage (Vg) at the gate of pass transistor is higher than the output voltage and can even increase to values above the supply voltage. So, a charge pump may be required to boost the error amplifier output voltage above the power supply. In this work, a charge pump is not required since the supply voltage is around 7V above the output voltage, and the $V_{th}$ of the HV FET is around 2.5V. Figure 21 shows the implementation diagram of the NMOS pass transistor type linear regulator. The output is sampled using a potential divider and fed back to the inverting terminal of the operational amplifier (op-amp). The fed back signal is compared with a fixed reference of 2.5V (supplied externally to the IC), to generated an error signal to regulate the output voltage.

\[
\frac{V_{PV}}{R} = \frac{V_{REF}}{2.5V} \quad \text{and} \quad \frac{V_{PV}}{R} = \frac{V_{OUT}}{5V}
\]

![NMOS Type Linear Regulator](image)

**Figure 21: NMOS Type Linear Regulator as the Auxiliary Supply**

A large capacitance of 4.7µF is connected to the output of the regulator, which acts as a local battery to the load. Sudden changes in load (high frequency content) are supplied by the capacitor. The auxiliary regulator also supplies the MPPT circuitry. The regulator uses a folded cascode OTA with a PMOS buffer as the error amplifier. All the circuits were
built in 20V HV CMOS devices. As there are no bias generators before this auxiliary supply, there is a self-biased beta multiplier designed to supply current to the regulator. Figure 21 shows the output voltage droop with respect to changes in load current spikes of 1A. The output voltage ripple is 4mV_{PP}.

![Figure 21: Output Voltage Droop](image)

**Figure 22: Transient Response of the Auxiliary Regulator to Current Spikes**

### 4.2. Sawtooth Waveform Generator

The driver consists of a sawtooth waveform generator, which has a constant current charging a capacitor, and discharges it abruptly when an upper voltage limit is reached. The sawtooth generator is designed for four frequency modes, selectable using two pins. The control signal from the MPPT circuitry is compared with the saw-tooth generator output using a fast comparator to generate the PWM control signal. Figure 23 shows the implemented sawtooth waveform generator architecture.
A tunable delay circuitry converts the PWM control signal from the comparator to complimentary PWM signals with four selectable dead-time delays for 1MHz, 5MHz, 10 MHz and 20MHz operation. The dead-times are optimized to minimize the switching losses.

4.3. Level Shifter

The high-side signal has to be level shifted to drive the high side e-GaN HEMT with respect to the switching node. The voltages associated with the switching node and high side drive are too high for the 5V devices associated with the chosen process, hence 20V isolated well, mid-gate oxide devices were used to build the level shifter [24]. Figure 22 shows the level shifter with M1, M2, M3 and M4 HV isolated extended drain transistors M5, M6, M7 and M8 and the gates are low voltage isolated transistors. The level shifter below draws no static supply current and doesn’t require HV capacitors. All devices are placed in N-wells. NMOS transistors are placed in P-wells inside N-wells. Dashed boxes indicate separate N-wells. The separate N-wells allow the devices to be operated at higher voltages with respect to the common p-substrate without damaging the devices. Moreover,
the NMOS devices will have separate local body connection that allows the shorting of source to body, hence avoiding the body effect losses. This also reduces noise coupling between all the devices as they are not connected to the same substrate directly as in normal CMOS process. But these wells add significant parasitics that can hinder performance at high frequencies, if not designed with care.

A typical low-voltage level shifter consists of two pulldown transistors connected to a cross-coupled PMOS latch. For the high voltage version, M1 and M2 are HV devices directly used as pull downs instead of a cascoded structure. M3 and M4 are also HV transistors that protect the floating LV circuitry formed by M7 and M8. M5 and M6 are added to prevent the sources of the HV PMOS transistors being pulled more than a diode drop below V_Lx, which is the switching node. Hence, they actively pull down the source voltages of the HV PMOS transistors to the V_Lx node. Therefore, the transistors M5/M6 and M7/M8 pairs form two latching inverters with the HV PMOS devices M3 and M4.

Figure 24: High Voltage Level Shifter
At higher frequencies the delay of the level shifter is significant enough to create a delay between the high side and low side paths. So a delay match circuit with similar topology is introduced in the low side path as shown in Figure 21.

4.4. Final Driver Stage

The e-GaN device has an input capacitance \(C_{iss}\) of 45pF. The gate driver circuit charges and discharges this capacitance to switch the e-GaN device on and off. In order to switch the device with high slew rate, the transient current requirement will be high. There will be significant power loss due to the shoot through current in the final driving stage that needs to be taken care. The cross connected NOR-NAND structure shown in Figure 25 introduces a delay between the gate signals going to the PMOS and NMOS of the final inverter driving the e-GaN device(s). Hence either of the devices turn-on only after the other one turns off, hence avoiding shoot through losses.

![Figure 25: Delay Compensated Gate Drive](image)

Figure 25: Delay Compensated Gate Drive
An optimum delay of 320ps is introduced to ensure minimum losses from shoot-through current. The Figure 24 shows the simulated delay introduced in the path of the high side PMOS and low side NMOS of the final stage.

![Image](image.png)

**Figure 26: Delay Compensated Circuit Simulation**

The on-state resistances of the NMOS and PMOS drives were designed for minimum loss and also to prevent the Miller turn ON. A carefully designed bootstrap circuit with clamp ensures that the voltage across the floating capacitor remains below 5V. The presence of parasitic inductances at the switching nodes can create negative voltages, causing the bootstrap capacitor to charge beyond the designed 5V. The presence of a separate gate return ensures that the loop inductance is outside of the gate driver loop, hence avoiding any unnecessary ringing in the gate drive pulses.
5. RIPPLE CORRELATION CONTROL

Every PV system is faced with the problem of operating the system under maximum power point. Under varying temperature and irradiance, the maximum power point of the panel varies as shown in Figure 4 and Figure 5. The problem considered by various MPPT techniques is to find the voltage $V_{MPP}$ or current $I_{MPP}$ at which a PV array should operate to obtain the maximum power output $P_{MPP}$ under a given temperature and irradiance. Under shading conditions, there are cases that can produce multiple local maxima, but there remains only one maximum power point. There are a plethora of proposed algorithms to find the MPP, but the most popular ones are the hill climbing, perturb and observe (P&O), and the Incremental Conductance. Hill climbing technique [48-50] uses a perturbation in duty ratio of the power converter, and observe the movement of the power. If there is an increase in power, the subsequent perturbations should be kept the same, and if there is a decrease in power, the perturbations should be reversed. P&O technique [51-53] uses perturbations on voltage to reach the MPP. Hill climbing and P&O methods are different ways to envision the same fundamental method. Incremental conductance method [54, 55] utilizes the property of the PV power curve that the slope of the curve is zero at the MPP, positive at the left of MPP, and negative at the right of MPP. There has been various other techniques derived from these three techniques, but they use an external perturbation to see whether the output power moves towards or away from the Maximum Power Point.

Ripple Correlation Control (RCC) is a fast analog MPPT technique that relies on the converter’s voltage and current ripple to track the MPP. Switching converters inherently contain current and voltage ripple, due to their switching behavior. RCC correlates the time derivative of power to the time derivative of voltage (current), hence
driving the power gradient to zero. As RCC uses the ripple, which has the same frequency as the switching frequency, the RCC convergence is at a rate that is only limited by the switching frequency, thus making it faster than other MPPT techniques.

Figure 27: P-V Derivatives on a P-V Characteristics

Moreover, its simple implementation made possible by using analog circuits makes RCC an attractive technique for low power applications. Another advantage of the technique is that it does not require external perturbation as done in other techniques [16].

Figure 27 shows the PV derivatives at the left and right of the MPP. The goal of the algorithm is to force \( V_{PV} \) to track \( V_{MPP} \), which is the voltage at the MPP, as quickly as possible irrespective of temperature, irradiance or other variations. The voltage across the PV, \( V_{PV} \) is composed of average value \( V_{PV} \) and ripple \( \tilde{V}_{pv} \). Similarly, the current out of PV, \( I_{PV} \) is composed of average value \( I_{PV} \) and ripple \( \tilde{i}_{pv} \). At a given irradiance and temperature, \( I_{PV} \) is adjusted and the power flow, \( P_{PV} = V_{PV}.I_{PV} \) varies. The power is composed of average value \( P_{PV} \) and ripple \( \tilde{p}_{pv} \).
From inspection of Figure 27, when the $V_{PV}$ is below MPP, a voltage ripple imposed along the curve leads to an in-phase power ripple; this implies that the time derivative of $V_{PV}$ and the time derivative of $P_{PV}$ is positive. When the $V_{PV}$ is above MPP, both the voltage and power ripple are out of phase and the product of $dV_{PV}/dt$ and $dP_{PV}/dt$ is negative.

\[
\frac{dP_{PV}}{dt} \frac{dV_{PV}}{dt} < 0, V_{PV} > V_{MPP}
\]

\[
\frac{dP_{PV}}{dt} \frac{dV_{PV}}{dt} > 0, V_{PV} < V_{MPP}
\]

This forms the basis of RCC law. If the input current $I_{PV}$ decreases when the product is greater than zero and increases otherwise, then $V_{PV}$ should approach $V_{MPP}$. This is done by integrating the product as:

\[
d = -K \int \frac{dP_{PV}}{dt} \frac{dV_{PV}}{dt} dt
\]
Where \( d \) is the duty cycle of the PWM that drives the switch and \( K \) is a constant positive gain. The inductor current increases and decreases as the duty cycle \( d \), so adjusting \( d \) should provide the correct movement of the power, \( P_{PV} \) toward the MPP.

There are several papers in literatures that resemble RCC. [44], and use the polarity of time derivatives of power and duty ratio. However, they require external perturbation of the duty ratio to generate a disturbance in power. [45] and [46] use a hysteresis version of RCC. A low frequency dithering signal is used as perturbation in [47]. The RCC technique used in this work is the fastest technique currently available, and will be particularly suitable for fast changing environments. Also RCC is parameter insensitive and the application is independent of solar array/panel configuration. The challenge is the implementation of RCC at 20MHz frequency, at which the ripple voltage becomes significantly small. Also all the circuits has to maintain high bandwidth in order to process the ripple signal.

5.1. Block Level Simulation

The RCC algorithm shown in Figure 28, was initially implemented using Matlab/Simulink as shown in Figure 29. The simulink diagram shows the RCC algorithm implemented using ideal components to verify that the algorithm accurately and quickly tracks the MPP.
5.2. Circuit Implementation

The heart of the algorithm is a multiplier, which finds the product of the current and voltage from the sub-panel, while providing a bandwidth high enough so not to filter out the ripple in the input signal. Both the DC and AC part of the input current and voltage are required to achieve the convergence. This is proved mathematically by Midya [56].
Figure 30: Block Diagram of the Ripple Correlation Control

The output of the multiplier, $P_{pv}$, and the sub-panel voltage, $V_{pv}$, are differentiated with single ended differentiators having cutoff frequencies of 100MHz. The output of the differentiators are square waves of very small amplitude because of the very low amplitude of the input signal and the attenuation of the multiplier. These signals are scaled up using cascaded amplifiers with high bandwidth and eventually buffered using inverters to get square waves with sharp edges, whose phase information are converted into duty cycles. The voltage branch is faster due to the absence of the multiplier. The multiplier adds significant delay to the power branch. To compensate for the delay of the multiplier, additional delay is added in the voltage branch with tunability.
The square wave signals from both the voltage branch and power branch are XOR-ed to achieve the product of the expression $\frac{dP_{pw}}{dt} \ast \frac{dV_{pv}}{dt}$. Depending on the sign of this product, the duty cycle is adjusted. If the product is negative, the duty cycle is increased, and if the product is positive, the duty cycle is decreased. This is achieved by adding an integrator after the XOR gate. The time constant of the integrator can be adjusted to vary the speed of the MPP convergence.

![Multiplier Circuit Diagram](image)

**Figure 31: Multiplier Circuit Diagram**

The multiplier design is based upon the design presented in [30]. It is used to multiply the PV sub-panel sensed voltage signal and the output of the current sense op-amp, which represents the PV instantaneous current, to get the power of the PV. The multiplier output can be calculate as:

$$V_{out} = \frac{\mu \cdot C_{ox}}{8} \ast \left( \frac{W}{L} \right) \ast V_{PV} \ast I_{PV}$$

Where Vpv andIpv are the input signals of the multiplier, and W/L is the aspect ratio of the transistors M1, M2, M3 and M4 in the Figure 31.
6. RESULTS

The designed power management IC was fabricated in the AMS HV 180nm process [40]. The physical layout of the full chip is shown in Figure 32. The total size of the full-chip is 2000\(\mu\)m X 2000 \(\mu\)m (2 mmX2 mm).

A single PCB board was fabricated to include the boost converter, designed power management chip, and the current sense circuits. Figure 33 shows the switching converter with the e-GaN devices zoomed-in. The board has 4 layers to allow multiple planes to handle up to 60W of power. Significant care was taken to minimize parasitic inductances in the layout. The common source inductance and the power loop are physically made small by good layout techniques [55], hence reducing the effective inductances. The high
frequency power loop involving the e-GaN HEMTs and the output capacitor are laid out on the top layer in close proximity and the return path to this power is routed in the 2nd layer, hence achieving the smallest physical loop size. These techniques reduce parasitic loop inductances and also help in reducing EMI.

Figure 33: Photo of the Designed PCB Board

The sawtooth generator and the auxiliary supply were initially tested without enabling the boost converter. Once the desired functionality was ensured, the driver was tested and the power consumption at desired frequencies were measured. The gate driver loss is plotted and compared with other architectures in Figure 34. The presented gate drive circuitry has significantly lower losses than the state of the art gate drives for e-GaN. Also the gate drive facilitates operation at higher frequencies than the available commercial driver ICs, with minimum bootstrap losses, and inductive losses
The boost converter was then tested for various frequencies to check the efficiency using a fixed DC power supply. The simulated results are plotted in Figure 35. The decrease in the efficiency at increased frequencies is due to the increase in switching losses.
The system was examined under various irradiation levels to confirm the functionality of the developed MPP control algorithm. Figure 36 and Figure 37 shows the system simulation results under different irradiation levels, specifically 1000W/m² (100% irradiance), 750W/m² (75% irradiance) and 500W/m² (50% irradiance).

Figure 36: Input Power and Output Power under Different Irradiations Levels
Figure 37: MPPT Output Voltage and Output Current under Different Irradiation Levels

Figure 38 shows the regulated 5V at the output of auxiliary regulator with negligible ripple even in the presence of switching loads. A voltage to current converter (V to I), is used to generated bias for all the internal circuitry from an external $V_{\text{ref}}$ voltage. Figure 38 shows that the V to I input node is closely tracking the 2.5V reference, ensuring the proper functioning of the bias circuitry.
Figure 38: Auxiliary Regulator and V-to-I Node Voltage

Figure 39 and 40 shows the measure gate drive signals at 1MHz and 20MHz respectively.

Figure 39: Gate Drive Signals Measured at e-GaN Gate @ 1MHz
Figure 40: Low Side Gate Drive Signal Measured at e-GaN Gate @ 20MHz

A summary of the achieved system performance is given in Table 4.

<table>
<thead>
<tr>
<th>Parameters</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Switching frequency</td>
<td>20 MHz</td>
</tr>
<tr>
<td>Maximum sub-panel input power</td>
<td>65 W</td>
</tr>
<tr>
<td>Converter output power</td>
<td>59.86 W</td>
</tr>
<tr>
<td>Maximum converter efficiency</td>
<td>92.5 %</td>
</tr>
<tr>
<td>MPPT tracking time</td>
<td>600 $\mu$s</td>
</tr>
<tr>
<td>MPPT tracking efficiency</td>
<td>98%</td>
</tr>
</tbody>
</table>

Table 4: System Performance Parameters
7. CONCLUSION AND RECOMMENDATIONS

The design of a high efficiency, 20MHz, small form-factor, hybrid GaN-CMOS DC-DC Maximum Power Point Tracker (MPPT) for a 12V/5A sub-panel is presented. This work pushes the limit of hard switching converters to higher frequencies with efficient gate drives. A completely analog implementation of RCC MPPT with very high dynamic performance is presented in this work. The RCC and custom gate driver were fabricated in an HV AMS 180nm process. The dynamic performance of the implemented RCC MPPT, power efficiency of the 20MHz boost converter, and the power efficiency of the gate driver illustrate an integrated system with highest-reported efficiency at 20MHz switching speeds. In conclusion, an integrated silicon solution of size 2mm x 2mm was developed for efficiently driving an e-GaN power stage.

This research is the first step to efficient integration of medium power converters for solar applications. The future recommendations are given below.

7.1. Recommendations

- Higher levels of integration for both the e-GaN FETs and the silicon CMOS gate drivers (for driving more than 2 devices).
- Higher frequencies with newer generations of e-GaN FETs. Gate drive controllers implemented using standard CMOS processes, rather than high-voltage CMOS.
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