Electrostatic Analysis of Gate All Around (GAA) Nanowire over FinFET

by

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ABSTRACT

CMOS Technology has been scaled down to 7 nm with FinFET replacing planar MOSFET devices. Due to short channel effects, the FinFET structure was developed to provide better electrostatic control on subthreshold leakage and saturation current over planar MOSFETs while having the desired current drive. The FinFET structure has an undoped or fully depleted fin, which supports immunity from random dopant fluctuations (RDF – a phenomenon which causes a reduction in the threshold voltage and is prominent at sub 50 nm tech nodes due to lesser dopant atoms) and thus causes threshold voltage ($V_{th}$) roll-off by reducing the $V_{th}$. However, as the advanced CMOS technologies are shrinking down to a 5 nm technology node, subthreshold leakage and drain-induced-barrier-lowering (DIBL) are driving the introduction of new metal-oxide-semiconductor field-effect transistor (MOSFET) structures to improve performance. GAA field effect transistors are shown to be the potential candidates for these advanced nodes. In nanowire devices, due to the presence of the gate on all sides of the channel, DIBL should be lower compared to the FinFETs.

A 3-D technology computer aided design (TCAD) device simulation is done to compare the performance of FinFET and GAA nanowire structures with vertically stacked horizontal nanowires. Subthreshold slope, DIBL & saturation current are measured and compared between these devices. The FinFET’s device performance has been matched with the ASAP7 compact model with the impact of tensile and compressive strain on NMOS & PMOS respectively. Metal work function is adjusted for the desired current drive. The nanowires have shown better electrostatic performance over FinFETs with excellent improvement in DIBL and subthreshold slope. This proves
that horizontal nanowires can be the potential candidate for 5 nm technology node. A GAA nanowire structure for 5 nm tech node is characterized with a gate length of 15 nm. The structure is scaled down from 7 nm node to 5 nm by using a scaling factor of 0.7.
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CHAPTER 1. INTRODUCTION

The first Bipolar Junction transistor shown in Fig. 1.1 was built in 1948 at Bell labs. Later, in 1958, Texas Instruments demonstrated their first integrated circuits. Gordon E. Moore, one of the founders at Intel, had observed the ongoing trend of the integrated Circuit development and noted that the number of transistors in a fixed die area will double in every 18-24 months [Moore98]. Several scaling laws were emerged after Moore’s prophecy. Dennard’s scaling is one of those stated scaling laws [Dennard74]. In today’s semiconductor devices, more importance is given to the speed and battery life of the device. On a fixed die, higher the number of transistors fabricated, higher are the functions to build on it.

![First Transistor Made in Bell Labs in 1948](image)

*Fig. 1.1 First Transistor Made in Bell Labs in 1948.*
1.1. Dennard’s Scaling Law

Following the Moore’s prophecy, Dennard’s Scaling law states that the transistors become faster, consume less power, and are cheaper to manufacture as they shrink. Thus, the Operational characteristics of a MOS transistor can be preserved and the performance is improved if the critical parameters are scaled down by a factor of “S” [Weste10].

– Critical Parameters:
  - Device dimensions
  - Device voltages
  - Doping densities

![Fig. 1.2 Power Dissipation Over the Years. [Nikolic2008]](image)

It is also known as the constant field scaling as both power supply and device dimensions scale down. Power dissipation is becoming a major concern with the current market scenarios. With the current scaling trend, power dissipation for every transistor reduces by a factor of two keeping the frequency constant. In order to support the power scaling, the power supply should be reduced. However, with the $V_{dd}$ scaling, threshold voltage ($V_{th}$) should also scale simultaneously to maintain the drive current. But $V_{th}$ does
not follow the scaling trend as expected. Power dissipation has increased drastically until the early 2000’s due to frequency increase with considerable pipelining [Nikolic08]. Fig. 1.2 shows how the power dissipation increases almost linearly till the year 2000.

1.2. Challenges with Scaling trend

As there is a limit to everything, transistors cannot be fabricated smaller than atomic size. From 45 nm Technology node, designers are making trade-offs between power and delay since further scaling has been slowed down. Below ~32 nm, it became difficult to follow Moore’s law and scale down further with the planar MOSFET devices. A lot of techniques had been introduced to keep this trend alive to allow more advanced nodes.

Fig. 1.3 Industry Scaling Trend Over the Years.
Researchers have generated lots of plots depicting scaling trends over the years showing the limit of critical dimension. Fig. 1.3 from Applied Materials, shows channel length scaling over the years. In this, it can be observed that at \( \sim 45 \) nm \( L_{\text{gate}} \), conventional planar transistors were incapable of being scaled down further due to several different causes including electrostatic scaling problems and degradation of DIBL. To overcome this, various solutions and suggestions proposed by the researchers were thin channel devices such as FinFETs and ultrathin-bodied silicon-on-insulator (SOI) transistors.

Apart from these performance issues, there was one more challenge present in front of the semiconductor industry, the fabrication of such advanced node devices. The existing lithography machines and techniques were not capable to fabricate sub 90 nm device.

1.2.1. Immersion Lithography

According to the scaling law of resolution [Lin15],

\[
W = K1 \left( \frac{\lambda}{NA} \right),
\]

Where,

- \( W \) is half pitch of the feature to be printed,
- \( k1 \) is the resolution scaling coefficient,
- \( NA \) is numerical aperture of the imaging lens,
- \( \lambda \) is the imaging wavelength.

At \( k1 = 0.28, \lambda = 193 \) nm, and \( NA = 1.35 \), the \( W \) is 40 nm. [Lin10]

Due to the wavelength of light, the allowed feature size is 40 nm, which makes a minimum pitch of 80 nm. Now, to go below 40 nm, various multiple patterning
techniques like litho-etch-litho-etch (LELE), litho-freeze-litho-etch (LFLE), self-aligned double patterning (SADP), self-aligned quadruple patterning (SAQP) has been suggested. These multi-patterning schemes come with a commensurate cost and hinder the reduction in cost per transistor with scaling.

1.2.2. Extreme Ultraviolet Lithography (EUV)

As a successor of Immersion lithography, EUV has a wavelength of 13.5 nm and can have a half feature size of 15 nm. But there are lot of challenges with EUV at present such as,

- Brightness of light source.
- EUV litho resist.
- Cost feasibility.

Because of these challenges, EUV is still under research.

1.2.3. Short Channel Effects

Planar MOSFET devices can be scaled down below 14 nm but their performance starts degrading. The main problems that came into light with these short channel lengths are the short channel effects which created the hindrance for planar MOSFET devices.

Short channel effects become significant when the channel length is of the same order of magnitude as the depletion layer widths of source and drain junctions.

1.2.3.1. DIBL and Punchthrough.

When voltage is applied between drain and source junctions in a MOSFET, the depletion region around the drain starts to expand and merges with source. At this point the flow of charge carriers are controlled more by drain voltage than the gate voltage. This is known as punch through. The electric field under the gate then depends on the
drain voltage. Source and drain (S/D) regions form reverse biased p-n junction diodes with the body of the MOSFET and thus a depletion region is present around both the regions. In long channel devices (devices that do not come under short channel regime), the depletion region of source and drain does not play any important role as both Xd_S & Xd_D (width of the depletion region of source & drain) are very small compared to the channel length. But as we enter into short channel regime, the depletion region widths of S/D region are no longer negligible as compared to the channel length. With increasing voltage on the drain terminal, the width of drain depletion region increases, reducing the effective channel length which is known as DIBL.

In normal MOSFET operation, gate voltage controls the potential barrier and causes the formation of the channel between source and drain. But in short channel devices, because of DIBL, drain to source voltage V_{ds} also impacts the barrier.

Due to a reduction in the potential barrier, electrons flow from source to drain even if the gate to source voltage (V_{gs}) is not present. As a result, the saturation current increases with a more positive slope in I_d-V_{ds} curve since current is inversely proportional to the channel length ‘L’.

![Fig. 1.4 Drain Current Vs Gate Voltage for Two Different Drain Voltages. [Weste10]](image-url)
Fig. 1.4 shows the impact of $V_{ds}$ on the threshold voltage of the device. Increasing the drain voltage lowers the $V_{th}$ and increases the current in saturation mode due to the shorter channel length.

1.2.3.2. $V_{th}$ Roll-off

![Graph showing the threshold voltage roll-off due to channel length.](image)

*Fig. 1.5 Threshold Voltage Roll-off due to Channel Length. [Saeidmanesh13]*

With MOSFET channel length reduction, the number of depletion charge carriers decrease, which leads to change in the threshold voltage. With the device scaling, dielectric oxide thickness is also getting scaled down to 1-2 nm. Due to this, lesser charge is required to invert the channel which results a decrease in the threshold voltage. Fig. 1.5 [Saeidmanesh13] shows the plot of the threshold voltage and channel length showing a variation of ~80 mV from 15 nm to 5 nm. As we are moving towards ~5 nm, there is a big drop in the threshold voltage which becomes worse by increasing the drain to source voltage ($V_{ds}$).
1.2.3.3. Subthreshold Leakage

In an ideal transistor, drain current should only be flowing when the gate voltage is greater than threshold voltage ($V_g > V_{th}$). But practically this is not the case. Current does not abruptly cut-off below threshold voltage but a small amount of leakage current flows between source and drain which is proportional to the drain to source potential difference. The inversion charge density does not drop to zero abruptly, instead, an exponential dependence on $V_g$ can be observed. When the gate voltage of the device is lesser than the threshold voltage, it operates in the weak inversion regime. Drain current has two components drift (current due to the movement of charge carriers under the influence of electric field) and diffusion (current due to the diffusion of charge carriers from higher concentration to lower concentration). In the weak inversion regime, diffusion current is the dominant factor and is the root of subthreshold leakage. When $V_{ds}$ reaches above few multiples of $KT/q$ (thermal voltage) the subthreshold current becomes independent of drain voltage. This happens because the diffusion current is the dominant current transport factor in sub-threshold regime [Weste10].

$$\text{Ids} = \text{Ids}_0 e^{-\frac{V_{gs}-V_{to}+\eta V_{ds}-\gamma V_{sb}}{nVT}} \left[1 - e^{-\frac{V_{ds}}{VT}} \right].$$

Where,

$\text{Ids}$ is subthreshold leakage,

$\text{Ids}_0$ is drain current when gate voltage is equal to threshold voltage of the MOSFET,

$n$ is process dependent term,

$\eta V_{ds}$ is the DIBL factor,

$\gamma V_{sb}$ is parameter for body biasing,
\( v_T \) is thermal voltage (26mV at Room Temperature),

\( K \) is Boltzmann Constant,

\( T \) is temperature,

\( q \) is electrical charge of electron.

The subthreshold slope is an important factor of consideration for dynamic circuits and DRAMs. A rise in temperature decreases the threshold voltage and thus increases subthreshold leakage. With the scaled down power supply, subthreshold leakage of an OFF transistor discharges the storage capacitor in DRAM memories unless it is periodically refreshed. Leakage also contributes to power dissipation in idle circuits. As the threshold voltage \( V_{th} \) decreases, subthreshold leakage increases exponentially. At present, overcoming the power dissipation is one of the biggest challenges and subthreshold leakage is the most dominant factor of it. Industry is moving towards IoT (Internet of things), where devices operate at very low power. For technology nodes, where the threshold voltage is \( \sim 200-300 \) mV, the subthreshold leakage consumes a big amount of power.

Usually subthreshold leakage is measured by subthreshold slope (SS) as change in gate voltage \( (V_{gs}) \) per decade of drain current \( (I_{ds}) \). Units are mV/dec. The lower limit for the subthreshold slope has been measured as 60 mV/dec \((n.vT.ln(10))\).

**1.2.3.4. Velocity Saturation**

In the MOSFET, the drain current is composed of two components drift and diffusion. When the gate voltage is above the threshold voltage, the transistor operates in the strong inversion regime and drain current is dominated by drift factor. The drift velocity is directly proportional to the lateral electric field \( E_{lat} \) \( (= V_{ds} / L) \) between the
source and drain. The constant of proportionality is called the carrier mobility \((v = uE_{lat})\). The mobility of carriers is a constant parameter and thus velocity of carriers is supposed to vary linearly with the applied electric field. But with decreasing channel length, due to excessive collisions suffered by the charge carriers, mobility degradation occurs and velocity starts saturating after the critical electric field. A plot between velocity and the electric field has been shown in Fig. 1.6. Mobility is the slope of the curve, which starts decreasing after a critical electrical field is reached and the velocity of the device saturates to a constant velocity. A higher electrical field is required to saturate holes' velocity and thus PMOS transistors are less pronounced to this effect as compared to NMOS.

![Fig. 1.6 Saturation of Carrier Velocity due to Electric Field. [Rabaey03]](image)

1.3. Metal Gate

MOSFET got its name due to the use of the metal gate. Initially, aluminum was used as the gate material for traditional CMOS devices. But because of manufacturing processes operating at a very high temperature [Ahmad07], polysilicon was used as gate electrode due to its ability to withstand heat treatment in the process. The processes
switched to the dual work function doped polysilicon gate, due to its benefits in controlling short channel effects and threshold voltage [G06].

However, metals came back as gate material in the Intel’s 45 nm process nodes with high-K dielectric materials as gate oxide. Due to the application of gate voltage, doped poly-silicon (semiconductor) forms a depletion region, which acts as a thicker oxide reducing the inversion charge and a reduction in the drive current. Metal gates eliminates poly-depletion problem and results in an improved drive current [Mistry07].

1.4. Strain Effects

Introduction of strained Silicon in NMOS and PMOS in the Intel’s 90 nm process generation was a significant breakthrough. Tensile Strain can be added in NMOS by growing an epitaxial Silicon layer on a relaxed SiGe film. Compressive strain was added in PMOS by replacing the conventional source/drain region with strained SiGe (a process often called embedded-SiGe or e-SiGe). The addition of strain in these devices, enhanced the channel mobility, resulting in improved drive current for both NMOS and PMOS.

Adding strain in the silicon provides mobility improvement to the MOSFETs in two ways. By reducing the effective mass of the silicon and by moving carriers to places with good effective mass (or reducing movement of carriers to places with bad effective mass) [Intel08]. In typical NMOS transistors, having low effective mass of electrons in conduction band leads to better mobility which increases the ON current resulting in higher performance. This is one of the main reasons to prefer [100] surface on the wafer for building MOSFETS. For a surface with [100] lattice structure, channel orientation is along [110] [Obrad04] in which, only two of the ellipsoids of electron orbitals are aligned with low effective mass and the rest are having larger effective mass causing hindrance to
the mobility of the carriers. When the MOSFET is stretched by having a tensile stress along [110], the energy bands of the higher effective mass orbitals further split and align with the outer ellipsoids of lower effective mass. This increases the mobility of the carriers along the channel. Typically, over ~2 Gpa of stress, the majority of the electrons form the ellipsoids having lower effective mass. Similarly, for holes (in PMOS) having compressive strain along [110] will reduce the effective mass in the direction of hole propagation which results in a higher mobility among the carriers in PMOS [Mistry04].

According to [Gong13], compressive strain improves the hole mobility due to two major reasons. First, more band bending induced by uniaxial compressive strain causes reduced effective mass for the topmost valence band where holes primarily occupy, which leads to higher hole mobility. Second, the LH (Light Hole) and HH (Heavy Hole) band separation increases, which enhances the hole mobility. [Naka09] explains the strain effect on the band structure. Where he uses the deformation potential model to explain the band shifts in the conduction band and k.p Hamiltonian model for the valence band. Although the same models have been used to observe the effect of strain on the device current but studying the impact of strain on the device and its band structure is completely a different topic and is out of the scope of this project.

1.5. FinFET

To tackle the problem of short channel effects, Dr. Chenming Hu and his group proposed the structure of FinFET [Xuejue99] built on SOI. FinFET is a 3-dimensional multi (tri) gate device shown in Fig. 1.7. The metal gate controls the channel between source & drain called ‘fin’ from three sides. FinFET offers good scaling down capability
and has better performance (DIBL, SS, drive current) in high speed digital integrated circuits than planar MOSFET devices.

**Fig. 1.7 Tri-Gate FinFET Structure.**

Due to the better gate control on the channel and potential barrier, FinFET seemed to be a promising structure. As fins (channel) are surrounded from three sides by the gate, effect of DIBL is comparatively lesser than planar MOSFET device. FinFETs have lesser subthreshold leakage than planar devices, leakage due to parasitic capacitance can be controlled in FinFET devices.

With the current technology demand, the maximum operating frequency of the microprocessors has been limited by the power dissipation and power density. To achieve the same number of tasks, multi-core microprocessors have taken the place of single-cores. But with the advanced nodes, existing cooling systems are not sufficient for the
multi-core processors. Leakage due to parasitic capacitance can be controlled in FinFET devices, which makes it better than planar device [Sachid12].

Due to the 3-dimensional structure, FinFET has more effective width than planar MOSFET in the same device width and thus has more drive current.

![Image](image1.png)

*Fig. 1.8 Multi-Gate Structures available in BSIM Models.*

Fig. 1.8 shows the possible structures available in BSIM-CMG models [BSIM12], which can be set by the Hspice model parameter ‘GEOMOD’. For nanowire, we need to set it to ‘3’. The used structures for this project are FinFET (GEOMOD =1) and cylindrical nanowires (GEOMOD =3).

Table 1-1 presents the parameters that Hspice uses for the effective width calculation. The values present in the table are taken from the Arizona State Predictive PDK-ASAP7 [Clark16] 7 nm FinFET device.

\[
GEOMOD = 1 \text{ for FinFET.}
\]

\[
W_{eff0} = 2 \times H_{FIN} + FECH \times T_{FIN} - DELTAW
\]

\[
W_{eff0} = 2 \times 32 + (1 \times 6.5) - 0.0 = 70.5 \, \text{nm}
\]

The effective width of the conducting channel for ASAP7 FinFET device is calculated as 70.5 nm.
<table>
<thead>
<tr>
<th>NAME</th>
<th>UNIT</th>
<th>DEFAULT</th>
<th>MIN</th>
<th>MAX</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>HFIN</td>
<td>m</td>
<td>30 nm</td>
<td>1e-9</td>
<td>-</td>
<td>Fin height</td>
</tr>
<tr>
<td>FECH</td>
<td>-</td>
<td>1.0</td>
<td>0</td>
<td>-</td>
<td>End-channel factor, for different orientation/shape (Mobility difference between the side channel and the top channel is handled by this parameter)</td>
</tr>
<tr>
<td>DELTAW</td>
<td>m</td>
<td>0.0</td>
<td>-</td>
<td>-</td>
<td>Reduction of effective width due to the shape of fin</td>
</tr>
<tr>
<td>Tfin</td>
<td>m</td>
<td>15 nm</td>
<td>1e-9</td>
<td>-</td>
<td>Fin thickness</td>
</tr>
<tr>
<td>D</td>
<td>m</td>
<td>40 nm</td>
<td>1e-9</td>
<td>-</td>
<td>Diameter of cylinder (for GEOMOD=3) Currently using D = 8 nm</td>
</tr>
<tr>
<td>DELTAWCV</td>
<td>-</td>
<td>0.0</td>
<td>-</td>
<td>-</td>
<td>CV reduction of effective width due to shape of Fin</td>
</tr>
</tbody>
</table>

Table 1-1 Compact Models Parameters of FinFET and Nanowire [BSIM12].

1.6. Nanowire

Looking at the next CMOS technology generation, scalability of thin body devices like FinFETs is under the question whether these devices can maintain the subthreshold slope and short channel effects like DIBL [Huynh-Bao16] at 5 nm technology node. Horizontal GAA nanowire can be considered as the better structure than FinFET (both have fully depleted channel). The nanowire is not yet a matured structure and is still under research. Researchers have suggested horizontally and vertically stacked nanowires with a gate all around structure. To provide the competitive drive current, multiple nanowires are stacked together to increase the effective channel width. The nanowire FET (NWFET) have better gate control on the channel which leads to lower DIBL and lower subthreshold leakage as compared to FinFET.

Fig. 1.9 shows two vertically stacked nanowires 3-D structure. The conducting channel region is wrapped by a thin oxide layer of SiO₂ and high-K dielectric HfO₂
layers. Due to the surrounding of the metal gate, nanowires show better gate control and lower DIBL.

![Nanowire Structure](image)

*Fig. 1.9 Nanowire Structure.*

A large number of techniques have been developed in different research labs to fabricate Si nanowires [Zhuge10] [Sacch09] [Gu12]. Which we can classify into bottom-up and top-down fabrication techniques. In top-down fabrication, fabricated structure is defined by the lithography that is then transferred from the photo-resist to the substrate by etching or a similar way of structuring with an already available material. In the bottom-up approach, the material is added to the substrate in a self-organized way [Ke15].

For the current research, vertically stacked horizontal nanowires have been studied. Fig. 1.8 shows three types of FET devices that we can use for the FET structure for SPICE simulations [BSIM12]. The first structure is the FinFET structure. Second & third presents the nanowire structure.

*For GAA nanowire, GEOMOD = 3 [BSIM12]*
\[ R = \frac{D}{2} \]  
(Considering a Diameter = 8.0 nm for nanowire)

\[ W_{\text{eff0}} = \pi D - \Delta W \]

\[ W_{\text{eff0}} = 3.14 \times 8 - 0.0 = 25.12 \text{ nm} \]

[Ferry08] demonstrate how the diameter limitation of nanowire can cause a surface area wastage of Si and will not satisfy the law regarding the cost of Si real estate. According to this law, the effective width of nanowire (or transistor periphery) should be greater than pitch of the device (W). Fig. 1.10 shows the nanowire on Si surface with the transistor pitch W.

![Diagram of nanowire on silicon surface](image)

*Fig. 1.10 Nanowire on Silicon Surface [Ferry08].*

Below equation must be met to fit the wire in the given pitch,

\[ d > \frac{2(t_{\text{ox}} + t_G)}{\pi - 1} \]

Where,

- \( d \) is the diameter of nanowire,
- \( t_{\text{ox}} \) is the thickness of oxide thickness,
\[ t_G \] is the thickness of the metal gate.

This equation poses a fact that diameter of nanowire should be greater than or equal to 5 nm. Which is true, but vertical stacks of nanowires [Singh08] [Gu12] shown in Fig. 1.9 could be a solution of this limitation. Stacking increase the effective width of device and can satisfy the law regarding the cost of Si real estate. A vertical stack of 2 nanowires (with a diameter of 8.00 nm) has an effective width of 50.00 nm, which can compete the FinFET in both drive current and Si cost.

![Image](image.png)

**Fig. 1.11 Impact of Uniaxial Strain on Drive Current and \( V_{th} \) [Hashemi08].**

[Hashemi08] discusses about the impact of strain on the \( I_{d_{\text{lin}}} \) and \( I_{d_{\text{sat}}} \) and made an argument that drive current enhancement is almost 2x (Fig. 1.11) in linear region as compared to saturation. For \( I_{d_{\text{sat}}} \), because of an increase in the series resistance caused by high resistivity of ultrathin body of S/D, the enhancement is slightly degraded. Due to the presence of uniaxial stress, the threshold voltage also shifts by 0.1 V as expected which is attributed to lowering in conduction band edge. But the devices that they manufactured
and used for analysis has gate length of 0.5 to 4 um. The reported 1.95x current drive improvement is for \( L_{\text{gate}} \) 1.0 um and thickness of 8 nm and width of ~20 nm.

[Hash08] analyzed a nanowire structure strained to 2.2 GPa, fabricated by a bond and etch back technique. Using e-beam lithography, dense nanowires with widths of 20 nm to 60 nm were created. The nanowire length varied from 0.4 to 4 um, which showed ~2x increase in drain current.

All of these analyses were done on long channel devices. And thus, the improvement of 2x cannot be promised on the short channel devices at 7 nm or 5 nm technology nodes. [Cheng13] used a device with gate length of 120 nm and wire width of 7.5 nm. They reported a drain current improvement of around ~35\% instead of 2x reported for longer channel devices.
CHAPTER 2. TECHNOLOGY COMPUTER AIDED DESIGN (TCAD)

Technology Computer-Aided Design (TCAD) refers to the use of computer simulations to develop and optimize semiconductor processing technologies and devices. It can be used for various device technologies including CMOS, Memories and Solar cells etc.

**Fig. 2.1 Sentaurus TCAD Flow for Device Simulations.**

Synopsys Sentaurus TCAD tools are used for the device simulations in this project. Although for accurate performance measurement, the suggested method should be the process simulation but device simulation can also provide the required data if we are not interested in the device fabrication methodologies and various defects. Fig. 2.1 shows the complete TCAD flow that have been used for this project. It shows all the required steps for the device simulation. Sentaurus ‘svisual’ is also used for taking the
doping plots but that is not necessary for the device simulation and analyzing the current curves and extract the required parameters.

Using a PERL script length of the gate ($L_{gate}$) is changed from 13 nm to 23 nm by changing the width of the spacers. The critical poly pitch (CPP) is kept constant at 54 nm. Also, the S/D extension of 15 nm is not changed. The script calculated all the dimensions of gate length and spacers dynamically and provides the new command file to the Sentaurus Structure Editor (SDE). It feeds the structure created by SDE to the device simulator sdevice as shown in Fig. 2.1.

2.1. Sentaurus Structure Editor

FinFET and nanowire structures have been created using Sentaurus Structure Editor. All the dimensions of shapes have been matched with the ASAP7 PDK FinFET structures. Both NMOS and PMOS FET has been created. Table 2-1 shows the device dimensions for the FinFET devices.

<table>
<thead>
<tr>
<th>Regions</th>
<th>Dimensions (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$H_{FIN}$</td>
<td>32</td>
</tr>
<tr>
<td>$T_{FIN}$</td>
<td>6.5</td>
</tr>
<tr>
<td>Gate height from oxide</td>
<td>56</td>
</tr>
<tr>
<td>Gate width</td>
<td>21</td>
</tr>
<tr>
<td>Spacer width</td>
<td>9</td>
</tr>
<tr>
<td>Spacer’s height</td>
<td>56</td>
</tr>
<tr>
<td>Source/Drain width</td>
<td>15</td>
</tr>
<tr>
<td>Width of oxide (HfO2)</td>
<td>1</td>
</tr>
<tr>
<td>around fin</td>
<td></td>
</tr>
<tr>
<td>Width of oxide (SiO2)</td>
<td>0.6</td>
</tr>
<tr>
<td>around fin</td>
<td></td>
</tr>
</tbody>
</table>

*Table 2-1 Device Dimensions.*

The Sentaurus structure editor (command is sde) tool allows to add the impurities in the structure by different regions as well as by defining different windows. Table 2-2
and Table 2-3 shows the doping concentrations used for NMOS and PMOS respectively. A flat doping roll-off = 1 nm/dec is set during the addition of impurities. The sde tool can be run in batch mode with the input command file *.scm. With the use of PERL code, multiple *.scm files were generated for different structures (Gate Length from 13 nm to 23 nm) for the experiments.

<table>
<thead>
<tr>
<th>Region</th>
<th>Doping Material</th>
<th>Doping Concentration (cm^{-3})</th>
<th>Roll-off</th>
</tr>
</thead>
<tbody>
<tr>
<td>S/D</td>
<td>ArsenicActiveConce.</td>
<td>2e+20</td>
<td>1 nm/dec</td>
</tr>
<tr>
<td>Substrate</td>
<td>BoronActiveConce.</td>
<td>1e+17</td>
<td>-</td>
</tr>
<tr>
<td>Subfin</td>
<td>BoronActiveConce.</td>
<td>5e+18</td>
<td>-</td>
</tr>
<tr>
<td>Fin</td>
<td>BoronActiveConce.</td>
<td>1e+15</td>
<td>-</td>
</tr>
</tbody>
</table>

*Table 2-2 Doping Profile for NMOS.*

<table>
<thead>
<tr>
<th>Region</th>
<th>Doping Material</th>
<th>Doping Concentration (cm^{-3})</th>
<th>Roll-off</th>
</tr>
</thead>
<tbody>
<tr>
<td>S/D</td>
<td>BoronActiveConce.</td>
<td>2e+20</td>
<td>1 nm/dec</td>
</tr>
<tr>
<td>Substrate</td>
<td>ArsenicActiveConce.</td>
<td>1e+17</td>
<td>-</td>
</tr>
<tr>
<td>Subfin</td>
<td>ArsenicActiveConce.</td>
<td>5e+18</td>
<td>-</td>
</tr>
<tr>
<td>Fin</td>
<td>ArsenicActiveConce.</td>
<td>1e+15</td>
<td>-</td>
</tr>
</tbody>
</table>

*Table 2-3 Doping Profile for PMOS.*

2.2. Mesh

For creating the mesh structure sde internally calls the Sentaurus snmesh tool. Regions are broken down into smaller (finite) elements which define nodes on which equations are solved numerically. Proper meshing is the key for the right simulations. For the design under test (DUT), mesh grid has been defined using Ref/Eval window after a couple of iterations.
A tighter grid can consume a lot of time for device simulation or sometimes simulation failure and a loose grid can lead to wrong results, which has been observed during the experiments. Fig. 2.2 shows the meshing used for the curved fin structure. For the critical regions like conducting channel and junctions, tighter mesh is defined. While for the other regions like substrate, there is no need for tighter mesh and thus we could save some time by defining not so tighter mesh (losing it 5x-10x) for such regions.

2.3. Sentaurus Device Simulator (sdevice)

Sentaurus sdevice is the device simulator which is used for the simulations. It is also a command line tool like Hspice, where we can include netlist and define testbench
in a text file named “sdevice_des.cmd”. There are various sections of the sdevice_des.cmd file explained below [Sentaurus09].

2.3.1. File Section

A device is defined by its shape, material composition, and doping. The structure that is created by Sentaurus Structure Editor has been used for device simulation and is defined by the TDR file, which we can specify with the keyword Grid in the File section of sdevice command file. File section specifies the input and output files required for the simulation. The output files include the *.plt file for the “Inspect” to view the current plots and *.tdr file for “svisual” to see the doping profiles, electron, hole mobility and all the specified electrical parameters.

    File {
        Grid = "mosfet.tdr"
        ...
    }

2.3.2. Electrode

Electrode section defines the electrodes Source, Drain, Gate, Substrate which needs to be used for the device simulation with their respective bias conditions. It also allows specifying the resistance for a specific electrode. Any contacts that are not defined as electrodes are ignored by Sentaurus Device.

2.3.3. Physic Section

We can specify Physics models that we want to use for the calculations in the Physics section. Sdevice allows us to specify different models for different materials, regions,
interface or electrode. Mobility models, HighFieldSaturation, stress models are included in this section. For the current project, few models that are added with the sample FinFET sdevice command file:

- Inversion and Accumulation Layer Mobility Model (IALMob)
- DeformationPotential model with ekp and hkp option to add strain
- Mobility – DopingDependence, HighFieldSaturation

Rest of the models and parameters are kept constant as were given in the 7 nm FinFET examples of Sdevice.

2.3.4. Plot

The plot section includes all of the solution variables like eDensity, hDensity, eCurrent, hCurrent, Potential, SpaceCharge, ElectricField, eMobility, hMobility etc that are saved in the output plot files (*.tdr). Svisual uses the resulted *.tdr file to plot the doping profiles, contours and above mention parameters. A large number of variables are present in the sdevice database which we can include in the Plot section for analysis.

2.3.5. Math

All the device equations defined by the different models present in sdevice command file which are a set of partial differential equations are solved by Sentaurus Device self-consistently, on all the data points defined by the discrete mesh by multiple iterations to minimize the error and it tries to converge on a solution with an acceptably small error. For this project, a couple of such settings are defined in the Math section for the numeric solver [Sentaurus09].
2.3.6. Solve

All the sweep parameters and the sequence for the solver is defined in the solve section. Several default equations are used for the solver, which were present for the FinFET examples including ‘Poisson’ equation for the initial solution using the initial values of all the electrodes present in the ‘Electrode’ section. A minimum step size of \(1 \times 10^{-6}\) V is used for the solution as the tool automatically applies a reduction in the step size if it is not able to converge at any point during simulation.

2.4. Inspect & Svisual

Inspect is a curve display tool like cscope & waveviewer that we use for Hspice simulations. It plots the output data file *.plt from sdevice and helps in analyzing the output results. Inspect provides graphical user interface (GUI) for visualizing the data. It provides a scripting language, which can be used to extract various parameters from the output curves like DIBL, \(V_{th}\), subthreshold slope without running the tool in GUI. It also gives freedom to define macros or use an in-built macro for extracting these parameters and helps in automating the complete flow. The current curves were extracted from the inspect in CSV format to use them for curve matching during the generation of compact models for Hspice for ASAP5 5 nm.

Synopsys svisual is a part of Sentaurus workbench visualization tool suit and can be run standalone. It also supports both GUI and scripting language like inspect and helps in plotting the experimental data. It can be used to create plots that display fields, geometries, and different regions of the structure including results such as p-n junctions and depletion layers. Users can visualize the complete structure in 2D or 3D. Once the mesh is defined, it can be seen in svisual to observe the junctions and how fine the user
has defined the mesh. Svisual can be used to plot the “*_msh.tdr” file resulted from the ‘sde’ and “*_msh.tdr” file processed and generated by sdevice, which has all the parameters specified in the plot section of the sdevice command file. It helps in extracting the doping profiles and the doping cutline using the in-built probe commands.
CHAPTER 3. FINFET

3.1. Structure

For the TCAD device simulation, the FinFET structure has been created with channel length = 21 nm and HFIN = 32 nm matching all other dimensions to the ASAP7 PDK. The thickness of fin is 6.5 nm. Fig. 3.1 and Fig. 3.2 shows the 3-D structure of the FinFET used for the simulation. The fin shape is rectangular with round edges as shown to reduce the gate leakage. In addition, due to a reduction in the fin width, DIBL reduces. [Xiong04] has shown a 50% decrease in DIBL due to a reduction in fin width by making them curved instead of sharp rectangular edges. The effective gate length is 19 nm which is considered below 2e+19 cm$^{-3}$ with the gate overlap of 1 nm making lightly doped drain (LDD). This is done to avoid aggressive doping junctions. The subfin region is highly doped to avoid source to drain punch through currents.

Fig. 3.1 3D FinFET Structure Created in Sentaurus Sde.
A 15 nm of raised S/D extension has been used. Diamond shaped S/D matches the ASAP7 FinFET S/D structure for lesser resistance. The S/D contacts are made by tungsten metal as shown in Fig. 3.1. It has been shown that with decreasing the S/D extension, the parasitic resistance of S/D reduces leading to a better drive current and reduced delays [Mahe12]. Fig. 3.3 shows the increase in drive current with the decrease in S/D extension. Both source and drain regions are heavily doped by 2e+20 cm$^{-3}$ with a degradation of 1 nm/dec.

![Fig. 3.2 3D Fin Structure with High-K Dielectric and Metal Gate.](image)

![Fig. 3.3 Effect of S/D Ext. on Drain Current [Mahe12]](image)
For the test structure, the device $I_d-V_g$ curve has been matched with the ASAP7 compact model simulation results for RVT device using the work function tuning. $I_{on}$ to $I_{off}$ ratio of $\sim 4 \times 10^6$ has been observed proving a good device with a low leakage current of around 100 pA. Subthreshold slope of $\sim 69$ mV/dec and DIBL $\sim 30$ mV/V is shown by the device with $L_{gate}$ of 21 nm.

Fig. 3.4 shows the doping cutline across the fin for the test structure generated in ‘svisual’ for FinFET structure for $L_{gate} = 21$ nm. With a doping roll-off of 1 nm/dec, the effective channel length is 19 nm below $2\times 10^{19}$ cm$^{-3}$. A thin high-k dielectric (HfO$_2$) oxide layer is inserted between gate and spacers for better insulation between gate and S/D regions. The spacer length is kept as 8 nm to keep the parasitic capacitance low.

![Doping Cutline for GAA Nanowire ($L_{gate}=21$ nm)](image)

*Fig. 3.4 Doping Cutline for GAA Nanowire ($L_{gate}=21$ nm)*
3.2. Impact of Stress

A uniaxial stress of 2 GPa has been added using the deformation potential model with k.p models for electrons and holes. The change in the energy band gaps structure, caused by the small deformation of the lattice, is a linear function of the strain. TCAD device simulations have been done to compare the impact of strain on the MOSFET performance. Table 3-1 and Table 3-2 show the TCAD simulation results for NMOS and PMOS FinFET device (with and without stress). Which shows ~30% improvement in the $I_{\text{sat}}$ for both devices. The performance improvement of nearly ~2x reported earlier [Hashemi08] were for long channel devices. As mentioned before, [Cheng13] reported a performance improvement of 35% for a channel length of 120 nm which shows a degradation in the improvement with a decrease in channel length and in accordance with the TCAD simulation performed in this project.

![Fig. 3.5 Impact of Uniaxial Strain on Drain Current for NMOS.](image)

At 21 nm L$_{\text{gate}}$, saturation current is increased from 31.75 uA to 41.11 uA. A threshold voltage shift of ~30 mV & ~45 mV (for NMOS and PMOS respectively) for both FinFET structure at a long range of L$_{\text{eff}}$ is observed. The impact of stress can be seen clearly on the off current ($I_{\text{off}}$) with a change of almost ~3x (rise) for NMOS and ~5x rise.
for PMOS shown in Fig. 3.5 & Fig. 3.6 for NMOS and PMOS. The impact of stress on linear drain current (\(I_{\text{dlin}}\)) is around 10\%, which is very low as compared to drain current in the saturation region.

![Graph showing impact of uniaxial strain on drain current for PMOS.](image)

**Fig. 3.6 Impact of Uniaxial Strain on Drain Current for PMOS.**

### 3.3. Results

It has been observed that decreasing the work function for NMOS increases the current drive \(I_d\), whereas PMOS results completely show a reverse effect, as \(I_d\) only increases when the WF value increase. Similar observation is found in the results by [Rezali16] doing an analysis of work function Vs current drive.

Table 3-1 shows the TCAD simulation results for NMOS in both linear and saturation region. For 23 \(\text{nm} L_{\text{gate}}\), the leakage current, as well as saturation current, is lowest as expected. The table shows the increasing trend line for the drain current with decreasing channel length. An 11\% increment can be seen from 23 \(\text{nm}\) to 13 \(\text{nm}\) for \(I_{\text{dsat}}\). The impact of the decrease in \(L_{\text{gate}}\) is more pronounced on \(I_{\text{off}}\) than to \(I_{\text{on}}\). At 13 \(\text{nm} L_{\text{gate}}\), \(I_{\text{off}}\) increases to 3.96 nA and shows ~70x increment from \(L_{\text{gate}}=23\) \(\text{nm}\) (with stress). The simulation results show a decrease in the \(I_{\text{lin}}\) with decreasing channel length for NMOS opposite to the \(I_{\text{sat}}\).
Table 3-1 Results For NMOS

For PMOS, simulation results are shown in Table 3-2. From 23 nm to 13 nm $L_{\text{gate}}$, $I_{\text{sat}}$ shows an increment of 30% which is almost three times than NMOS. In the case of $I_{\text{off}}$, PMOS shows a 156x increment for $L_{\text{gate}} = 13$ nm as compared to $L_{\text{gate}} = 23$ nm which is two times more than NMOS showing an exponential increase in leakage. Although PMOS shows a reverse trend from NMOS for $I_{\text{lin}}$ and increases from 7.12 $\mu$A to 8.18 $\mu$A.

Table 3-2 Results for PMOS

Fig. 3.7 & Fig. 3.8 shows the subthreshold slope for NMOS and PMOS respectively. $SS$ for both linear ($V_{ds} = 0.05$ V) and saturation ($V_{ds} = 0.7$ V) are plotted in the graphs. $SS$ is lower when the drain to source voltage ($V_{ds}$) is lower. Decreasing the channel length decreases threshold voltage, which leads to an exponential increase in the subthreshold leakage. [Horig16] observed the same behavior for the subthreshold slope.
for a fin width of 7-8 nm and $L_{\text{gate}}$ from 12 to 24 nm and the results are nearly the same as generated by these experiments.

![Graph showing subthreshold slope in saturation and linear region for NMOS](image)

*Fig. 3.7 Subthreshold Slope in Saturation and Linear Region for NMOS.*

$I_d-V_{gs}$ curve is generated for both NMOS and PMOS shown in Fig. 3.9. Which shows an $I_{\text{off}}$ around 34 pA & 26 pA in linear region and nearly 74 pA & 58 pA in saturation region for NMOS and PMOS respectively. The $I_{\text{off}}$ current is matched with the compact model results later for the comparisons including circuit delays.
**Fig. 3.8** Subthreshold Slope in Saturation and Linear Region for PMOS.

**Fig. 3.9** $I_d-V_g$ curve for NMOS and PMOS.
CHAPTER 4. NANOWIRE

4.1. Structure

GAA devices have excellent electrostatic properties as compared to FinFET. For this project, a GAA structure with two nanowires per device and one nanowire per device has been simulated using TCAD. L_{gate} and all other dimensions have been kept same as the FinFET design for apple to apple comparison. With fin height = 32 nm, two nanowires with diameter = 8 nm is placed under the gate. Nanowire diameter from D = 8 nm to 7 nm has been simulated to get the desired current drive by keeping the I_{off} as low as required. Nanowire with diameter = 8 nm provides the desired current drive maintaining the SS and DIBL. A thin oxide with equivalent oxide thickness E_{tox} = 1.1 nm is present in between the gate and nanowires. Fig. 4.1 shows the vertically stacked two nanowires placed horizontally. Spacers are created with a width = 8 nm for lesser parasitic capacitance between gate and S/D regions with 1 nm high-K HfO_{2} layer which is similar to FinFET structure. A uniaxial stressXX of 2 GPa is used in the device simulation.

![Fig. 4.1 Vertically Stacked Horizontal Nanowires.](image)
Nanowires are isolated from the metal gate with two thin oxide layers of SiO$_2$ and high-K dielectric (HfO$_2$) making an equivalent thin gate oxide of 1.1 nm around the nanowires. For the above structure, aluminum is used as the metal gate with tuned work function for the desired threshold voltage and drive current. The metal gate is isolated from source and drain on both sides by spacers and a thin oxide of HfO$_2$.

Fig. 4.2 a & b Nanowire Structure and Doping Profile

The complete structure of GAA nanowire FET is shown in Fig. 4.2a. It is kept same as FinFET device with the change in the channel region (two nanowires replaced single fin). Fig. 4.2b shows the doping concentrations of Silicon structures. The channel region shows a doping concentration of 1e+15 cm$^{-3}$, which is equal to zero if we calculate the number of impurity atoms present in the given volume of nanowires.
A doping cutline shown in Fig. 4.3 is generated using Sentaurus ‘Svisual’ for the GAA nanowire device for $L_{\text{gate}}=15$ nm, which represents the doping profile across the nanowire (channel region). The x-axis represents the distance between the source and drain through the nanowire. The constant doping roll-off is kept 1 nm/dec for these devices as well like FinFET structures. The effective channel length is selected below $2e+19$ cm$^{-3}$.

### 4.2. One Vs Two Wires

Looking at the required current drive of FinFET, one wire per device cannot provide sufficient drain current. Two different structure templates – ‘one wire per device’ & ‘two wire per device’ has been created and simulated using TCAD device simulator. Both the structures are simulated for the gate length sweep of 13 nm to 23 nm. As expected two wires shows the drain current twice the single nanowire. Below Table 4-1
shows that the saturated drain current increases with decreasing channel length but \( I_{d\text{lin}} \) decreases with decreasing channel length from 23 nm to 13 nm for NMOS. The subthreshold slope and DIBL is not presented in the table below as both the device structures shows the similar results, the difference is only the current drive. Results for SS and DIBL for nanowire and FinFET are compared in the later sections.

<table>
<thead>
<tr>
<th>( \text{Nwires = 1} )</th>
<th>( \text{Nwires = 2} )</th>
</tr>
</thead>
<tbody>
<tr>
<td>( L_{\text{gate}} ) (nm)</td>
<td>( L_{\text{eff.}} ) (nm)</td>
</tr>
<tr>
<td>13</td>
<td>11</td>
</tr>
<tr>
<td>14</td>
<td>12</td>
</tr>
<tr>
<td>15</td>
<td>13</td>
</tr>
<tr>
<td>17</td>
<td>15</td>
</tr>
<tr>
<td>19</td>
<td>17</td>
</tr>
<tr>
<td>21</td>
<td>19</td>
</tr>
<tr>
<td>23</td>
<td>21</td>
</tr>
</tbody>
</table>

Table 4-1 Drive Current Comparison Between One & Two Nanowires for NMOS.

4.3. Final Structure for ASAP5 5 nm GAA

Vertically stacked GAA nanowire structure is proposed for ASAP5 5 nm technology node. A scaling factor of 0.7 is used for the critical dimension. All the device regions are scaled down. Table 4-2 shows the sizes in nanometers for different regions of the FET device. The reduced S/D extension decreases the parasitic resistance and results in increased drive current. The diameter of the nanowire is 8.00 nm, which provides the effective width of ~25.00 nm per wire. A vertically placed stack of 2 horizontal nanowires is considered to provide a total effective width of 50.00 nm, which is exactly 0.7X of the 7 nm FinFET device. The gate length is kept as 15 nm resulting in \( L_{\text{eff}} = 13.00 \) nm. The critical poly pitch (CPP) is also scaled down to 38.00 nm from the 54.00 nm gate pitch. The fin height parameter used here is to demonstrate the height in which 2
equidistant nanowires could be placed. The doping concentrations are kept same in the S/D regions as $2e+20 \text{ cm}^{-3}$ with arsenic and boron as the doping impurities in NMOS and PMOS respectively. The Silicon nanowires are fully depleted and isolated from the gate with thin oxide (high-K dielectric HfO$_2$) of 1.00 nm. Tungsten is used as metal contacts for the diamond shaped S/D regions to keep the resistance low. For the desired current drive, the work function is tuned accordingly.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Diameter of Nanowire (D)</td>
<td>8.00 nm</td>
</tr>
<tr>
<td>S/D extension</td>
<td>10.00 nm</td>
</tr>
<tr>
<td>$L_{gate}$</td>
<td>15.00 nm</td>
</tr>
<tr>
<td>$L_{eff}$</td>
<td>13.00 nm</td>
</tr>
<tr>
<td>$W_{eff}$</td>
<td>50.00 nm</td>
</tr>
<tr>
<td>Spacer width</td>
<td>6.50 nm</td>
</tr>
<tr>
<td>Critical poly pitch (CPP)</td>
<td>38.00 nm</td>
</tr>
<tr>
<td>Number of nanowires per device</td>
<td>2</td>
</tr>
<tr>
<td>Fin Height</td>
<td>32.00 nm</td>
</tr>
</tbody>
</table>

*Table 4-2 Dimensions for ASAP5 GAA Nanowire Device*

**Drain Current**

*Fig. 4.4 $I_d$-$V_d$ Curve for NMOS for $V_g$ Steps of 100 mV.*
Device simulations are done for both $I_d$-$V_d$ curves and $I_d$-$V_g$ curves for the final structure. Fig. 4.4 & Fig. 4.5 shows the $I_d$-$V_d$ plot for the NMOS and PMOS device respectively with the step size of 100 mV for gate voltage ($V_g$). The maximum drain current achieved for NMOS is 35.7 uA. Whereas, PMOS is stronger than NMOS with a total drain current of 36.6 uA. Due to the short channel effect, both the devices show a positive slope for $I_d$ in the saturation region at all the gate voltages. Fig. 4.6 shows the conventional $I_d$-$V_g$ curves for both the GAA nanowire devices in saturation and linear region.

![Fig. 4.5 $I_d$-$V_d$ Curve for PMOS for $V_g$ Steps of 100 mV.](image-url)
All the parameters that were extracted for FinFET, are extracted for GAA nanowire at $L_{\text{gate}}=15$ nm. The resultant subthreshold slope is calculated as 71 mV/dec and 68.3 mV/dec for NMOS & PMOS respectively. A 25 mV/V & 35.4 mV/V DIBL values are observed for the final structure. Table 4-3 shows the drain current and the electrostatic parameters for GAA nanowire structure extracted using the ‘inspect’ macros.

<table>
<thead>
<tr>
<th>Device</th>
<th>$I_{\text{lin}}$ (uA)</th>
<th>$V_{\text{th, lin}}$ (mV)</th>
<th>$I_{\text{sat}}$ (uA)</th>
<th>$I_{\text{off}}$ (pA)</th>
<th>$V_{\text{th, sat}}$ (mV)</th>
<th>SS (mV/dec)</th>
<th>DIBL (mV/V)</th>
</tr>
</thead>
<tbody>
<tr>
<td>NMOS</td>
<td>9.33</td>
<td>285</td>
<td>35.7</td>
<td>19.4</td>
<td>269</td>
<td>70.8</td>
<td>24.6</td>
</tr>
<tr>
<td>PMOS</td>
<td>10.9</td>
<td>247</td>
<td>36.7</td>
<td>22.4</td>
<td>224</td>
<td>68.3</td>
<td>35.4</td>
</tr>
</tbody>
</table>

*Table 4-3 Drain Current for GAA Nanowire at $L_{\text{gate}}=15$ nm.*
CHAPTER 5. PERFORMANCE COMPARISON BETWEEN NWFET AND FINFET

MOS devices are compared based on various parameters for performance and reliability. At advanced technology nodes, power and delays can be considered as the dominant factors. For optimum performance of the devices, it is best to have minimum leakage and thus minimum subthreshold slope. The ideal SS, which can be obtained by a silicon device is 60 mV/dec. All the FinFET and similar devices have reached to ~65 mV/dec and still have some space for improvement. Due to DIBL, the threshold voltage of the device changes with a change in the power supply and thus metal gate loses full control on the channel. However, in analog circuits, to achieve the maximum gain, the slope of $I_d-V_d$ curve should be zero resulting in infinite output resistance of the transistor. Because of DIBL, all the transistors have a positive slope restricting the gain of analog amplifier circuits. Moving towards 5 nm technology node, these parameters are getting worse resulting in the bad device performance. GAA nanowires are not immune to these short channel effects. But the question is whether semiconductor industry can move forward with GAA nanowires on the predicted scaling trend and can keep the Moore’s law alive.

5.1. DIBL

A fair comparison is made between GAA nanowire and FinFET for DIBL. Fig. 5.1 shows the DIBL values for various gate lengths for both FinFET and nanowires. For $L_{gate}$ = 21 nm, nanowire FET has DIBL ~10 mV/V, which is almost 0.4 times the FinFET having DIBL = 27.69 mV/V.
From the plot, we can deduce that nanowire with Gate length 15 nm shows the same amount of DIBL that FinFET with a gate length of 21 nm (Reference structure) presents. Which leads to a ~28% $L_{\text{gate}}$ scaling, keeping the same device performance and maintaining the current drive.

![DIBL plot for NMOS FinFET & Nanowire.](image)

For 5 nm technology, if we plan to have $L_{\text{gate}}$ as 15 nm, DIBL for FinFET device becomes worse with a value 77 mV/V, which is more than twice the DIBL value at 21 nm $L_{\text{gate}}$. On the other hand, nanowire shows the same DIBL at $L_{\text{gate}} = 15$ nm, which FinFET has at $L_{\text{gate}} = 21$ nm.

The DIBL plot for PMOS is shown in Fig. 5.2. PMOS show more impact of drain voltage on channel barrier than NMOS showing DIBL = 32.31 mV/V for $L_{\text{gate}} = 21$ nm which is approximately same as ASAP7 RVT device. The DIBL becomes worse as the channel length decreases from 23 nm to 13 nm and increases by 5X. Like NMOS, PMOS nanowire device also shows the same amount of DIBL at $L_{\text{gate}} = 15$ nm, which FinFET
device has at \( L_{\text{gate}} = 21 \) nm giving some space to scale down from 7 nm technology node to 5 nm and keep the performance same.

![Graph showing DIBL for PMOS FinFET & Nanowire](image)

*Fig. 5.2 DIBL for PMOS FinFET & Nanowire.*

### 5.2. Subthreshold Slope

A fixed drain current (50 nA) is assumed for the calculation of the threshold voltage for all the test structures. Using the Inspect command file, the gate voltage is calculated for this point. The slope of the \( I_d-V_g \) curve at this point is found by the in-built derivative command of ‘Inspect’ tool. Further, the subthreshold slope is calculated by taking the inverse of the slope of this curve. The calculation procedure is kept same for both FinFET and nanowire structures.

**For NMOS**

The subthreshold slope for all the NMOS devices is shown in Fig. 5.3. It shows an increasing trend with decreasing channel length. For FinFET structure, the SS increases from 67.03 mV/dec to 89.7 mV/dec by sweeping the \( L_{\text{gate}} \) from 23 nm to 13 nm. Whereas for nanowire, the SS varies from 64.42 mV/dec to 76.13 mV/dec and do not show much
variation. For scaling down to 5 nm, and at $L_{\text{gate}} = 15$ nm, nanowire shows the SS = ~71 mV/dec. The SS of nanowire ($L_{\text{gate}} = 15$ nm) is not same as FinFET at $L_{\text{gate}} = 21$ nm.

![Graph showing SS for NMOS FinFET & Nanowire](image)

**Fig. 5.3 SS Calculated for NMOS FinFET & Nanowire.**

For PMOS

Fig. 5.4 shows the subthreshold slope for PMOS structures. PMOS devices show better SS than NMOS with a minimum SS of 62.23 mV/dec for nanowires and 65.63 mV/dec for FinFET at $L_{\text{gate}}=23$ nm. SS becomes worse for the FinFET structure at $L_{\text{gate}}=15$ nm with a value of 81 mV/dec. For 5 nm proposed nanowire structure, the calculated SS is 68.33 mV/dec, which is approximately same as FinFET (for $L_{\text{gate}} = 21$ nm).
CMOS circuit delays are one of the most important parameters to measure the performance. By scaling to the advanced node, circuit delays are expected to be less as compared to older technology nodes. To compare the delays of FinFET (7 nm) and GAA nanowire (5 nm), both the devices are calibrated with the same $I_{\text{off}}$ (19 pA) by changing the work function. Fig. 5.5 is used to do the delay analysis.

*Fig. 5.5 Back to Back Inverter.*
After a scaling factor of 0.7x, the final structure has an effective width of 50 nm. Whereas, the FinFET (7 nm) has an effective width of 71 nm. As the gate capacitance is directly proportional to the effective width.

Change in Capacitance,

\[ \Delta C = \frac{\text{Weff of Nanowire}}{\text{Weff of FinFET}} = \frac{50}{71} = 0.7 \]

Change in Drain Current,

\[ \Delta I = \frac{I_{\text{dsat of Nanowire}}}{I_{\text{dsat of FinFET}}} = \frac{36.5}{41.7} = 0.875 \]

Delay (\(\tau\)) can be calculated by the following equation,

\[ \tau = \frac{CV}{I} \]

Keeping Voltage constant, change in delay,

\[ \Delta \tau = \frac{\Delta C}{\Delta I} = 0.7/0.875 = 0.8 \]

Keeping the voltages constant for both the structures, GAA nanowires are expected to be 20% faster (optimistic), which is a significant improvement.
CHAPTER 6. SUMMARY

Multi-Gate FinFET structures and GAA nanowire 3D structures are created and simulated using the device simulation in Sentaurus tool suit. The nanowire structures are created with the same sizes as FinFET with only change of nanowires instead of fin as conducting channel and gate surrounds the channel completely instead of three sides. The experiment is conducted on seven structures with different channel length ($L_{\text{gate}}$) from 13 nm to 23 nm and changing the widths of spacers to keep the critical poly pitch (CPP) constant. While generating the 3D mesh structure, the total number of data points are kept under 40000 as with the available resources, the total time was taken more than 50 minutes for one iteration (mesh creation and device simulation). Also, meshing depended on the convergence (a very fine mesh caused the convergence failure) during device simulation. A uniaxial stressXX (compressive strain for PMOS and tensile strain for NMOS) of 2.0 GPa is added in all the structures to strain the silicon for better performance and to match the devices with the compact model results of ASAP7 PDK using the piezo section in sdevice command file. Once the 7 nm ($L_{\text{gate}} = 21 \text{ nm}$) FinFET structure was characterized using the work function tuning and correct physics models, then rest all of the structures of FinFET and GAA nanowire were simulated using the same sdevice command file and meshing.

FinFET structures show an increase of around 25 mV/dec in the subthreshold leakage by decreasing the channel length from 23 nm to 13 nm. Also, the DIBL shoots above 100 mV/V for 13 nm structure, touching approx. ~114 mV/V for NMOS and nearly 121 mV/V for PMOS, which is almost 5X the amount observed for the structure with $L_{\text{gate}} = 23 \text{ nm}$. When the same device simulations are done for the GAA nanowire
structures, they showed an increase of around 11 mV/dec in the subthreshold leakage by decreasing the channel length from 23 nm to 13 nm that is even lesser than half the value observed for FinFET. Whereas, GAA nanowires also showed an increase in DIBL by nearly 5X, which is almost same as FinFET structures. But due to the presence of metal gate on all sides of the conducting channel, the DIBL is noted below 50 mV/V for both NMOS and PMOS.

The optimized structures proposed for ASAP5 5 nm PDK has channel length (L\text{\_gate}) of 15 nm and thus effective channel length of 13 nm. If we use FinFET structure, all the MOS devices has to suffer with a subthreshold leakage of nearly 78-80 mV/dec and DIBL of around ~80 mV/V for both devices (NMOS and PMOS) leading them to the poor performance. However, GAA nanowires show a SS of nearly 71 mV/dec for NMOS and 68.3 mV/dec for PMOS. With a significant increment in DIBL, nanowires still show 25 mV/V & 35.4mV/V, which is lesser than half of the DIBL values (shown for L\text{\_gate} = 15 nm FinFET) for NMOS and PMOS respectively. Nanowires, thus maintain these parameters while scaling down from L\text{\_gate} = 21 nm to L\text{\_gate} = 15 nm. A fair comparison of FOR4 Inverter delay is made between the two devices. Nanowires show a 20% reduction in the circuit delays. For better electrostatics, GAA nanowire seems to be a better candidate, which can be scaled down to L\text{\_gate}=15 nm and can still meet the SS and DIBL limits.
REFERENCES


