Amorphous Silicon Contacts for Silicon and Cadmium Telluride Solar Cells

by

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ABSTRACT

Achieving high efficiency in solar cells requires optimal photovoltaics materials for light absorption and as with any electrical device—high-quality contacts. Essentially, the contacts separate the charge carriers—holes at one terminal and electrons at the other—extracting them to an external circuit. For this purpose, the development of passivating and carrier-selective contacts that enable low interface defect density and efficient carrier transport is critical for making high-efficiency solar cells. The recent record-efficiency n-type silicon cells with hydrogenated amorphous silicon (a-Si:H) contacts have demonstrated the usefulness of passivating and carrier-selective contacts. However, the use of a-Si:H contacts should not be limited in just n-type silicon cells.

In the present work, a-Si:H contacts for crystalline silicon and cadmium telluride (CdTe) solar cells are developed. First, hydrogen-plasma-processed a-Si:H contacts are used in n-type Czochralski silicon cell fabrication. Hydrogen plasma treatment is used to increase the Si-H bond density of a-Si:H films and decrease the dangling bond density at the interface, which leads to better interface passivation and device performance, and wider temperature-processing window of n-type silicon cells under full spectrum (300–1200 nm) illumination. In addition, thickness-varied a-Si:H contacts are studied for n-type silicon cells under the infrared spectrum (700–1200 nm) illumination, which are prepared for silicon-based tandem applications.

Second, the a-Si:H contacts are applied to commercial-grade p-type silicon cells, which have much lower bulk carrier lifetimes than the n-type silicon cells. The approach is using gettering and bulk hydrogenation to improve the p-type silicon bulk quality, and then applying a-Si:H contacts to enable excellent surface passivation and carrier transport.
This leads to an open-circuit voltage of 707 mV in $p$-type Czochralski silicon cells, and of 702 mV, the world-record open-circuit voltage in $p$-type multi-crystalline silicon cells.

Finally, CdTe cells with $p$-type a-Si:H hole-selective contacts are studied. As a proof of concept, $p$-type a-Si:H contacts enable achieving the highest reported open-circuit voltages (1.1 V) in mono-crystalline CdTe devices. A comparative study of applying $p$-type a-Si:H contacts in poly-crystalline CdTe solar cells is performed, resulting in absolute voltage gain of 53 mV over using the standard tellurium contacts.
To my parents who give me a beautiful life.

To my friends who encourage and help me.
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Photovoltaics (PV), which converts sunlight directly into electricity, is one mainstream division of renewable energy technologies. Besides its well-known advantages (e.g. wide geographical sunlight distribution, long-term national energy security after using up fossil-based resources, environmental pollution reduction, and no greenhouse gas emission), PV could have huge economic benefits over the utility, commercial and residential markets [1], [2]. These benefits can be traced back the fast growing PV market—40% compound annual growth rate between 2010 and 2016 [3], and such growth is expected to continue to 2025 [4] or 2030 [5].

Developing high-efficiency solar cells [6] is always one of the most important research thrust in PV community for reshaping the world energy future. For the mainstream terrestrial non-concentrating applications, improving the efficiency is the key to decrease balance-of-system costs [7] and provide large-scale electricity generation [8], [9].

1.1 Solar Cell Efficiency and Device Parameters

The efficiency ($\eta$) of a solar cell is determined by:

$$\eta = \frac{I_{mp} V_{mp}}{P_{in}} = \frac{I_{sc} V_{oc} FF}{P_{in}}$$

For standard terrestrial solar cells, the measurement is typically under AM1.5G condition at 25°C and the input light density ($P_{in}$) is fixed at 100 mW/cm². Thus, the solar cell
efficiency is only dependent on short-circuit current density ($J_{SC}$), open-circuit voltage ($V_{OC}$), and fill factor (FF).

Table 1-1 Functions of PV absorber and contacts in a solar cell.

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<tbody>
<tr>
<td>$J_{SC}$</td>
<td>absorption of light to generate electron-hole pairs</td>
<td>PV absorber</td>
</tr>
<tr>
<td>$V_{OC}$</td>
<td>separation of charge carriers of opposite types</td>
<td>PV absorber and contacts</td>
</tr>
<tr>
<td>FF</td>
<td>extraction of the carriers to an external circuit</td>
<td>PV contacts</td>
</tr>
</tbody>
</table>

Table 1-1 links the device parameters to the energy conversion process, in which PV absorber and/or PV contacts play important roles. Firstly, increasing the light absorption within the PV absorber has a direct impact on getting high $J_{SC}$ value; secondly, limiting the recombination losses from PV absorber and contacts is essential to get high $V_{OC}$ value; and finally, reducing carrier-transport ohmic losses, mainly from PV contacts, is essential to get high FF value.

Achieving high efficiency in solar cells requires optimal PV absorber materials and high-quality contacts. Specifically, high-quality PV contacts have direct impact on achieving high $V_{OC}$ and FF values for any type of PV absorbers.

1.2 Passivating and Carrier-Selective Contacts for Solar Cells

One definition of a PV contact is the terminal of a solar cell that includes a metallic electrode [10]. This definition is sensible for diffused-junction solar cells in which metal makes direct contact to a heavily doped region of the PV absorber, but does not capture the full complexity of emerging, heterojunction-based contact schemes. An alternative definition recognizes that the metallic electrode must be in contact with a semiconducting
or semi-insulating region where the conductivity for one carrier type is much greater than for the other carrier type [10], and the carrier-selective region is referred to as a carrier-selective contact [11]. We use this definition of “contact” throughout this thesis, and include within the definition any passivating layers that may be between the absorber and the carrier-selective region.

![Diagram of solar cell with absorber, passivating and carrier-selective contacts](image)

Figure 1-1. Schematic solar cell with absorber, passivating and carrier-selective contact layers and electrodes.

Figure 1-1 shows a schematic solar cell with absorber, passivating and carrier-selective contacts [10], [12] and electrodes. The passivating contact means low interface defect density between the PV absorber and the PV carrier-selective contact. This is usually referred to as the chemical attachment of atomic or molecular species to the undesirable dangle bonds or defects at the PV absorber surface [11]. As to carrier selectivity, an ideal hole-selective contact has very high hole conductivity but very small electron conductivity to facilitate the carrier transport and reduce the recombination loss [10], [13]; On the contrary, the hole conductivity must remain very small compared to the electron conductivity in an ideal electron-selective contact [10], [13]. Only through different
conductivities of electrons and holes on the way toward their contacts, effective selective transport can be realized, as described in [10].

One way to achieve good carrier selectivity is via mobility asymmetry (at the hole contact, for example, having very high hole mobility and very low electron mobility); however, such mobility asymmetry is not practical in the real word [10]. Typically, the good carrier selectivity is achieved from carrier density asymmetry [10], either from band bending via doping and/or work function selection [14], or from asymmetrical tunneling probability in the hole and electron contacts [14]. The examples of these two approaches are discussed in Section 1.3.

In short, the function of passivating and carrier-selective contacts is suppressing charge carrier recombination and extracting either electrons or holes (facilitate one type but inhibit the other) from the PV absorber, which contributing to high $V_{OC}$ and FF values of a solar cell.

1.3 Contact Designs for High-Efficiency c-Si Solar Cells

The most dominant PV technology in the market is crystalline silicon (c-Si) wafer-based solar cells [15], accounting for about 94% of the total production in 2016 [3]. The predominant c-Si usage lies in its element abundance in the Earth, its near-optimum bandgap (1.12 eV) for sunlight absorption, its doping flexibility ($n$-type and $p$-type), and its well-developed production technology from microelectronic and other semiconductor industries. Here c-Si wafer-based solar cells are used as examples to illustrate the importance of PV contacts.

Figure 1-2 shows the existing c-Si solar cell architectures and the predicted market shares in the next ten years. Clearly, while the market portion of conventional back surface
field (BSF) c-Si cells decrease, all the other counterparts—Passivated Emitter Rear Cell (PERC) and its family [16], [17], silicon heterojunction (SHJ) [18], interdigitated back contact (IBC) [19] and Si-based tandem cells [20], [21]—are expected to increase in market share over time. The change of the market share, essentially, is due to the achievable high efficiency of each solar cell architecture and the low cost prediction in high volume manufacturing.

![Bar chart showing market share of different c-Si solar cell architectures over the next ten years. The BSF means p-type cells with p⁺ BSF regions, which are usually formed by firing screen-printed Al paste in a belt furnace. The PERC/PERL/PERT stands for Passivated Emitter Rear Cell/Passivated Emitter with Rear Locally diffused/Passivated Emitter Rear Totally diffused architectures.]

**Figure 1-2.** Estimated market share of different c-Si solar cell architectures over the next ten years [22]. The BSF means p-type cells with p⁺ BSF regions, which are usually formed by firing screen-printed Al paste in a belt furnace. The PERC/PERL/PERT stands for Passivated Emitter Rear Cell/Passivated Emitter with Rear Locally diffused/Passivated Emitter Rear Totally diffused architectures.

In addition to these demonstrated c-Si solar cell architectures for PV manufacturing in the industry, the PV research community is working on promising next-generation, high-efficiency c-Si cell architectures (mostly led by research universities or institutes). Similarly, PV contact design is quite important to gain high efficiency.

The quality of contact in c-Si solar cells is typically characterized by the recombination current density prefactor \( J_0 \) and the contact resistivity \( \rho_{\text{contact}} \) [11], [14], [23].


Experimentally, the $J_0$ can be determined from the method proposed by Kane and Swanson [24]: plotting the Auger-corrected inverse effective minority carrier lifetime as a function of the excess carrier density. Some other following works have also been added to get the accurate $J_0$ value [25]–[27]. The $\rho_{\text{contact}}$ is typically determined via transfer length method [28]–[30], which involves making a series of contact pads (e.g. c-Si bulk/contacting layers/metal electrode) separated by various distances on the test structure. If several measurements are made between contact pads, a plot of resistance versus contact pad spacing can be obtained to extract the exact $\rho_{\text{contact}}$ value.

To understand the impact of $J_0$ and $\rho_{\text{contact}}$ on the cell efficiency, Figure 1-3 shows the maximum c-Si solar cell efficiency using Quokka simulation, varying the $J_0$ and $\rho_{\text{contact}}$ values in the full-area rear contact [14] (note: complex partial-area rear contact can be found in [11], [23]). For this ideal c-Si absorber, higher device efficiency is only achievable by using the desirable passivating and carrier-selective contact, which minimize both $J_0$ (related to $V_{\text{OC}}$ and recombination losses [11]) and $\rho_{\text{contact}}$ (related to FF and resistance losses). To get low $J_0$ and $\rho_{\text{contact}}$ values simultaneously, it is necessary to maximize the conductivity of majority carriers in the contact and minimize the conductivity of minority carriers in the contact at the same time [14].
Figure 1-3. Contour plot of the maximum c-Si solar cell efficiency as a function of rear-side $J_0$ and $\rho_{\text{contact}}$ from device simulation. For the 110-μm-thick c-Si absorber with idealized current generation (i.e. 43.31 mA/cm$^2$) and ideal front contact (i.e. $J_0 = 0$ fA/cm$^2$ and $\rho_{\text{contact}} = 0$ Ω·cm$^2$), the calculated efficiency is only limited by $J_0$ and $\rho_{\text{contact}}$ of the full-area rear contact together with the unavoidable radiative and Auger recombination in the c-Si. The reported record conversion efficiency value is shown next to the label for each solar cell architecture; note that the $J_0$ and $\rho_{\text{contact}}$ are weighted area-corrected for the partial-contact architectures: $J_0 = A_f \cdot J_{0,\text{metallized}} + (1 - A_f) \cdot J_{0,\text{passivated}}$ and $\rho_{\text{contact}} = \rho_{\text{contact,metallized}} / A_f$, where $A_f$ is the metallized area fraction of the solar cell [14].

Several conceptual approaches have been used to achieve the desired carrier selectivity [14]:

- the heavily doping in the c-Si,
- the surface carrier concentration and conductivity modulation by the application of an external potential source (i.e. work function, or fixed charge density),
- the formation of a heterojunction between the c-Si and a wide-bandgap material with the desired conductivity type via suitable band alignment,
• the formation of a tunnel barrier with an asymmetrical tunneling probability for electrons and holes.

In practice, the contact design may employ some of these above-mentioned mechanisms simultaneously, which resulted in many passivating and carrier-selective contact materials and structures [11], [14]. For the reported high efficiency c-Si solar cells in Figure 1-3, both classic SHJ and TOPCon cells have very low $J_0$ values, and the $\rho_{\text{contact}}$ difference at this range becomes quite insignificant to affect the efficiency. In addition, PERL cell has quite low $\rho_{\text{contact}}$ but high $J_0$ from the recombination loss at c-Si/metal interface. In the industrial solar cell category, n-PERT solar cell has a significantly higher efficiency than the p-PERC and the n-Pasha solar cells, indicating the benefit of having a very low $J_0$ value. Combing the theoretical upper efficiency limit and the current state-of-the-art efficiency values, it is clear that no significant efficiency improvement can be expected when the $\rho_{\text{contact}}$ is below ~0.1 $\Omega \cdot \text{cm}^2$ [14]. Therefore, to fabricate a high-efficiency solar cell, it is apparently more important to further reduce $J_0$ once a sufficiently low $\rho_{\text{contact}}$ value is reached [14].

While many other materials have exhibited interesting results (like Al$_2$O$_3$ as non-conductive passivating layer [31], [32], TiO$_x$ as electron contact [33]–[35], MoO$_x$ as hole contact [36]–[38]), most of the reported high efficiency c-Si solar cells still prefer to use silicon-based materials as the PV contacts. Figure 1-4 shows the c-Si solar cell efficiency with various contacts during the past few years. In terms of the cell efficiency, the hydrogenated amorphous silicon (a-Si:H) and oxide/poly-Si are the most promising contact designs in c-Si solar cells. Essentially, the a-Si:H contact forms suitable band bending on c-Si substrate via doping and/or work function selection while the SiO$_x$/poly-Si contact
uses asymmetrical hole/electron tunneling probability—both achieve quite low $J_0$ [27], [39]. Though a-Si:H contact may have a bit higher $\rho_{\text{contact}}$ (note: the most recent $\rho_{\text{contact}}$ is unknown [27]), the side-by-side comparison of record efficiency c-Si solar cells favors using a-Si:H contact to some extent, due to the higher $V_{\text{OC}}$, FF, larger cell area, and cost-effective c-Si wafers (see Table 1-2). These advantages motivate us to focus on a-Si:H contact development throughout the rest of the thesis.

![Figure 1-4](image)

**Figure 1-4.** Progress of c-Si solar cell efficiency with various contacts structures [14].

<table>
<thead>
<tr>
<th>Material</th>
<th>$V_{\text{OC}}$ (mV)</th>
<th>FF (%)</th>
<th>Area ($\text{cm}^2$)</th>
<th>Material</th>
</tr>
</thead>
<tbody>
<tr>
<td>a-Si:H SHJ [27]</td>
<td>738</td>
<td>84.9</td>
<td>180</td>
<td>Czochralski silicon</td>
</tr>
<tr>
<td>oxide/poly-Si [39]</td>
<td>725</td>
<td>83.3</td>
<td>4</td>
<td>Float-zone silicon</td>
</tr>
</tbody>
</table>

**1.5 Amorphous Silicon Contact for Solar Cells**

Amorphous silicon (a-Si) is the non-crystalline form of silicon that does not have long-range order in the atomic positions. While this leads to undesirable properties like dangling bonds and defects, such amorphous state actually introduces a structure of
freedom [40], especially when integrating hydrogen into the a-Si network. Thanks to the hydrogen passivation that reduces the dangling bond density by several orders of magnitude, the hydrogenated amorphous silicon (a-Si:H) can be used in solar cells. In addition, the a-Si:H has quite flexibility in bandgap tuning, doping, composition, and alloy with other elements, which are desirable to develop good passivating and carrier-selective contacts. Detailed information of a-Si:H materials is in Section 1.6.

One existing success is that the $n$-type, mono-crystalline SHJ cell—using $p$-type/intrinsic a-Si:H stack layers to extract holes and $n$-type/intrinsic a-Si:H stack layers to extract electrons—achieves the highest $V_{OC}$ and the world-record 26.7% efficiency among all the c-Si wafer-based solar cells [6], [27]. The high $V_{OC}$ value, 738 mV in the 26.7%-efficient cell, is attributed to the excellent hydrogen passivation of the thin intrinsic a-Si:H layers at the high-quality c-Si wafer surface and the good carrier selectivity by the large c-Si band bending from decent doping level of $p$-type/$n$-type a-Si:H layers. The high FF value, 84.9% in the 26.7%-efficient cell, is attributed to the excellent a-Si:H/c-Si interface passivation as well as resistance loss optimization.

Figure 1-5 shows a schematic equilibrium band diagram of a standard SHJ cell [13]. On both sides of the $n$-type c-Si absorber, the symmetric intrinsic a-Si:H layers have high hydrogen content—as will be discussed in Sections 2.2 and 2.3—that can passivate the dangling bonds of c-Si surface [40], enabling very low interface recombination velocity. The low defect density of the intrinsic a-Si:H layers also work as the buffer to isolate the defects in the doped a-Si:H and transparent conducting oxide (TCO) layers [13]. For the doped a-Si:H layers, the main function is to form large c-Si band bending at each side. As a result, the left-side Fermi-level is pushed towards the valence band due to $p$-type a-Si:H
doping, and the right-side Fermi-level is pushed towards the conduction band due to $n$-type a-Si:H doping. The second function of doped a-Si:H is to ensure effective charge carrier transport into the TCO layer, in which a sufficient high doping in a-Si:H and a small work function mismatch between the two materials are required [13]. With respect to the TCO layers, they should provide effective carrier extraction from the doped a-Si:H—ideally have high work functions at the hole contact and low work functions at the electron contact—and also serve as other functions (good lateral transport, good contact to metal, and anti-reflection coatings).

![Figure 1-5. Schematic equilibrium band diagram of a standard SHJ cell [13]. The c-Si(n) has 1.12 eV bandgap while the a-Si:H has ~1.7 eV bandgap.](image)

Essentially, this SHJ device structure uses a higher bandgap material (doped a-Si:H) on PV absorber to create a greater potential for vastly different electron and hole
conductivities, and inserts an intermediate defect-passivating layer (intrinsic a-Si:H) to improve the device performance.

Another demonstrated success using a-Si:H contact is in the cadmium telluride (CdTe) thin-film solar cells, in which p-type a-Si:H is used as a hole-selective layer in n-type, mono-crystalline CdTe cells with wide-bandgap cadmium magnesium telluride (CdMgTe) passivating layers. A world-record V_{OC} of 1.1 V is achieved in such CdMgTe/CdTe/CdMgTe double-heterojunction device structure [41]. Further device optimization lead to a total-area efficiency of 18.5% (V_{OC}=1.09 V and FF=75.7%) measured at Arizona State University (ASU) [42]. The main function of a-Si:H here is to provide large band bending of CdTe for hole selectivity. The detailed physics and band diagram is in Chapter 5.

Overall, if the a-Si:H contacts can create a great potential for vastly different electron and hole conductivities while maintain good interface passivating properties, such passivating and/or carrier-selective a-Si:H contacts are promising to improve the V_{OC} and FF of any types of solar cells.

1.6 Hydrogenated Amorphous Silicon Materials

Here we review the a-Si:H materials properties that are important for satisfying the principle of passivating and carrier-selective contacts.

1.6.1 Early history

Using radio-frequency glow discharge from silane (SiH_{4}) gas, the a-Si:H was first made by Chittick et al. in 1969 [43]. The technique is essentially similar to what people now use. Also, the authors found adding phosphine (PH_{3}) into the a-Si:H growth can lead
to reduced resistivity, demonstrating the $n$-type doping possibility [43]. The substitutional a-Si:H doping ($n$-type or $p$-type) was reported by Spear and LeComber in 1975 [44], which attracted great interest from the research community. The hydrogen content within a-Si:H from the glow discharge method was studied in 1977 [45], which is recognized as the essential component of a-Si:H film for reducing the defects and passivating other materials.

1.6.2 Growth of a-Si:H

The a-Si:H has quite flexibility to form many Si-H bonding configurations, exhibiting a variety of electronic properties. Since the a-Si:H network is mostly defined during its growth, the study of a-Si:H growth process needs to be reviewed.

The common a-Si:H growth is using radio-frequency (RF) plasma-induced dissociation of SiH$_4$ and other gases, typically at a plasma enhanced chemical vapor deposition (PECVD) chamber. The RF plasma sets the gas dissociation rate and thus the film deposition rate. The gas pressure during the deposition is typically at 0.1-10 Torr, to sustain the plasma and to define the mean free path of the gas radicals during the process. For SiH$_4$ and the other added gases (for dilution, doping, or alloying), the gas flow determines the quantity of each gas during the complex chemical reactions in the chamber. Affecting the chemical reactions in the chamber and on the substrate surface, the chamber and substrate temperatures are usually set the same, referred as deposition temperature. It can take from 30-400 °C, but the optimum deposition temperature is typically at 200-300 °C due to low defect density and decent hydrogen fraction in the film.

In addition to PECVD method, sputtering is another method of depositing a-Si:H film. By using silicon target with additional hydrogen, the sputtered a-Si:H film in theory could have the same properties. However, the sputtered a-Si:H film may suffer from ion
bombardment damage that degrades the film quality. Also, sputtering is a physical vapor deposition (PVD) process that may not give a smooth conformal a-Si:H film on the non-flat substrate [46].

1.6.3 Hydrogen in a-Si:H

Hydrogen is known to have passivating properties for dangling bonds and defects, implicating its application into the passivating contacts. Within the a-Si:H film, the hydrogen and silicon have different bonding properties. Such properties are sensitive to the a-Si:H growth and post-deposition treatment. Fourier-transform infrared spectroscopy (FTIR) can be used to characterize the Si-H bonding information [47]. Nuclear magnetic resonance (NMR) gives more information about the local environment where the hydrogen atoms reside [48], [49]. Mostly during the post-deposition treatment, the hydrogen diffusion and evolution can be studied via secondary ion mass spectrometry (SIMS) or nuclear reaction analysis (NRA) [50]. As an alternative, in situ ellipsometry is a power tool to observe a-Si:H film growth [51], and fit the thickness and bandgap (i.e. hydrogen content) of the a-Si:H during post-deposition treatment [52].

1.6.4 Doping of a-Si:H

The doping of a-Si:H, reported by Spear and LeComber in 1975 [44], is revolutionary for this disordered a-Si:H material. They found the conductivity of the a-Si:H increases upon adding PH$_3$ or B$_2$H$_6$ into the a-Si:H growth gas (see Figure 1-6), which led to extensive applications since then. The conductivity change is due to a shift of the Fermi level. Without the doping possibility of a-Si:H film, it is impossible to forming a-
Si:H carrier-selective contacts via band alignment and/or external potential source for c-Si and other types of solar cells [14].

![Graph](image)

Figure 1-6. The effect of phosphorus and boron doping on the position of the Fermi level and conductivity in a-Si:H film [44].

Adding the dopant can change the a-Si:H deposition rate [53]: the deposition rate increases with boron $p$-type doping and it decreases with phosphorus $n$-type doping. Importantly, such doped a-Si:H layers have quite many defects, compared to undoped a-Si:H layers as well as compensated a-Si:H layers [53]. It suggests the defect states are largely an intrinsic result of doping [53]. The high defect density in the doped a-Si:H layers is also confirmed in [54], and now it is widely acknowledged.

Another important parameter for doped a-Si:H is its doping efficiency, defined as the fraction of impurities that are active dopants. As was explicated studied in [55], the doping efficiency in a-Si:H is quite low (typically below 10%), and it greatly decreases to below 1% at high doping levels.

1.6.5 Metastability of a-Si:H
The a-Si:H is known to have metastability issue over the past few years, including the famous Staebler-Wronski effect reported in 1977 [56]. For example, illumination, charge, or particle bombardment, can induce defects into the a-Si:H film, but these defects can be subsequently removed by a low-temperature annealing process.

In terms of experiments, it is always a good idea to try annealing (e.g. 150-200 °C) after any external excitation on the a-Si:H film. This is the main reason that researchers typically perform annealing for devices with a-Si:H layers [57], [58].

1.6.5 Surface of a-Si:H

Like c-Si surface, a-Si:H surface oxidizes upon exposure to the air. However, Figure 1-7 shows the oxidation is quite slow for a good-quality PECVD-grown a-Si:H film. This information is quite useful for a-Si:H sample storage in the absence of vacuum or N₂ ambience.

![Figure 1-7. Room-temperature oxidation of a-Si:H and of c-Si [59].](image)

1.6.6 Metallic electrode to a-Si:H
On top of the a-Si:H layers, the metal-like degenerate semiconductor layer and metal electrode are needed to form ohmic contact and extract the holes (or electrons) out of the device. While they are not the focus of the thesis, careful selection of the metallic materials that have desirable work functions is very important. Detailed references can be found in [18], [60]–[62].

1.6.7 Challenges of a-Si:H

After the literature review, the a-Si:H materials are good to work as passivating and carrier-selective contacting layers. However, there are three challenges of a-Si:H materials: 1) low doping efficiency; 2) high parasitic absorption; 3) low temperature stability. For these challenges, μc-Si:H [63] and a-SiC:H [64] film recipes are developed to address the limitations at ASU. In addition, avoiding the parasitic absorption and alleviating temperature stability are discussed in the following sections of the thesis.

1.7 Thesis Outline

In this work, we would like to discover the possibility of using a-Si:H contacts in various PV absorbers—silicon and non-silicon materials—to achieve high $V_{OC}$ and good solar cell performance. Chapter 2 describes using hydrogen-plasma-treated a-Si:H contact in $n$-type SHJ cells processing. Chapter 3 describes thickness-varied a-Si:H contact for $n$-type SHJ solar cells under the infrared spectrum for future tandem application. Chapter 4 describes $p$-type SHJ cells with pre-fabrication wafer treatment before the a-Si:H contact formation. Chapter 5 describes CdTe cells with $p$-type a-Si:H contact, in which wide-bandgap CdMgTe or aluminum oxide ($Al_2O_3$) is used as an intermediate passivating layer.
CHAPTER 2

A-Si:H CONTACT AND HYDROGEN PLASMA TREATMENT IN SHJ SOLAR CELLS

The a-Si:H contact was first introduced into the n-type c-Si wafers by Sanyo in 1992, which resulted an 18.1% efficient silicon heterojunction (SHJ) solar cell [18]. With continuous research efforts, this SHJ technology led to n-type SHJ solar cells with record-high efficiencies, including 25.7% in 2014 [65] and 26.7% in 2017 [6], [27].

Hydrogen plasma treatment, a plasma-initiated process that dissociates the molecular hydrogen precursor gas into atomic hydrogen [66], can be used to increase the Si-H bond density of a-Si:H films [67] and decrease the dangling bond density of a-Si:H/c-Si interface [68]. After the hydrogen plasma treatment, 7-nm-thick or 15-nm-thick intrinsic a-Si:H layers with enhanced passivation [68], [69] were reported on n-type c-Si substrates recently, indicating a promising approach to improve the SHJ solar cell performance.

In this chapter, we investigate the possibility of integrating such hydrogen plasma treatment into various aspects of the standard n-type SHJ cell fabrication process.

2.1 Standard SHJ Cell Fabrication and Measurement

Except where otherwise stated, we used 1–5 Ωcm, 160-200 μm thick, n-type monocrystalline Czochralski (CZ) silicon wafers as substrates. Wafers were textured in an alkaline solution to form random pyramids, cleaned in piranha and RCA-B solutions, and then dipped in buffered oxide etch (BOE) prior to a-Si:H deposition. To avoid cross-contamination, intrinsic, boron-doped p-type and phosphorus-doped n-type a-Si:H films (i.e. a-Si:H(i), a-Si:H(p), a-Si:H(n)) [70] were deposited in three separate chambers in an
Applied Materials P-5000 plasma-enhanced chemical vapor deposition (PECVD) tool (see APPEXD A for the tool specification). Table 2-1 shows the gases used in the three a-Si:H recipes. Intrinsic and $p$-type a-Si:H films were first deposited on one side of the wafer at 250 °C, and intrinsic and $n$-type a-Si:H films were then deposited on the other side at 250 °C. After a-Si:H depositions, the indium tin oxide (ITO) layers were sputtered on both sides, a silver electrode was sputtered on the rear, a silver grid was screen printed on the front, and the samples were finally annealed at 200 °C or higher to cure the silver paste. Several 4 cm² small cells were made on each same wafer using a shadow mask during sputtering and a dedicated screen during printing. The process flow and SHJ solar cell structure can be seen in Figure 2-1.

Table 2-1 Gas flow of a-Si:H(i), a-Si:H(n) and a-Si:H(p) films.

<table>
<thead>
<tr>
<th>Gas flow (sccm)</th>
<th>a-Si:H(i)</th>
<th>a-Si:H(n)</th>
<th>a-Si:H(p)</th>
</tr>
</thead>
<tbody>
<tr>
<td>SiH₄</td>
<td>40</td>
<td>40</td>
<td>40</td>
</tr>
<tr>
<td>H₂</td>
<td>200</td>
<td>197</td>
<td>175</td>
</tr>
<tr>
<td>PH₃</td>
<td>-</td>
<td>30</td>
<td>-</td>
</tr>
<tr>
<td>TMB</td>
<td>-</td>
<td>-</td>
<td>18</td>
</tr>
</tbody>
</table>

Figure 2-1. Process flow and $n$-type SHJ solar cell structure. Either emitter type could be used for SHJ cell fabrication.
After a-Si:H depositions on n-type silicon wafers, the samples (referred as SHJ cell precursors) were typically measured by a Sinton photoconductance-decay lifetime tester to get their effective minority carrier lifetimes. Meanwhile, the implied \( V_{OC} \) and implied FF were calculated from the lifetime measurement result. For the complete SHJ cells, current-voltage (I-V) characteristics with AM 1.5G (100 mW/cm\(^2\)) illumination by a sun simulator is a direct method to get the actual device \( V_{OC} \), FF and \( J_{SC} \). To study the impact of series resistance on FF loss, Suns-\( V_{OC} \) measurement was used to extract pseudo fill factor (pFF). For precise \( J_{SC} \) value, external quantum efficiency (EQE) measurement was used to extract 300-1200 nm spectral response and the total integrated photocurrent density (\( J_{SC, EQE} \)).

### 2.2 Hydrogen Plasma Treatment on a-Si:H(i) and Device Integration

The in-situ hydrogen plasma treatment (60 W, 3.5 Torr, 500 sccm hydrogen, 250 °C; process optimization can be found in APPENDIX B) was performed on 10-nm-thick a-Si:H(i) layers on one-side polished c-Si substrates. Using these samples for spectroscopic ellipsometry measurement, Figure 2-2 shows the fitted thickness and bandgap of the a-Si:H(i) layer upon hydrogen plasma treatment. While the hydrogen plasma treatment is known to have a fast etching effect on a-Si:H(i) film [52], [69], [71], the initial bandgap of 1.71 eV of the typical device-quality a-Si:H(i) film—widens to up to 1.85 eV, corresponding to an increase in the hydrogen fraction from 16% to 30% [72].

Knowing the hydrogen plasma treatment can increase the hydrogen content in a-Si:H(i) layer, we made a lifetime test to reveal the passivation effect. Figure 2-3 shows the lifetimes of two c-Si wafers, either polished or textured, with 10-nm-thick as-deposited front a-Si:H(i) layer that later performing a subsequent hydrogen plasma treatment. The rear side of each c-Si wafer was deposited with a relative thick a-Si:H(i) layer, so the
measured lifetime result was mainly dependent on the thin front a-Si:H(i) passivation. In both cases, the lifetimes were greatly increased by a factor of >2, demonstrating the possibility of further passivation enhancement by adding additional hydrogen into the 10-nm-thick a-Si:H(i) film. Note that longer hydrogen plasma treatment could lead to lower lifetime, which is to be explained in Section 2.4.

Figure 2-2. Bandgap and thickness of intrinsic a-Si:H layers on a polished c-Si wafer upon hydrogen plasma treatment. The results were obtained by fitting ellipsometry measurements with a Tauc-Lorentz model.

Figure 2-3. Effective minority carrier lifetime of a polished/textured c-Si wafer with 10-nm-thick front a-Si:H(i) layer upon hydrogen plasma treatment. The rear side of c-Si wafer is coated with an as-deposited 50-nm-thick a-Si:H(i) layer without treatment.
Figure 2-4. Effective minority carrier lifetime of textured c-Si wafers with a-Si:H(i) symmetrical layers on both sides, or with device-relevant a-Si:H(i/p) and a-Si:H(i/n) layers, in which only a-Si:H(i) layer were treated with H$_2$ plasma. The doped a-Si:H layers were deposited after the H$_2$-plasma-treated a-Si:H(i) layers.

To make sure that this 30-second hydrogen plasma treatment recipe could transfer into the optimal a-Si:H/c-Si passivation for SHJ cell fabrication, we made a lifetime test to reveal the passivation effect on SHJ cell precursors (see Figure 2-4). Similar to the c-Si wafers with a-Si:H(i) passivating layers, the SHJ cell precursors with additional doped a-Si:H carrier-selective layers also welcome the hydrogenation plasma treatment. Note that hydrogen plasma treatment was performed only on the symmetric a-Si:H(i) layers on both side of the textured c-Si wafers. It indicates the quality of a-Si:H(i) passivation layer mainly determinates the effective carrier lifetime of the SHJ cell precursors.

Finally, we started a baseline SHJ cell run: half of the eight wafers used hydrogen plasma treatment while the remaining four wafers did not. Figure 2-5 shows the schematic SHJ cell fabrication process and the final SHJ cell parameters with and without hydrogen plasma treatment. The $J_{SC}$ and FF were statistically the same, but the two main parameters ($V_{OC}$ and $pFF$, relating to the a-Si:H passivation) were higher for the SHJ cells with the added hydrogen plasma treatment. In addition, an absolute 0.4% efficiency gain was
achieved at that time. Thus, we started to use this hydrogen-plasma-treated a-Si:H(i) recipe for all the following weekly baseline runs.

Figure 2-5. Schematic SHJ cell fabrication and SHJ cell performance before and after switching to hydrogen-plasma-treated a-Si:H(i) recipe. The SHJ cells did not have high FFs when we made full-size 156 mm×156 mm cells with a bit thick a-Si:H(i) and non-optimized ITO layers.
2.3 Dehydrogenation and Rehydrogenation of a-Si:H(i) and Device Integration

This content was published in Applied Physics Letters under the title "Plasma-initiated rehydrogenation of amorphous silicon to increase the temperature processing window of silicon heterojunction solar cells" [73]. Below are the brief results:

![Figure 2-6. Bandgap and thickness of intrinsic a-Si:H layers on a polished c-Si wafer. Data are shown for the as-deposited state, after annealing at 400 °C for 20 min, and after hydrogen plasma treatment. The a-Si:H layers were deposited on one wafer which was then broken into four pieces that were processed as indicated on the x-axis. The results were obtained by fitting ellipsometry measurements with a Tauc-Lorentz model; the error bars represent the 90% confidence intervals of the fits.](image)

The dehydrogenation of a-Si:H(i) at temperatures above 300 °C degrades its ability to passivate silicon wafer surfaces, which greatly limits the temperature of post-passivation processing steps during the fabrication of advanced SHJ or silicon-based tandem solar cells. Figure 2-6 shows the typical hydrogen fraction reduction (15.0±2.5% to 8.5±2.5%) of a-Si:H(i) after 400 °C annealing that is undesirable for c-Si surface passivation, but subsequent hydrogen fraction enhancement (8.5±2.5% to 33±3%) is achieved via applying...
a hydrogen plasma treatment—a rehydrogenation process that could help passivate a-Si:H/c-Si interface.

Figure 2-7. Effective minority-carrier lifetimes of textured c-Si wafers with intrinsic a-Si:H layers on both sides: the as-deposited state, after high-temperature annealing for 20 min, and after hydrogen plasma treatment. The a-Si:H layer thickness is varied in (a) and the annealing temperature is varied in (b).

To investigate the effective minority-carrier lifetime in textured wafers passivated with symmetric a-Si:H(i) layers, the dehydrogenation and rehydrogenation were performed and showed in Figure 2-7. After testing different a-Si:H(i) thicknesses, the annealing temperatures and the hydrogen plasma time, we find that a good dehydrogenation-and-rehydrogenation process window for the device-relevant a-Si:H(i) thickness (6-10 nm). Namely, the hydrogen plasma treatment fully restores the effective carrier lifetime to several milliseconds in textured crystalline silicon wafers coated with 8-nm-thick a-Si:H(i) layers after annealing at temperatures of up to 450 °C.
Figure 2-8. Performance of SHJ solar cells with varying treatments following deposition of the intrinsic a-Si:H layers (schematic diagram at the top). Each symbol represents the average value of three 4cm² cells on the same wafer, and the error bars indicate the maximum and minimum values.

We next tested the rehydrogenation of a-Si:H(i) layers exposed to a high-temperature step in complete SHJ solar cells to evaluate the compatibility of this process with real devices. All solar cells were identically fabricated, except for four different steps directly following the deposition of the a-Si:H(i) layers: (i) no treatment; (ii) annealing at 450 °C for 20 minutes; (iii) annealing at 450 °C for 20 minutes and then 30 seconds of hydrogen plasma treatment; and (iv) 30 seconds of hydrogen plasma treatment. Figure 2-8 shows $V_{OC}$, FF, $J_{SC}$ and efficiency of these cells: the FF and $J_{SC}$ are statistically similar for...
all four cell types, but the implied and actual $V_{\text{OC}}$s are quite different. Note that our current baseline SHJ cell processing uses the fourth type, which gives better surface passivation than the first type (no hydrogen plasma treatment). The first three types of cells show that—as anticipated from the lifetime measurements in Figure 2-7—dehydrogenation greatly degrades the implied and actual $V_{\text{OC}}$s, and rehydrogenation recovers them. Comparing the third and the fourth types reveals that rehydrogenation via hydrogen plasma treatment after dehydrogenation via annealing not only enables millisecond passivation, but also does not negatively impact light absorption and carrier transport. The efficiency of the third type of SHJ cell exceeds 19% and is statistically equivalent to the fourth type (reference cell).

In short, a SHJ solar cell subjected to annealing at 450 °C (following intrinsic a-Si:H deposition) had a $V_{\text{OC}}$ of less than 600 mV, but an identical cell that received hydrogen plasma treatment reached a voltage of over 710 mV and an efficiency of over 19%. This plasma-initiated rehydrogenation is promising to increase the temperature-processing window of SHJ solar cells.

2.4 Alleviating Hydrogen Plasma Damage to a-Si:H/c-Si Interface Passivation

This content was published in IEEE PVSC Proceedings under the title "Alleviating hydrogen plasma damage to amorphous/crystalline silicon interface passivation" [74]. Below are the brief results:

Hydrogen plasma treatment is used to enhance the interface passivation of a-Si:H/c-Si heterojunctions, but prolonged hydrogen plasma treatment can cause adverse passivation damage. Specifically, Figure 2-9a shows effective lifetimes of textured c-Si wafers with 10-nm-thick intrinsic a-Si:H on both sides before and after hydrogen plasma treatment. Performing 1-min hydrogen plasma treatment on an a-Si:H/c-Si heterojunction
results in passivation enhancement, which is attributed to atomic hydrogen diffusion to the a-Si:H/c-Si interface that reduces dangling bond density [68]. However, negative effects of hydrogen plasma treatment quickly occur—if such treatment is 2 min or longer, the a-Si:H/c-Si interface passivation plummets.

![Figure 2-9](image-url)

Figure 2-9. (a) Effective lifetimes of a textured c-Si wafer with 10-nm-thick a-Si:H before and after H₂ plasma treatment; (b) Effective lifetimes of four textured c-Si wafers encountering time-varied H₂ plasma treatment first and then being passivated with 10-nm-thick a-Si:H. All of the a-Si:H depositions and H₂ plasma treatments were performed on both sides of the samples.

One possibility to explain this lifetime degradation is that the a-Si:H layer after hydrogen plasma treatment is close to the critical minimum thickness (4-5 nm [75]) needed to provide sufficient passivation, because the hydrogen plasma treatment also etches a-Si:H films quite fast. However, in this particular case, we find that the remaining a-Si:H thickness after 2-min hydrogen plasma treatment is above 6 nm. With this film thickness, the lifetime for as-deposited a-Si:H/c-Si/a-Si:H samples is around 1.5 ms (see Figure 2-7), but a far lower lifetime (below 0.1 ms) is achieved in Figure 2-9a. Besides, other samples exhibit low lifetimes (<0.15 ms) even when >10 nm a-Si:H is still retained after prolonged hydrogen plasma treatment (reference samples without any treatment have lifetimes of 1-
Thus, we suspect that over-etching of the a-Si:H passivation layer is not the essential reason for this lifetime degradation.

Another possibility is that the underlying c-Si substrate is damaged by prolonged hydrogen plasma treatment [71]. To validate this hypothesis, we performed hydrogen plasma treatment directly on c-Si wafers, and subsequently deposited 10-nm-thick a-Si:H layers. We found that hydrogen plasma treatment causes severe damage on c-Si wafers that could not be recovered by subsequent a-Si:H passivation (see Figure 2-9b), which agrees with other reports [76], [77]. Thus, we think that the hydrogen plasma damage to the c-Si substrate is the essential cause of the interface passivation degradation for prolonged hydrogenation. Of course, as the remaining a-Si:H layer becomes thinner (because of the hydrogen plasma etching effect), the lifetime degradation is more prominent because the hydrogen plasma damage to the underlying c-Si substrates is more severe.

To alleviate the hydrogen plasma damage to the a-Si:H/c-Si interface, we inserted an additional thin silicon oxide (SiOₓ) capping layer after a-Si:H deposition and before hydrogen plasma treatment. Figure 2-10 shows effective minority-carrier lifetimes of a-Si:H/c-Si heterojunctions with SiOₓ capping layers of varied thickness (up to 2.5 nm), denoted here by the SiOₓ deposition time. Clearly, as the SiOₓ layer becomes thicker, the lifetime is higher under each hydrogen-plasma-treatment condition. In particular, the sample with 3-sec SiOₓ capping layer actually experiences lifetime enhancement upon 2-3 min of hydrogen plasma treatment, compared to the reference sample without SiOₓ capping layer that incurs lifetime degradation. Therefore, adding a SiOₓ capping layer helps alleviate the lifetime degradation of a-Si:H/c-Si heterojunctions upon prolonged hydrogen plasma treatment, especially for the sample with ~2.5-nm-thick oxide layer.
Figure 2-10. Schematic structure of sample processing and the effective minority-carrier lifetimes of textured c-Si wafers with SiO_x/a-Si:H (0-2.5 nm/10 nm) stacks on both sides, before and after H_2 plasma treatment. Before hydrogenation, the symbol represents the average value from different positions within a five-inch wafer while the error bars indicate the maximum and minimum values; this wafer was then cut into four pieces for further SiO_x deposition and the final hydrogenation.

To further investigate whether the ~2.5-nm-thick SiO_x layers can completely protect the a-Si:H/c-Si heterojunction, we performed a series of prolonged hydrogen plasma treatments on such structures until the measured lifetime decreased to near zero in Figure 2-11. We find that severe hydrogen plasma damage is greatly alleviated (slowed down by a factor of 7-10) while the hydrogen still penetrates into the underlying a-Si:H/c-Si layer for interface passivation.
Figure 2-11. (a) Effective minority-carrier lifetimes of textured c-Si wafers with SiO$_x$/a-Si:H (2.5 nm/10 nm) stacks and with a-Si:H (10 nm) layers on both sides, before and after continuous H$_2$ plasma treatment. Each symbol represents the average value of five different positions within a five inch wafer, and the error bars indicate the maximum and minimum values; (b-c) SiO$_x$ thickness, a-Si:H thickness, and a-Si:H bandgap on separate flat silicon wafers before and after H$_2$ plasma treatment (each data point corresponds to one separate sample within the same run), fit by a SiO$_x$/a-Si:H stack (two-layer fitting) with ellipsometry.

Unfortunately, SiO$_x$ capping cannot prevent the ultimate lifetime degradation after 21-min hydrogen plasma treatment, even though the a-Si:H layer still has sufficient thickness (~10 nm) and reasonable bandgap (~1.8 eV) for what should be good surface passivation. In this case, we suspect that the low lifetime may be due to the slowly accumulated hydrogen damage in the near-surface c-Si [73], which requires a set of high-quality transmission electron microscopy images or other characterization methods to confirm.
2.5 a-Si:H Layer Stack with Hydrogen Plasma Treatment

Hydrogen plasma treatment is usually performed on a-Si:H(i)/c-Si structure, either in as-deposited state (Section 2.2), or in dehydrogenated state (Section 2.3). As the additional plasma-initiated hydrogen diffuses into the a-Si:H(i) film, which effectively hydrogenates the silicon dangling bonds at the a-Si:H(i)/c-Si interface, the passivating a-Si:H contacts enable higher $V_{OC}$ of the final SHJ solar cell.

But it would be interesting and beneficial to see if the hydrogen plasma treatment could be directly applied to a SHJ cell precursor with intrinsic/doped a-Si:H layer stack. If successful, it can widen the processing window for silicon-based tandem cells with a SHJ bottom cell (e.g. the top cell can be processed at a high temperature, after the completion of the pseudo SHJ bottom cell), and unveil the fundamental physical and chemical interaction between plasma-initiated hydrogen atoms/ions and silicon surface in vacuum.

Firstly, three a-Si:H passivating structures and their lifetimes upon hydrogen plasma treatment are shown in Figure 2-12. Similar to the treatment on a-Si:H(i) layer, hydrogen plasma treatment is successfully performed on a-Si:H(i/n) layer stack without adverse effects (till up to ~3 min). However, hydrogen plasma treatment behaves differently on a-Si:H(i/p) layer stack: the lifetime does not improve—it actually decreases—during the hydrogenation process.
Figure 2-12. Schematic a-Si:H/c-Si/a-Si:H structures and effective minority carrier lifetimes upon hydrogen plasma treatment. The single a-Si:H layer is 10 nm thick, regardless what type the a-Si:H is; the total a-Si:H bi-layer is 20 nm thick.

It is known that the measured effective lifetime can be limited by defects in the a-Si:H bulk as well as defects at the sharp a-Si:H/c-Si interface [78]–[80]. The c-Si substrate is not damaged till 4-5 min hydrogen plasma treatment, as the short-time hydrogen plasma treatment cannot make detrimental damage to a c-Si wafer with 20-nm-thick a-Si:H layers. Therefore, the lifetime change in Figure 2-12 is mainly dependent on the hydrogen content and structure of the a-Si:H film, which strongly affect a-Si:H/c-Si interface [72]. The hydrogen content is studied from ellisometry fitting, and hydrogen structure within in the a-Si:H film is studied by Fourier-transform infrared spectroscopy (FTIR).
Figure 2-13. Ellipsometry-fit bandgap or thickness of a-Si:H upon hydrogen plasma treatment: one-layer a-Si:H, two-layer a-Si:H(i/n) stack and two-layer a-Si:H(i/p) stack. Tauc-Lorentz model was used results to fit the ellipsometry measurements. Each symbol respresent one particular sample within the same experiment. The colors correspond to the individual layers in the stack.

Figure 2-13 shows the change of a-Si:H bandgap upon hydrogen plasma treatment. No matter whether the a-Si:H film is doped or not, the plasma-initiated hydrogen goes into the a-Si:H layer and widens its bandgap. However, when performing hydrogen plasma treatment on the intrinsic/doped a-Si:H layer stack, it looks like the additional hydrogen goes into the underlying a-Si:H(i) film of a-Si:H(i/n) layer stack but it cannot penetrate into the underlying a-Si:H(i) film of a-Si:H(i/p) layer stack. This phenomenon could be explained by the charge-related hydrogen movement [52], or by the boron-assisted a-
Si:H(p) barrier effect—no hydrogen plasma etching in a-Si:H(p) layer, which is different from the linear etching in a-Si:H(i) or a-Si:H(n) layer. Anyway, as the bonded hydrogen content in the a-Si:H(i) layers adjacent to c-Si substrates matters most for the passivation quality—compared to undesirable but inevitable defects in doped a-Si:H, it partially explains why that hydrogen plasma treatment is successfully performed on a-Si:H(i/n) layer stack rather than on a-Si:H(i/p) layer stack.

Figure 2-14. FTIR of a-Si:H films before and after hydrogen plasma treatment: a-Si:H(i/i), a-Si:H(i/n) and a-Si:H(i/p) layer stack. The LSM (1980-2010 cm$^{-1}$, dashed curves) peak and the HSM peak (2070-2100 cm$^{-1}$, dotted curves) are fitted from the measured FTIR data after background signal subtraction (solid curves). The total a-Si:H thickness is 40 nm in each case to get decent FTIR signals.

Figure 2-14 shows FTIR curves of a-Si:H films on (111) polished c-Si wafers before and after hydrogen plasma treatment. To tell the difference of monohydride (SiH) bonds and of dihydride (SiH$_2$) bonds, a two-peak fit for low stretching mode (LSM, 1980-2010 cm$^{-1}$) and high stretching mode (HSM, 2070-2100 cm$^{-1}$) is also shown. For a-Si:H(i) film, the increased ratio of HSM to LSM corresponds to the previous report [69], indicating the a-Si:H film becomes disordered and contains more voids [81]. However, the presence of more hydrogen and increased disorder of such a-Si:H film may be close to the crystallization transition [69], which is actually good to get enhanced surfaced passivation.
For a-Si:H(i/n) layer stack, it simply follows the example of a-Si:H(i). Interestingly, the a-Si:H(i/p) layer stack has very high HSM ratio that corresponds to mostly disordered a-Si:H film with lots of voids, mainly caused by the highly defective a-Si:H(p) top layer, even before hydrogen plasma treatment; such high HSM ratio does not change much upon the afterwards hydrogen plasma treatment.

Figure 2-15. Effective minority carrier lifetime of a textured c-Si wafer with symmetric a-Si:H(n) or a-Si:H (p) layers on both sides. After doped a-Si:H deposition, the hydrogen plasma treatment was immediately performed. The symbols here represent the average measured lifetime value from five different positions within a five-inch square wafer.

To better understand the different passivation between a-Si:H(i/n) and a-Si:H(i/p) layer stacks, either before and after hydrogen plasma. We performed a comparison study of a-Si:H(n) and a-Si:H(p) passivation on textured c-Si wafers. In Figure 2-15, it is shown that a-Si:H(p) layer has very limited passivation effect. As expected, the passivation seldom changes upon performing a subsequent hydrogen plasma treatment.

Also in Figure 2-15, the as-deposited a-Si:H(n) layers have some passivation effect (400-500 μs). Surprisingly, the passivation degraded upon doing hydrogen plasma treatment on a-Si:H(n)/c-Si. While the mechanism of the passivation degradation is unclear
(even when the hydrogen content of a-Si:H increases), it indicates that the additional a-Si:H(i) layer has to be put underneath a-Si:H(n) layer, like Figure 2-12, for any positive passivation enhancement during hydrogen plasma treatment.

Indeed, we find the underlying a-Si:H(i) is essential for the potential passivation enhancement for a-Si:H (i/n) stack. A similar experiment to Section 2.3 shows that the rehydrogenation can also be performed on a-Si:H(i/n) stack after its dehydrogenation (Figure 2-16). For a-Si:H (i/n) passivation stack, the effective lifetime can be recovered to its original value after dehydrogenation and rehydrogenation.

Figure 2-16. Effective minority carrier lifetime of a textured c-Si wafer with symmetric a-Si:H(i/n) or a-Si:H (i/p) layers on both sides. The total a-Si:H layer stack thickness is 20 nm on each side; the intrinsic, n-type and p-type a-Si:H is 10 nm each. The annealing was 450 °C for 20 min, and the hydrogen plasma was conducted at 250 °C. The symbols here represent the average measured lifetime value from five different positions within a five-inch square wafer, and the error bars indicate the maximum and minimum values.

In short, hydrogen plasma treatment can increase the passivation of a-Si:H(i) and a-Si:H(i/n) stack films on the c-Si substrates, due to the more hydrogen in the a-Si:H(i) layer that is adjacent to the c-Si substrates and a possible a-Si to c-Si transition that is suitable for c-Si surface passivation. The a-Si:H(i) has to be underneath the a-Si:H(n) for
the hydrogen plasma treatment. However, hydrogen plasma treatment cannot increase the passivation of a-Si:H(i/p) stack films on the c-Si substrates, because the low hydrogen in the a-Si:H(i) layer and highly disordered a-Si:H(i/p) matrix are immune to any changes upon treatment.

2.6 a-Si:H and TCO Layer Stack with Hydrogen Plasma Treatment

For the SHJ cell fabrication, the device passivation is more limited by the a-Si:H(i/p) side rather than the a-Si:H(i/n) side, according to the literature [40] and our own experience. However, we find that it is not accessible to improve the passivation by imposing the direct hydrogen plasma treatment on such a-Si:H(i/p) layer stack. For the a-Si:H(i/n) layer stack, a follow-up question is that if this treatment can apply to a-Si:H(i/n) and TCO layer stack, which represents a pseudo rear/front SHJ cell structure for front/rear- emitter device structure before Ag metallization.

To start with, we tested the hydrogen plasma reaction with standard ITO and indium zinc oxide (IZO) layers that we used for SHJ cell fabrication. For the optical properties in Figure 2-17, we find the H₂ plasma treatment can lead to decreased transmittance of ITO or IZO layers. Such TCO layers cannot be used at the front side of solar cells due to its high absorption; however, the ITO layer after 1-min H₂ plasma treatment may be acceptable to be used at the rear side, because the decreased transmittance at 900-1200 nm is relatively small (~96% of its original value). For the electrical properties in Figure 2-18, we find the H₂ plasma treatment increases the carrier concentration for ITO and IZO. The high-mobility IZO suffers quite a lot while the ITO retains most of its mobility value. The results here are not in agreement of a previous report, which claimed that the optical and electrical IZO films should not be impacted from plasma treatment [84].
Figure 2-17. Transmittance of ITO/glass and IZO/glass samples without and with hydrogen plasma treatment. The corresponding sample photo is show on the right side.

Figure 2-18. Bulk concentration and mobility of ITO and IZO samples without and with hydrogen plasma treatment.
While the TCO layers interacts with H₂ plasma treatment strongly with degraded optoelectronic properties, it is still interesting to see if hydrogen can penetrate the TCO layers and go into the underlying a-Si:H layers for a-Si:H/c-Si interface passivation. Figure 2-19 shows quite promising result, indicating that atomic hydrogen may penetrate into the a-Si:H/c-Si interface for the passivation enhancement. The typical sputtering damage was also recovered in the same time. As expected, prolong hydrogenation treatment caused the final passivation degradation.

Figure 2-19. Effective minority carrier lifetime of a textured c-Si wafer with symmetric a-Si:H(i/n) on both sides, which was later sputtered ITO and then was treated with time-varied hydrogen plasma at 250 °C. The intrinsic and n-type a-Si:H is 10 nm each. The symbols here represent the average measured lifetime value from five different positions within a five-inch square wafer, and the error bars indicate the maximum and minimum values.

To confirm if the passivation enhancement effect comes from hydrogen plasma treatment, we performed some follow-up experiment. Unfortunately, this lifetime enhancement in Figure 2-19 is largely due to the hydrogen movement between ITO and a-Si:H stack during post-ITO thermal treatment (e.g. 250 °C hydrogen flow without RF plasma that cannot increase the hydrogen content within a-Si:H matrix). Therefore, such
an added hydrogen plasma treatment directly on ITO/a-Si:H(in) layer stack is not applicable, at least not needed, for the SHJ solar cell rear-side a-Si:H contact development.

2.7 Summary

Hydrogen plasma treatment increases the hydrogen content within the a-Si:H(i) passivating layer and decreases the dangling bond density at the a-Si:H/c-Si interface, which can be integrated into the standard n-type SHJ cell fabrication process with device performance improvement. Such hydrogen plasma also widens the SHJ cell temperature-processing window, which is desirable for advanced solar cell structure or silicon-based tandem solar cell development.

Prolonged hydrogen plasma treatment always causes passivation degradation. For the undesirable hydrogen etching and plasma damage effect, it is possible to control and alleviate such side effects by introducing a thin SiOx buffer layer.

The hydrogen plasma treatment can also increase the hydrogen content of a-Si:H(n) or a-Si:H(p) carrier-selective layer, but the passivation enhancement can only be observed in a-Si:H(i/n) layer stack with such hydrogenation treatment. It is also confirmed that the underlying a-Si:H(i) layer is essential for a-Si:H(i/n) layer stack to get passivation enhancement with hydrogen plasma treatment. For a-Si:H(i/p) layer stack, performing hydrogen plasma treatment makes little difference.

Finally, the hydrogen plasma treatment can change the transmittance, bulk carrier concentration and mobiles of ITO or IZO film. While the direct hydrogen plasma treatment is not desirable for any device structure that already have TCO layers, this hydrogen plasma treatment is highly desirable during a-Si:H film deposition for developing a-Si:H passivating and carrier-selective contacts.
CHAPTER 3

A-SI:H CONTACT FOR SHJ SOLAR CELLS: INFRARED AND FULL SPECTRUM

Within the past few years, the crystalline silicon (c-Si) cell efficiency is the main driving thrust that evolves the PV industry from one cell technology to another—and this trend will continue to be true. For example, the market share of passivated emitter rear (PERC) cells increases from 10% in 2015 to nearly 20% in 2018. It is predicted that the PERC cells, with 23% saturating efficiency, will gradually gain great significant PV market share over the back surface field c-Si cells in ten years [22]. After that, the silicon heterojunction (SHJ) solar cells, with 26.7% world-record efficiency in lab [27], are promising to offer higher saturating efficiency in PV market [22]. Then, the next-generation c-Si PV technology is envisioned as the silicon-based tandem cells—they are even expected to appear in mass production after 2019 [22].

However, silicon-based tandem cells are still in the early stage of lab-scale research due to many technology challenges. In this chapter, we discuss one specific issue: compared to a full-spectrum SHJ cell, shall the a-Si:H contact thickness be different when designing a silicon-based tandem cell?

3.1 IR-Spectrum SHJ Cells for Tandem Application

Silicon-based tandem cells, which use separate top cells and c-Si bottom cells to harvest a broad solar spectrum, can have up to 42–43% theoretical efficiency [20], [85], which is far higher than the 29.4% theoretical efficiency limit of single-junction c-Si solar cells [86]. With the existing record top and bottom cell technologies, the practical
efficiency limit of silicon-based tandem cells can be as high as 34-36% [20], which is also higher than the 26–27% world-record efficiency of single-junction c-Si solar cells. In addition, silicon-based tandems cells have quite flexibility to select various top cell materials: III-V [6], [87], [88], II-VI [89]–[91], and perovskite [6], [92]–[95]. The silicon-based tandems cells also have quite flexibility to choose different coupling configurations: two-/four-terminal, monolithic/mechanical/spectrum-split [20], [96]. Some of these tandem cells are promising to push the efficiency close to the 34–36% limit.

Within the silicon-based tandem cells, SHJ bottom cell technology is an excellent choice due to its high open-circuit voltage and spectral efficiency at long wavelength [20]. Many recent high-efficiency silicon-based tandems actually use SHJ bottom cells for two-junction tandem applications. For example, perovskite/SHJ (2-terminal, monolithic stack) cell achieved 23.6% efficiency [94]; perovskite/SHJ (4-terminal, mechanically stacked) cell got 25.2% efficiency [93]; and perovskite/SHJ (4-terminal, spectrum-split) cell obtained 28.0% efficiency [92]; and GaInP/SHJ and GaAs/SHJ (4-terminal, mechanically stacked) cells had 32.5% and 32.8% efficiency, respectively [87]). Although all these tandem devices have >23% efficiencies, the SHJ bottom cell fabrication is rarely changed and optimized compared to its single-junction application. However, two important differences when switching from a full-spectrum SHJ cell to an IR-spectrum SHJ cell—disregard near-ultraviolet and visible solar spectrum, and halved illumination intensity—could change the cell design rule.

Without considering the solar illumination from near-ultraviolet and visible spectrums, SHJ cell that works as a bottom cell (for example, 700–1200 nm) can ignore the front parasitic absorption losses (for example, ~2.1 mA/cm² in a full-spectrum SHJ cell
which gives much processing freedom on the front hydrogenated amorphous silicon (a-Si:H) layer thickness variance. Besides, our typical full-spectrum SHJ cell uses rear-emitter structure (i.e. thin n-type a-Si:H on the front, and p-type a-Si:H on the rear) rather than front-emitter structure, because the p-type a-Si:H layer—if on the front that needs limiting short-circuit current density ($J_{sc}$) loss—cannot be as thin as the n-type a-Si:H layer without reducing fill factor (FF). However, such front a-Si:H thickness constraint is no longer valid with IR-spectrum illumination, so the front-emitter cell structure may even be better.

In addition, with the halved illumination intensity that naturally leads to low $J_{sc}$, it is expected that the SHJ cell incurs lower open-circuit voltage ($V_{oc}$) but higher FF [97]. For the $V_{oc}$ and FF optimization, we need to re-evaluate the optimum cell performance mathematically under low solar spectrum illumination. At the physics level, the re-evaluation of $V_{oc}$ that is mainly affected by a-Si:H/c-Si passivation and carrier selectivity, and of FF that is mainly affected by series resistance; clearly, a-Si:H thickness is an important parameter to change the passivation, carrier selectivity and series resistance [18], [75], [98]. It should be noted that on top of a-Si:H layers, having an IR-transparent indium tin oxide (ITO) layer [62] that maintains a low a-Si:H/ITO contact resistance [99] is also important to make good IR-spectrum SHJ bottom cells, but such study is more focused on $J_{sc}$ and FF optimization, which will be reported separately.

In this work, we comprehensively vary the front a-Si:H layer thicknesses in SHJ cells with front-/rear-emitter structure, and then discuss the device performance under full and IR spectrums. A statistical analysis based on our results is also included to provide some
insights to PV industry on the IR-spectrum SHJ cell efficiency distribution by altering the a-Si:H thickness variance.

3.2 Experiment Details

We used the standard SHJ cell fabrication process to do this experiment (see Section 2.1). However, there are two notable differences here.

The first one is that we varied the front doped/intrinsic a-Si:H thicknesses and the rear intrinsic a-Si:H thickness (doped a-Si:H thickness: 6 nm, 10 nm, 20 nm; intrinsic a-Si:H thickness: 4 nm, 6 nm, 12 nm). Note that at the time of this experiment, excellent film thickness uniformity of 2.0%, 1.5%, and 2.7% over the entire 156 mm × 156 mm area was characterized in each PECVD chamber for a-Si:H(i), a-Si:H(p), and a-Si:H(n) deposition, respectively. The a-Si:H thickness in each chamber is calibrated and determined from the previous spectroscopic ellipsometry data taken on polished wafers. Except for the thickness variance shown in Figure 3-1, the a-Si:H(i), a-Si:H(p), and a-Si:H(n) layer thickness is 6 nm, 11 nm, and 5 nm, respectively.

The second one is that an optimum in-situ hydrogen plasma treatment (Section 2.2) was performed immediately after a-Si:H(i) film to improve the a-Si:H(i)/c-Si interface passivation: the thicker the a-Si:H(i) film, the more time the hydrogen plasma treatment takes.
Figure 3-1. Schematic diagram of n-type SHJ solar cells with varied front a-Si:H stack thicknesses: front-emitter (a) and rear-emitter (b).

A continuous-illumination Newport sun simulator was used to acquire the $V_{oc}$ and FF characteristics under full spectrum (AM 1.5G, 100 mW/cm$^2$) and under IR spectrum (AM 1.5G, 50 mW/cm$^2$, by cranking down the power) illumination. The $V_{oc}$ and FF at half the solar intensity are representative of the $V_{oc}$ and FF of a bottom SHJ cell with an assumed 1.75 eV wide-bandgap cell on top; note that one prerequisite for the bottom SHJ cell is to have effective minority carrier lifetimes of several milliseconds, enabling effective carrier collection in the IR wavelength range. While the condition here is not exclusively IR illumination, these measurements are specifically representative because of the long diffusion length in these high-lifetime SHJ cells. The pseudo FF was extracted from a Sinton Suns-Voc tester. The full-/IR-spectrum (300–1200 nm/700–1200 nm) $J_{sc}$ reported here was extracted from the integrated photocurrent calculated by external quantum
efficiency (EQE), measured by Solar Cell Spectral Response Measurement System (PV Measurements, Model QEX10).

### 3.3 Performance of SHJ Cells for Full- and IR-Spectrum Applications

![EQE curves of n-type SHJ solar cells with varied front a-Si:H stack thicknesses: front-emitter (a) and rear-emitter (b).](image)

Figure 3-2 shows the EQE curves of the SHJ solar cell series depicted in Figure 3-1. In both front- and rear-emitter cases, the front optical losses become severe as the a-Si:H stack becomes thicker. The short-wavelength spectral response is dependent on the front a-Si:H thicknesses [18], [75], [98]; here the collection efficiency of carriers in doped a-Si:H is lower than that in intrinsic a-Si:H [75]. Between the thinnest and thickest a-Si:H layer stacks (i.e. 4/6 nm and 12/20 nm), the $J_{sc}$ difference under full spectrum can be as large as for 2.9 and 2.7 mA/cm$^2$ for front-emitter and rear-emitter SHJ cells, respectively. However, the short-wavelength spectral response makes no difference for the IR-spectrum cells, which only collect current in the wavelength region of 700–1200 nm.
Figure 3-3. $V_{oc}$, FF, $J_{sc}$, and efficiency of SHJ solar cells with varying a-Si:H(p) and a-Si:H(i) layer thicknesses in front-emitter structure (left), and with varying a-Si:H(n) and a-Si:H(i) layer thicknesses in rear-emitter structure (right). The results under full- and IR-spectrum illumination are demonstrated. Lines are guides to the eyes.

To study the complete device performance under two illuminated spectrums, Figure 3-3 shows that $J_{sc}$, $V_{oc}$, FF and efficiency of SHJ solar cells by varying a-Si:H layer thicknesses and emitter position. Since IR-spectrum $J_{sc}$ is identical for all the SHJ cells, the tradeoff of $V_{oc}$ and FF is the only factor to impact the cell efficiency under IR spectrum illumination.
Firstly, among all the a-Si:H(i) thicknesses, 6 nm is clearly the optimum value to get highest efficiency under full or IR spectrum illumination. Upon increasing a-Si:H(i) thickness, $V_{oc}$ generally increases linearly and then saturates [18], [75], [98]; in our case, at least 6 nm is required to get decent $V_{oc}$ that is close to the saturated value. However, thicker a-Si:H(i) incurs quite a big FF loss, especially when a-Si:H(i) is 12 nm. This is due to the increased series resistance as the a-Si:H(i) becomes thick; without considering series resistance, the pseudo FF is almost identical. Take the front-emitter, full-spectrum cells for an example, the pseudo FF is almost the same: 82.6±0.3%, 82.5±0.2% and 82.5±0.5% for a-Si:H(i)=4 nm, 6 nm and 12 nm, respectively. A detailed discussion on FF and series resistance was reported separately by Weigand et al. at PVSC 2017. The tradeoff of $V_{oc}$ and FF determines the optimum a-Si:H(i) thickness to be 6 nm, which fit nicely for front- and rear-emitter SHJ structures under both full and IR spectrum illuminations.

Secondly, a thicker doped a-Si:H layer, either in front-emitter structure or in rear-emitter one, does not lead to higher efficiency of the finished SHJ cells. In most cases, the full-/IR- spectrum efficiency is the highest when the doped a-Si:H is only 6 nm, and we find that the efficiency difference with varied doped a-Si:H thicknesses becomes quite small under IR spectrum. The weak impact of doped a-Si:H thickness on efficiency is largely due to the fact that the thick doped a-Si:H layer does not give high FF (unless the a-Si:H(i) layer is 12 nm, which is not an optimum thickness for high efficiency). The phenomenon is different from [75], but it conforms with [18], [98]. Actually, 6-nm-thick doped a-Si:H layer is good enough to provide 78-80% FF when the underlying a-Si:H(i) layer is 4 or 6 nm. We do not use doped a-Si:H thickness that is below 6 nm, because the FF and $V_{oc}$ of SHJ cells would greatly drop if the doped a-Si becomes too thin, according
to our previous experiments and a separate report from H. Fujiwara and M. Kondo [98]. Simulation results by Bivour et al. indicate the critical minimum a-Si:H(p) thickness is between 4 nm (very high a-Si:H(p) net doping density) to 7.5 nm (very low a-Si:H(p) net doping density) to provide decent band bending without detrimental $V_{oc}$ and FF drop [61].

Thirdly, $V_{oc}$ decreases and FF increases experimentally upon switching from full spectrum to IR spectrum of each SHJ cell. The $V_{oc}$ is decreased by 22±2 mV, which corresponds to the logarithmical voltage calculation with approximate half of the light intensity. The absolute FF only slightly increases 0.2–0.3% when the a-Si:H(i) is 4 nm or 6 nm (FF=78.5–80%), but somehow increases 2-3% when the a-Si:H(i) is 12 nm (FF is still below 75%). As an external reference, Amir et al. observed that a SHJ cell that the authors fabricated increased ~0.9% absolute FF by lowering the illumination density from one sun to half sun (FF=77.5%) [97]. This FF and illumination dependency could be explained and modeled by taking the actual resistance losses into the consideration [100], [101].

By varying all the a-Si:H thicknesses, the optimization of SHJ cell under the full spectrum and IR spectrum is surprisingly similar: 6-nm-thick intrinsic a-Si:H coupled with 6-nm-thick doped a-Si:H on the front side. In terms of PECVD processing, there is no need to change the a-Si:H thickness from the standard full-spectrum SHJ cell to future SHJ bottom cell production.

Lastly, it is observed that SHJ cell working under the IR spectrum have a wider process window. All the SHJ cells have 11-12% IR efficiency (except one outlier), even when the intrinsic a-Si:H thickness varies from 4 nm to 12 nm and the doped a-Si:H thickness varies from 6 nm to 20 nm! Also, these SHJ cells working under the IR spectrum have the
identical current, which is desirable in tandems or cell strings when current match is required.

Having narrow efficiency and current distributions of solar cells is important and desirable for solar modules integration in PV industry. While there are many processes that can incur the cell-to-cell efficiency and current differences, the good a-Si:H film thickness uniformity—usually at the production-scale, large-area PECVD tool (chamber area $> 1 \text{ m}^2$)—is a critical parameter that directly led to the narrow efficiency and current distributions of SHJ cells under the full spectrum [102]. It is important to quantify the SHJ cell distribution via allowing a certain degree of a-Si:H film uniformity, and then compare the results between IR- and full-spectrum applications.

Specifically, we first fit the existing full-/IR-spectrum cell efficiency as a function of each a-Si:H layer thickness and then assumed 5–20% thickness variance ($\sigma$) within our a-Si:H target thickness ($t=6 \text{ nm}$). Finally, the absolute efficiency variance under full-/IR-spectrum was calculated as the maximum efficiency difference of three SHJ cell cases: with a-Si:H thickness of $t-\sigma$, $t$, and $t+\sigma$ each. Here we assume our measured cells—the champion cells with 6-nm-thick intrinsic a-Si:H coupled with 6-nm-thick doped a-Si:H on the front side—have 0% thickness variance, because the cell area is only $4 \text{ cm}^2$ and the three PECVD chambers have excellent film uniformity $156 \text{ mm} \times 156 \text{ mm}$ at the time of this experiment. As to the a-Si:H thickness variance, we set it between 5% to 20% because three separate values, $4.1 \pm 2.5\%$ [102], $<10\%$ [103], and $18\%$ [104], were reported separately for a large-area PECVD tool that usually exceeding $1 \text{ m}^2$. Note that such variance is defined from a batch of cells that are co-deposited within one large-area PECVD chamber in one run, and the temporal variance is not included here. The actual a-
Si:H PECVD film thickness uniformity can vary greatly, largely due to the varied PECVD chamber design, wafer handling, a-Si:H film recipes, tool maintenance, and many other factors.

![Graph showing absolute efficiency variance vs. front a-Si:H thickness variance](image)

Figure 3-4. Absolute efficiency variance via allowing 5–20% thickness variance in the front a-Si:H (i/p) or a-Si:H(i/n) stack layers. The results are calculated from our champion cells with 6-nm-thick intrinsic a-Si:H coupled with 6-nm-thick doped a-Si:H on the front side.

Figure 3-4 demonstrates the variability chart for absolute efficiency variance via allowing 5–20% thickness variance in the front a-Si:H (i/p) or a-Si:H(i/n) stack layers. For the production-scale, large-area PECVD tool (chamber area>1 m²), Meyer Burger and Roth & Rau demonstrated that good uniformity of a-Si:H layer characteristics (i.e. ~110-nm-thick a-Si:H layer, thickness variance=4.1±2.5%) is an essential element to achieve good uniformity of SHJ cell parameters (i.e. absolute efficiency variance=~1%) [102]. These cells can be integrated into approximately five types of solar modules, according to the typical 0.2% cell-to-cell efficiency difference within each module. Compared with their result, our statistical analysis has narrower full-spectrum efficiency variance (i.e. absolute efficiency variance=0.2–0.3% with 5% a-Si:H thickness variance), which is mainly
because that we only consider a-Si:H film uniformity and ignore other production-related factors. Also, our analysis is based on the actual SHJ cell structure (two a-Si:H layers with device-relevant thicknesses on the front sides), which could be more precise than just calibrating a-Si:H thickness in only one PECVD chamber [102]. However, both the results stress the importance of maintaining good a-Si:H film uniformity during SHJ cell production.

Under IR spectrum, however, we find the a-Si:H film uniformity requirement is relieved by a factor of 3–4 during SHJ cell production. If the a-Si:H film thickness uniformity is not satisfactory, such cells can be alternatively used as good IR-spectrum SHJ cells for two simple reasons: the front a-Si:H stack thickness optimization is the same; the absolute cell-to-cell efficiency variance is much less. In addition, the cell-to-module integration could be much easier under IR spectrum illumination. For example, if the a-Si:H thickness variance is as large as 20% for a batch of SHJ cells and the typical 0.2% cell-to-cell efficiency difference is allowed within each solar module, these cells need to selected into 5–6 module types under full-spectrum illumination. However, the same cells can be easily integrated into only 1–2 module types under IR-spectrum illumination. All these features of IR-spectrum SHJ cells suggest a potential way for developing initial tandem modules without costing a lot of money.

Besides, another way to capitalize on the reduced a-Si:H film uniformity requirement of IR-spectrum SHJ cell is that the a-Si:H deposition process could be much cheaper—for example, no need to buy a more expensive PECVD tool to guarantee higher film uniformity, and less maintenance costs to limit the non-uniform plasma power on the edge [103]. According to one SHJ PECVD equipment manufacturer that we interviewed, there
is clearly a trade-off between PECVD cost and thickness uniformity, and decreasing the thickness uniformity requirement to ±20–30% would result in a “big, big simplification of the machine”. Note that the a-Si:H PECVD tool is the most expensive equipment in a silicon solar cell production line [105], currently at 10–12 million US dollars for an 80–140 MW/year production line. With flexible uniformity requirement, this low-PECVD-cost approach help accelerate the production of tandem cells with SHJ bottom cells and could finally make SHJ bottom cells for tandem applications competitive in PV industry.

With such a wider a-Si:H processing window for IR-spectrum SHJ cells, we predict that it will be easier for PV companies to fabricate these bottom cells, to match current for top and bottom cells in tandem (if monolithic stack), and to perform subsequent solar module integration with narrowly distributed tandem efficiency and current distributions.

3.4 Summary

The device performances of front-/rear-emitter SHJ cells, with different front intrinsic and doped a-Si:H layer thicknesses, are measured and analyzed under full and IR spectrum illumination. Although IR-spectrum cells do not have front-parasitic-absorption limitation—only $V_{oc}$ and FF tradeoff matters, the design rule of front a-Si:H stack is the same for a SHJ cell working under IR and full spectrum illumination. Based on our best SHJ cell efficiency with the optimized a-Si:H thicknesses, the statistical analysis suggests the efficiency variance loss decreases by a factor of 3–4, if we switch the full spectrum into IR spectrum illumination. The simple no-thickness-change a-Si:H deposition and its high-film-uniformity tolerance in large-area PECVD chambers (i.e. low cost or high performance) essentially make SHJ IR-spectrum cells attractive to industrial PV companies. Important for the subsequent solar module integration, this advantage of
narrow efficiency distribution from using tandem solar cells with SHJ bottom cells over using the standard SHJ single-junction cells can be fully realized, if the wide-bandgap top cells (e.g. perovskite, II-VI, or III-V) also have similar or better efficiency-uniformity distribution.
CHAPTER 4

COMMERCIAL-GRADE P-TYPE SILICON CELLS WITH A-Si:H CONTACT

In previous chapters, the a-Si:H contact provides excellent surface passivation and carrier selectivity for SHJ solar cells, resulting in excellent $V_{OC}$ and FF (typically >725 mV and >77%) and high cell efficiency (typically ~21%) at ASU. Note that all these results are dependent on using high-quality n-type mono-crystalline wafers for SHJ cell fabrication.

![Different wafer types](image)

Figure 4-1. World market shares for different wafer types [22].

Figure 4-1 shows the world market shares for different wafer types. While it is estimated that the market share of n-type mono-crystalline silicon wafers will increase from 2017 to 2027, over 90% of the PV market uses p-type wafers currently and this portion will only slowly decrease to 70% in 2027. At least for the next ten years, an interesting question needs answering: Could the a-Si:H contact works on low-cost p-type mono- and multi-crystalline silicon wafers as well?
4.1 Process Design for High-Efficiency P-Type SHJ Cells

Detailed comparison of $p$-type and $n$-type Czochralski (CZ) silicon wafer and cell technology can be found in [106]. One key point is that compared to high-quality $n$-type monocrystalline CZ silicon wafers with lifetimes of several milliseconds, the commercial-grade $p$-type wafers used for mass production often have much lower lifetimes (below 200 μs), which would lead to substantially lower $V_{OC}$ and efficiency values. Therefore, improving the wafer quality is required to develop a high-efficiency $p$-type SHJ cell technology.

Gettering and bulk hydrogenation [106]—usually occurred during the homojunction cell fabrication (e.g. BSF and PERC)—enhance $p$-type c-Si bulk quality and lead to $V_{OC}$ of up to $\sim$680 mV for a complete PERC cell. However, such gettering and bulk hydrogenation are not included in the standard SHJ cell fabrication (Section 2.1), in which the low-temperature processing inhibits the potential gettering effect and the hydrogen passivation into the c-Si bulk. To solve this issue, we first perform the gettering and bulk hydrogenation on the commercial-grade $p$-type silicon wafers, and then complete the SHJ cell fabrication. We expect that better $p$-type SHJ solar cells can be made via pre-fabrication getting and bulk hydrogenation.

4.2 P-Type CZ Monocrystalline SHJ Cells

The content in this section was published in Solar RRL under the title "Pre-Fabrication Gettering and Hydrogenation Treatments for Silicon Heterojunction Solar Cells: A Possible Path to $>700$ mV Open-Circuit Voltages Using Low-Lifetime Commercial-Grade p-Type Czochralski Silicon" [107]. Below are the main results:
This experiment is in collaboration with the University of New South Wales (UNSW), where mature and repeatable gettering and hydrogenation processes have developed in the last few years. We used Commercial-grade $p$-type monocrystalline CZ silicon wafers (200 µm thick) with a bulk resistivity of $1.6\pm0.2$ Ω.cm. After saw damage etched in a potassium hydroxide solution, these wafers and divided into four primary processing groups:

- Control: no gettering or hydrogenation;
- G: gettering only;
- H: hydrogenation only;
- G+H: gettering and hydrogenation.

Substrates in groups G and G+H underwent RCA cleaning followed by a POCl$_3$ diffusion, resulting in a heavily doped $n^+$-emitter layer on both sides with a sheet resistance of approximately 35 Ω/sq. A short dip in 2% HF solution for 2 minutes was used to remove the phosphosilicate glass. Subsequently, wafers in all groups were alkaline textured to remove approximately 10 µm from each surface, including the diffused emitters in group G and G+H.

In preparation for hydrogenation treatment, wafers in groups H and G+H underwent RCA cleaning, and were coated 75-nm-thick hydrogenated silicon nitride (SiN$_x$:H) layers on both sides from a Roth & Rau MAiA PECVD system. The introduction of hydrogen into the silicon bulk was initiated through an industrial Schmid fast-firing metallization belt furnace, with a peak wafer temperature of $740\pm6$ °C (Q18 Datapaq) and a belt speed of 4.5 m/s. The samples were then dipped in 49% HF solution until hydrophobic to remove the SiN$_x$:H dielectric layers.
After getting these samples from UNSW, a similar SHJ cell fabrication process (Section 2.1, except for surface texturing) was applied to make $p$-type SHJ solar cells at ASU. We used front-emitter SHJ structure: 6-nm-thick a-Si:H(i) and 5-nm-thick a-Si:H(n) films on the front side of the $p$-type silicon wafers, and 6-nm-thick a-Si:H(i) and 11-nm-thick a-Si:H(p) films on the rear side. Note that in-situ 30-second-long hydrogen plasma treatment (Section 2.2) was performed immediately after a-Si:H(i) film to improve the a-Si:H(i)/c-Si interface passivation. For each group, we made two types of samples: one is the SHJ precursors with a-Si:H films—for the photoconductance lifetime measurements, and the other one is the complete SHJ solar cell, which underwent the remaining processes: front ITO, rear ITO and Ag, and front Ag screen printing.

For SHJ solar cell precursors with only a-Si:H layers, the addition of pre-fabrication gettering and bulk hydrogenation processes before SHJ processing had a profound impact on $\tau_{\text{eff}}$ and implied $V_{\text{OC}}$ (see Figure 4-2). The control samples with no prior processing reveal the initial wafer lifetimes of only 25 $\mu$s, whereas groups G and H demonstrated $\tau_{\text{eff}}$ values of approximately 50 $\mu$s and 75–100 $\mu$s, respectively. However, the most significant improvement was achieved using both gettering and hydrogenation (G+H), with $\tau_{\text{eff}}$ values of 125–150 $\mu$s. The total dark saturation current density ($J_0$) of all samples was 0.5–3.5 fA/cm$^2$, and hence the $\tau_{\text{eff}}$ was limited by bulk recombination. The results highlight the complementary nature of gettering and hydrogenation for attacking orthogonal defects and hence the importance of using both methods to increase the bulk lifetime of $p$-type silicon wafers, in agreement with previous studies [106], [108]. The corresponding improvement in the average implied $V_{\text{OC}}$ was from 615 mV on the control samples to an impressive 689 mV on samples with gettering and hydrogenation.
Figure 4-2. Impact of pre-fabrication gettering and hydrogenation on (a) the effective minority carrier lifetime (τ_{eff}) at Δn=1×10^{15} cm^{-3} and (b) the 1-sun implied V_{OC} for silicon heterojunction solar cell precursors fabricated on commercial-grade p-type CZ silicon wafers. Samples fall into four groups: non-gettered and non-hydrogenated control samples (Control), gettered samples (G), hydrogenated samples (H), and samples with both gettering and hydrogenation (G+H). Error bars represent the minimum and maximum values measured within 9 points across a single independent wafer in each group.

Table 4-1 Active-area J-V parameters of the champion cells within each group on monocrystalline silicon wafers.

<table>
<thead>
<tr>
<th>Group</th>
<th>J_{SC} (mA/cm²)</th>
<th>V_{OC} (mV)</th>
<th>FF (%)</th>
<th>pFF (%)</th>
<th>η (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control</td>
<td>38.0</td>
<td>621</td>
<td>68.9</td>
<td>80.2</td>
<td>16.3</td>
</tr>
<tr>
<td>Hydrogenating (H)</td>
<td>39.2</td>
<td>628</td>
<td>66.4</td>
<td>74.6</td>
<td>16.4</td>
</tr>
<tr>
<td>Gettering (G)</td>
<td>38.8</td>
<td>643</td>
<td>68.9</td>
<td>79.6</td>
<td>17.2</td>
</tr>
<tr>
<td>G+H</td>
<td>39.3</td>
<td>692</td>
<td>69.6</td>
<td>78.3</td>
<td>18.9</td>
</tr>
<tr>
<td>Al-BSF screen print</td>
<td>37.0</td>
<td>643</td>
<td>79.5</td>
<td>-</td>
<td>18.9</td>
</tr>
</tbody>
</table>

The lifetime enhancements translated to significant improvements in the electrical performance of finished solar cells. Table 4-1 shows the performance of conventional Al-BSF solar cells, as well as SHJ solar cells with and without gettering and bulk hydrogenation. The control SHJ solar cells had extremely poor electrical parameters with an average V_{OC} of only 621 mV. This is even lower than that of the relatively low-
efficiency Al-BSF solar cell structure with a $V_{OC}$ of 643 mV, which is higher most likely because of natural gettering and bulk hydrogenation that occurs during Al-BSF solar cell fabrication. This highlights the incompatibility of conventional SHJ solar cell processing with low-lifetime silicon wafers. However, with the addition of gettering and hydrogenation before SHJ fabrication, the $V_{OC}$ increased by more than 70 mV, to 692 mV, higher than that of current state-of-the-art PERC solar cells [109]. This corresponded to an average efficiency enhancement of 2.7% absolute. EQE measurements indicated a significant increase in the long-wavelength response of the devices through the incorporation of both gettering and hydrogenation (see Figure 4-3). This increase is consistent with the expectations of increasing lifetime in a front-emitter device structure with an improvement in minority carrier diffusion length from 25 µm to 85 µm – approximately half the thickness of the wafers.

![Figure 4-3. External quantum efficiency (EQE) of $p$-type SHJ solar cells fabricated on commercial-grade CZ silicon wafers.](image)

To our knowledge, the $V_{OC}$ of 692 mV achieved in this work is the second highest ever reported for a $p$-type CZ silicon solar cell and equal to that reported by Descoedures
et al. [110]. The only higher value we are aware of is 729 mV reported by Bätzner et al. [111].

In short, we have used gettering and bulk hydrogenation to improve the $p$-type wafer quality, and then applied a-Si:H passivating and carrier-selective contacts to form an integrated $p$-type c-Si solar cell fabrication process. The $V_{OC}$ of 692 mV achieved in this work is quite promising to develop high efficiency $p$-type SHJ solar cells.

4.3 Advanced Hydrogenation Process

The typical SHJ cell processing temperature is performed between 200 °C and 250 °C, which could undesirably form boron-oxygen defects in $p$-type c-Si wafers. Post-fabrication advanced hydrogenation process (AHP) [112]–[114] could help to eliminate this light-induced degradation of $p$-type SHJ cells.

Using high-intensity laser, this AHP developed at UNSW is to change the charge states of hydrogen and allow the hydrogen to passivate the defects within the $p$-type c-Si bulk. Here we used 300 °C, 10 s laser hydrogenation process (938 nm, >100 suns) on the fabricated $p$-type monocrystalline SHJ cells. Note that AHP itself does not incurs additional hydrogen into the solar cell; thus, the hydrogen source could be from the imposed hydrogenation in the $p$-type wafer, and also from the hydrogen-plasma-treated a-Si:H layers. For instance, we found that the boron-oxygen defects were passivated even without the bulk pre-hydrogenation process. Further experiments could be interesting to identify the main hydrogen source.

Comparing Tables 4-1 and 4-2, the most promising result is that AHP further improves the device $V_{OC}$ and efficiency, especially for G+H group. This $V_{OC}$ enhancement is due to the bulk defect passivation, which was verified by doing the same AHP on SHJ
solar cell precursors (G+H group): the \( \tau_{\text{eff}} @ 10^{15} \text{ cm}^{-3} \) was increased from 140 \( \mu \text{s} \) to 260 \( \mu \text{s} \). Thus, AHP is an effective method to improve \( V_{OC} \) of \( p \)-type CZ-Si solar cells, resulting in an impressive 707 mV.

Table 4-2 Active-area J-V parameters of the champion cells within each group on mono-crystalline silicon wafers after AHP. The same G+H+AHP cell (*) was certified by SERIS Characterisation Team independently; the lower \( J_{SC} \) (**) is due to the aperture current density value.

<table>
<thead>
<tr>
<th>Group</th>
<th>( J_{SC} ) (mA/cm²)</th>
<th>( V_{OC} ) (mV)</th>
<th>FF (%)</th>
<th>( \eta ) (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control+AHP</td>
<td>39.0</td>
<td>630</td>
<td>66.3</td>
<td>16.4</td>
</tr>
<tr>
<td>H+AHP</td>
<td>38.0</td>
<td>635</td>
<td>70.0</td>
<td>16.7</td>
</tr>
<tr>
<td>G+AHP</td>
<td>38.5</td>
<td>673</td>
<td>67.9</td>
<td>17.6</td>
</tr>
<tr>
<td>G+H+AHP</td>
<td>39.5</td>
<td>707</td>
<td>72.1</td>
<td>20.1</td>
</tr>
<tr>
<td>G+H+AHP (*)</td>
<td>34.4 (**)</td>
<td>707</td>
<td>74.1</td>
<td>18.0</td>
</tr>
<tr>
<td>UNSW PERL [6]</td>
<td>42.7</td>
<td>706</td>
<td>82.8</td>
<td>25.0</td>
</tr>
</tbody>
</table>

To our knowledge, this \( V_{OC} \) is the highest independently confirmed value reported for a solar cell fabricated on \( p \)-type CZ silicon wafers, which surpasses the \( V_{OC} \) obtained on the 25% efficient world-record \( p \)-type PERL cell (706mV) fabricated on a high-lifetime float-zone silicon wafer [6]. This \( V_{OC} \) thus suggests that \( p \)-type CZ silicon wafers of modest quality could be capable of efficiencies approaching 25% in the near future.

### 4.4 P-Type Multi-Crystalline SHJ Cells

Compared to \( p \)-type mono-crystalline silicon wafers, the \( p \)-type multi-crystalline silicon wafers have additional crystallographic defects that could limit their bulk quality. Thus, higher concentrations of impurities, dislocations and other types of defects are often found in the multi-crystalline silicon wafers.

This experiment is also in collaboration with UNSW. We used commercial-grade high-performance \( p \)-type multi-crystalline silicon wafers (200 \( \mu \text{m} \) thick) with a bulk resistivity of 1.8\( \pm \)0.2 \( \Omega \text{cm} \). Similar to the process in Section 4.2, we also divided the
samples into four groups, and made the SHJ precursors with a-Si:H films and the complete SHJ solar cells for each group.

Figure 4-4 shows PL images in the various evolutions in multi-crystalline bulk quality. With hydrogenation alone, an improvement can be seen within the intragrain regions corresponding to an approximate 30 mV increase in the implied $V_{OC}$. With gettering alone, intra-grain regions also improve, in addition to passivation of any residual saw damage. With both processes incorporated, we achieve further passivation of grain boundaries, suggesting that gettering is essential to enhancing the responsiveness of the material to the hydrogenation process, particularly around grain boundaries. Combing gettering and hydrogenation processes, implied $V_{OCS}$ of approximately 700 mV were achieved.

![Figure 4-4. Implied $V_{OC}$ calibrated photoluminescence images of sistering multicrystalline wafers after undergoing no treatment (C), hydrogenation treatment (H), gettering treatment (G) and both hydrogenation and gettering treatment (G+H).]
Table 4-3 Active-area J-V parameters of the champion cells within each group on multicrystalline silicon wafers. The same G+H+AHP cell (*) was certified by SERIS Characterisation Team independently; the low \( J_{SC} \) (**) is due to the small aperture current density value and inclusion of the inactive surrounding area, resulted from accidental cell breakage.

<table>
<thead>
<tr>
<th>Group</th>
<th>( J_{SC} ) (mA/cm(^2))</th>
<th>( V_{OC} ) (mV)</th>
<th>FF (%)</th>
<th>( \eta ) (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Control +AHP</td>
<td>30.7</td>
<td>640</td>
<td>62.9</td>
<td>12.3</td>
</tr>
<tr>
<td>H+AHP</td>
<td>29.3</td>
<td>685</td>
<td>67.9</td>
<td>13.6</td>
</tr>
<tr>
<td>G+AHP</td>
<td>28.8</td>
<td>687</td>
<td>68.9</td>
<td>13.7</td>
</tr>
<tr>
<td>G+H+AHP (*)</td>
<td>19.6 (**), 702</td>
<td></td>
<td>72.1</td>
<td>9.92</td>
</tr>
<tr>
<td>Jinko p-type PERC [6]</td>
<td>40.6</td>
<td>672</td>
<td>80.9</td>
<td>22.0</td>
</tr>
<tr>
<td>FhG-ISE n-type TOPCon [115]</td>
<td>41.1</td>
<td>674</td>
<td>80.5</td>
<td>22.3</td>
</tr>
</tbody>
</table>

Table 4-3 shows that multi-crystalline silicon cells that were subsequently fabricated. Combing gettering and hydrogenation, a-Si:H passivating and carrier-selective contacts, and the AHP treatment, we achieved \( V_{OC} \) of up to 702 mV in \( p \)-type multi-crystalline cells. To our knowledge, it is by far the highest value in multi-crystalline solar cells, which is substantially higher than that of the industrial \( p \)-type PERC cell and that of the record \( n \)-type TOPCon cell.

### 4.5 Optical Losses of \( P \)-Type SHJ Cells

From Table 4-2 and Table 4-3, it can be found that the multi-crystalline cells have quite lower \( J_{SC} \) values than the mono-crystalline cells. This ~8 mA/cm\(^2\) difference is mainly due to the difficulty of getting good surface texturing in multi-crystalline wafers, thus causing large \( J_{SC} \) loss in the wavelength range of 400-800 nm (Figure 4-5). The EQE curves of multi-crystalline SHJ cells are similar to the simulation work by Manzoor \textit{et al.} [116], indicating the wafer surface is quite flat.
Figure 4-5. EQE curves of multi-crystalline cells after undergoing no treatment (C), hydrogenation treatment (H), gettering treatment (G) and both hydrogenation and gettering treatment (G+H), and mono-crystalline cell as the reference. The multi-crystalline wafers were etched in acidic solution, and the mono-crystalline wafers were textured with random pyramids in alkaline solution.

Indeed, while mono-crystalline silicon wafers can be easily textured in alkaline solution with quite low surface reflectance, the texturing of multi-crystalline silicon wafers is not very straightforward. For 156 mm×156 mm multi-crystalline silicon wafers, the isotropic acidic texturing process [117] is not currently available at ASU or UNSW. Other alternative texturing methods [118]–[123] are interesting, but the surface roughness (e.g. nano-structured surface) may be a challenge to get conformal a-Si:H film deposition.

For both mono-crystalline and multi-crystalline silicon wafers, the parasitic absorption of front a-Si:H layers decreases the J_{SC} of the solar cells. One idea is to try a hybrid SHJ cell structure (e.g. homo-junction on the front and a-Si:H(i/p) contact on the rear, as it is shown in Figure 4-6) on p-type silicon wafers to improve the short-wavelength
response for high $J_{SC}$. Also, the use of $n^+$ emitter and SiN$_x$:H layers allows for natural gettering and bulk hydrogenation.

![Schematic diagram of hybrid SHJ cell structure.](image)

**Figure 4-6.** Schematic diagram of hybrid SHJ cell structure.

<table>
<thead>
<tr>
<th>Process Step</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.6 ± 0.2 Ω-cm B doped CZ Silicon</td>
</tr>
<tr>
<td>POCl$_3$ diffusion with 65 Ω/sq</td>
</tr>
<tr>
<td>Rear etching</td>
</tr>
<tr>
<td>Front: 75 nm SiN$_x$:H</td>
</tr>
<tr>
<td>Rapid annealing process at 740 °C</td>
</tr>
<tr>
<td>Rear: 6 nm a-Si:H(i) + 11 nm a-Si:H(p) + 150 nm ITO + Ag</td>
</tr>
<tr>
<td>Dopant application</td>
</tr>
<tr>
<td>Laser doping</td>
</tr>
<tr>
<td>Ni/Cu/Ag light induced plating</td>
</tr>
<tr>
<td>AHP + light soaking</td>
</tr>
</tbody>
</table>

**Figure 4-7.** Fabrication process flow of hybrid SHJ cells.

Using the fabrication process flow in Figure 4-7, we therefore made hybrid SHJ and full SHJ cells. Figure 4-8 shows the short wavelength EQE enhancement by using the hybrid SHJ cell. Without front parasitic absorption, replacing the front a-Si:H(i/n) layer stack by the homo-junction $n^+$ emitter layer lead to high $J_{SC}$; up to 3.6 mA/cm$^2$ can be gained according to our simulation [124]. However, this hybrid SHJ cell was limited by the front heavily doped $n^+$ emitter layer, thus the final $V_{OC}$ was restricted to 657 mV. This
low $V_{oc}$ was also partly resulted from possible contamination during the fabrication process.

In terms for the a-Si:H(i/p) contact on the rear, selecting the optimized a-Si:H(i) thickness on top of defect-rich a-Si:H(p) layer is also important, as it was shown in [125]. Overall, the front emitter quality, clean surface/interface without contamination, and rear a-Si:H contact quality need to be carefully designed for future experiments.

4.6 Fill Factor Losses of P-Type SHJ Cells

From Table 4-2 and Table 4-3, it can be also found that FFs of these $p$-type SHJ solar cells need improving. Indeed, the $p$-type SHJ cells do not have as high FF as the $n$-type counterparts. Note that $p$-type SHJ cell precursors typically have low effective lifetimes at low injection [110]—we also confirmed this effect in Figure 4-9, which is the key challenge for the FF enhancement in $p$-type SHJ cells [111] (also can limit the achievable FF for $n$-
type SHJ cells [126]). Indeed, the minority carriers (electrons) in $p$-type c-Si are more easily lost at the interface due to the larger capture cross section of the interface defects for electrons [110]. As a result, the $p$-type c-Si wafers suffer more from surface defect-assisted minority carrier recombination than the typical $n$-type ones [110]. The authors also claimed that the drop in lifetimes at low injection is not dominated by the band bending configuration at the interface [110], indicating that changing the doped a-Si:H type on top of the a-Si:H(i) layer is not a solution.

Clearly, we think the key for solving the low effective lifetimes at low injection is to optimize the passivating quality at the a-Si:H(i)/c-Si interface. One approach is to change the a-Si:H(i) layer thickness and its hydrogen content specifically for $p$-type wafers, similar to what has been done for $n$-type wafers in Chapter 2 and Chapter 3. Another approach is to create a lightly diffused $n^+$ emitter for the $p$-type c-Si wafers, possibly facilitating the electron transport at the a-Si:H electron contact. We have gotten some encouraging results from this approach.

Assuming that the injection-dependent lifetime issues are greatly alleviated (or fully solved ideally), the $p$-type SHJ cell precursors can have quite good implied FF values. The next step is using contact resistivity metrology [99] and total series resistance analysis (internally developed at ASU) to evaluate the resistance loss for each component (silicon bulk, a-Si:H, TCO, metal, etc.) for the actual FF optimization.
Figure 4-9. Injection-dependent minority carrier lifetime of \( p \)-type mono-crystalline SHJ cell precursors with no treatment (Control), gettering treatment (G), hydrogenation treatment (H), both gettering and hydrogenation treatment (G+H) with an additional advanced hydrogen process step (G+H+AHP).

4.7 Summary

\( a\)-Si:H contact can also work to fabricate \( p \)-type mono- and multi-crystalline silicon cells with \( V_{OC} \) of >700 mV, if the commercial-grade \( p \)-type wafers are pre-treated via gettering and hydrogenation to improve the bulk quality and the SHJ cells are post-treated via high-intensity laser process. For the c-Si bulk quality, gettering can remove impurities from the bulk, and hydrogenation can subsequently passivate the remaining impurities. Interestingly, the high-intensity laser process is used to change the charge states of hydrogen and allow the hydrogen to passivate the defects within the silicon bulk. The hydrogen source could be from the imposed hydrogenation in the \( p \)-type wafer, and/or from the hydrogen-plasma-treated \( a\)-Si:H layers. In additional to the high \( V_{OC} \), continuous
efforts on improving the $J_{sc}$ and FF are required to better use a-Si:H contacts for $p$-type silicon cells.
CHAPTER 5

CADMIUM TELLURIDE SOLAR CELLS WITH a-Si:H CONTACT

In addition to the success of using a-Si:H contact in c-Si solar cells, another success using a-Si:H contact is demonstrated in the mono-crystalline cadmium telluride (CdTe) thin-film solar cells. In particular, $p$-type a-Si:H or a-SiC:H is used as a hole-selective contact layer in CdTe cells with wide-bandgap CdMgTe passivating layers. A world-record $V_{OC}$ of 1.1 eV is achieved in such CdMgTe/CdTe/CdMgTe double-heterojunction device structure [41]. Further device optimization lead to a total-area efficiency of 18.5% ($V_{OC}$=1.09 V and FF=75.7%) measured at ASU [42].

However, the PV industry still uses poly-crystalline CdTe cells for the mass production. The $V_{OC}$s in these poly-crystalline CdTe cells are much lower, typically <0.85 V. In this chapter, we try to apply a-Si:H contact into the industry-preferred poly-crystalline CdTe cells to see if higher $V_{OC}$ and FF parameters are achievable.

5.1 Mono-Crystalline CdTe Solar Cells with a-Si:H Contact

This part is in collaboration with ASU MBE Optoelectronics Group, where high-quality mono-crystalline CdTe and CdMgTe layers have developed via molecular beam epitaxy (MBE) in the last few years.

The high $V_{OC}$ and efficiency in mono-crystalline CdTe cells [41] are achieved by using high bulk carrier lifetime $n$-type CdTe as PV absorber, wide-bandgap CdMgTe barriers to confine the minority carriers and reduce interface recombination velocity, and heavily doped $p$-type a-Si:H or a-SiC:H contact to facilitate transport of holes and impede...
holes electrons. To understand the carrier transport at the front side of the device, the device structure and its band diagram are shown in Figure 5-1. Specifically, $p$-type a-Si:H or a-SiC:H contact enables transport of holes across the front-side CdMgTe barrier while simultaneously blocking electrons by the large conduction-band offset [41].

![Figure 5-1. The device structure (CdTe/CdMgTe solar cell with a hole-selective a-SiC:H contact) and its band diagram [41].](image1)

Figure 5-2. (a) $V_{OC}$ values in relations to CdMgTe (30% or 40% Mg ratio, 5 or 10 nm in thickness) barrier layer and hole-selective contact layer (ITO only, a-Si:H(p)/ITO or a-SiC:H(p)/ITO); (b) FF versus $V_{OC}$ values for all the devices measured and showed in (a) [41].
Figure 5-2 shows the $V_{oc}$ and FF values by putting different front hole-selective contact layers on CdMgTe barrier layer. In terms of the passivating barrier layer, 10-nm-thick CdMgTe (Mg=40%) film is preferred to confine the minority carriers and reduce interface recombination velocity, thus increasing the final device voltage after hole-contact formation. As to the hole-selective contact layer, putting a heavily doped $p$-type a-SiC:H contact layer after CdMgTe passivating layer, yields a greatly enhanced $V_{oc}$ of up to 1.1 V. However, the relative lower FF of device with a-SiC:H contact layer—compared to a-Si:H contact layer—inhibits such hole-contact layer to become the most promising choice for mono-crystalline CdTe cells. Therefore, the $V_{oc}$ and FF tradeoff makes the $p$-type a-Si:H contact layer our preferred choice for future CdTe device integration.

It should be mentioned that both CdMgTe and $p$-type a-Si:H properties affect the $V_{oc}$ and FF of the final CdTe device: a further CdMgTe/a-Si:H optimization could help to facilitate the hole transport and keep low interface recombination velocity. Also, the low $J_{sc}$, largely due to reflection and parasitic absorption, limits the initial mono-CdTe device efficiency to 17% [41]. Thus, a detailed device optimization improve the active-area efficiency to 20.3% by using SiO$_x$/ITO electrode stack on top of the thickness-varied $p$-type a-Si:H contact for the monocrystalline CdTe/MgCdTe solar cell [42].

Table 5-1 PV parameters of monocrystalline CdTe/MgCdTe solar cell with different hole contact materials [127].
It should also be noted that the heavily doped $p$-type a-Si:H contact is not the only hole-contact material for monocry stalline CdTe/MgCdTe solar cells. However, Table 5-1 shows that the $p$-type a-Si:H is still the optimum choice of all the different hole-contact materials in monocry stalline CdTe/MgCdTe solar cell till now.

5.2 Difference between Mono- and Poly-Crystalline CdTe Solar Cells

Except for the grain boundary issue, the mono- and poly-crystalline CdTe cells should share a similar design rule in principle. However, we find transferring the success of using a-Si:H contact from the mono-crystalline CdTe cells into the polycrystalline CdTe cells is not as easy as it sounds. There are several technological differences between the two types of CdTe cells.

Table 5-2 Major differences between mono- and poly-crystalline CdTe cells.

<table>
<thead>
<tr>
<th>Absorber Type</th>
<th>Grain boundary</th>
<th>CdCl$_2$ needed</th>
<th>CdMgTe passivating</th>
<th>Contact position</th>
<th>Contact Stack</th>
</tr>
</thead>
<tbody>
<tr>
<td>mono-CdTe cell</td>
<td>$n$-type</td>
<td>No</td>
<td>No</td>
<td>Yes</td>
<td>Front</td>
</tr>
<tr>
<td>poly-CdTe cell</td>
<td>$p$-type</td>
<td>Yes</td>
<td>Yes</td>
<td>No</td>
<td>Rear</td>
</tr>
</tbody>
</table>

Table 5.2 shows the major differences between our mono-crystalline CdTe solar cells with CdMgTe/a-Si:H contact and the state-of-the-art poly-crystalline CdTe cells. In terms of absorber material quality, the $p$-type poly-crystalline CdTe has low carrier concentration, high bulk defect density, and recombination at grain boundaries [128]. The fundamental material difference between mono- and poly-crystalline CdTe—the recombination at grain boundaries—can be greatly alleviated by a follow-up CdCl$_2$ treatment. Actually, this CdCl$_2$ treatment is essential for CdTe grain boundary passivation by putting chlorine on tellurium vacancies as well as for other positive effects on CdTe
recrystallization, grain growth, removing stacking faults [129]–[131]. Experimentally, the cell efficiency can greatly increase (below 10% → up to 18%) by adding this CdCl₂ treatment. The wide-bandgap CdMgTe passivating barrier is not commonly used in polycrystalline CdTe cell fabrication, though there are two reports on using CdMgTe as an effective electron reflector film [132], [133]. Different rear contact materials (e.g. ZnTe [134] and Te [135]) have been used to form the final devices, though none of these materials is believed to be ideal for polycrystalline CdTe cells.

In p-type polycrystalline CdTe cells, the maximum achievable Vₜₜₒₜ_c—a without considering interface recombination, Fermi-level pinning, and non-ideal ohmic contact—is mainly related to the hole concentration and bulk lifetime [136], [137]. For example, the maximum Vₜₜₒₜ_c is ~910 mV for CdTe absorber with 10¹⁵ cm⁻³ hole concentration and 10 ns bulk lifetime [136]. Increasing hole density for the high built-in potential, or increasing bulk lifetime via reducing bulk defect density can enhance the maximum Vₜₜₒₜ_c value [138], which can be addressed by Group V doping or chlorine passivation for CdTe bulk.

Assuming p-type polycrystalline CdTe has high hole density and bulk lifetime, the rear contact formation is the next big problem to achieve high Vₜₜₒₜ_c. Without any intermediate rear contact materials, it is difficult to find an appropriate metal electrode with very high work function to form ohmic contact with CdTe, and to avoid Fermi-level pinning of the CdTe rear surface that increases the CdTe/metal interface recombination [139]. Thus, additional back contact materials need inserting between the CdTe absorber and metal electrode to facilitate the hole transport while inhibit the electron transport. These rear contact materials could be CdMgTe with positive conduction band offset (Sections 5.4-5.5), Al₂O₃ with additional fixed negative charge density (Section 5.8), or
heavily $p$-type doped a-Si:H to facilitate the favorable band bending (Sections 5.3, 5.5 and 5.8).

5.3 Direct a-Si:H Contact for Poly-Crystalline CdTe Cells

This part is in collaboration with University of Toledo, Colorado State University (CSU), and First Solar, where poly-crystalline CdTe absorber and CdTe cell fabrication have developed in the last few years. Since the typical poly-crystalline CdTe cells do not include CdMgTe passivating layer during fabrication, we just deposited boron-doped a-Si:H contacts directly on the CdTe absorbers for quick preliminary tests.

Figure 5-3 and Table 5-3 show the results in collaboration with University of Toledo. Compared with the referenced Cu/Au back contact, all the devices with a-Si:H(p) layers have lower $V_{OC}$ and FF values. While the physics mechanism for such poor device performance is under debate, it is clear that a-Si:H(i) layer—responsible for a S-shaped $J$-$V$ curve—is not needed for back contact formation. We suspect the hydrogen in a-Si:H(i) does not passivate the CdTe bulk, which generally requires chlorine passivation instead. Although not good within this experiment, the non-S-shaped $J$-$V$ curve of the a-Si:H(p) or a-SiC:H(p) back contact could be promising to provide higher device performance in the future.
Figure 5-3. Current density - voltage (J-V) characteristics at AM1.5G solar irradiance obtained from the best cells of CdS/CdTe thin film devices when using different back contacts; the respective parameters are provided in Table 5-3. For the device belonging to red curve, Cu/Au was finally deposited and annealed to diffuse Cu; for the rest of the devices, Cu was first deposited onto CdTe, rest of the layers were deposited afterwards—and finally all solar cells were annealed to diffuse Cu into CdTe bulk.

Table 5-3 PV parameters of CdS/CdTe solar cells with different back contacts. The a-Si:H(p), a-SiC:H(p) and a-Si:H(i) layer is 8 nm, 8 nm and 6 nm, respectively. The Cu and Au layer is 3 nm and 50 nm, respectively.

<table>
<thead>
<tr>
<th>Back Contact + Electrode</th>
<th>Voc(V)</th>
<th>Jsc (mA/cm²)</th>
<th>FF (%)</th>
<th>Efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>a-Si:H(p)/Cu/Au</td>
<td>0.530</td>
<td>19.2</td>
<td>50.6</td>
<td>5.1</td>
</tr>
<tr>
<td>Cu/a-Si:H(p)/Au</td>
<td>0.535</td>
<td>20.3</td>
<td>66.8</td>
<td>7.3</td>
</tr>
<tr>
<td>Cu/a-SiC:H(p)/Au</td>
<td>0.508</td>
<td>20.1</td>
<td>65.4</td>
<td>6.7</td>
</tr>
<tr>
<td>Cu/a-Si:H(i)/a-Si:H(p)/Au</td>
<td>0.649</td>
<td>18.5</td>
<td>33.7</td>
<td>4.0</td>
</tr>
<tr>
<td>Cu/Au</td>
<td>0.845</td>
<td>20.0</td>
<td>75.2</td>
<td>12.7</td>
</tr>
</tbody>
</table>

Figure 5-4 shows the results in collaboration with CSU. By adding the a-Si:H(p) layer into the back contact layer stack, the CdTe device performance is degraded with a S-shaped J-V curve. However, a device modeling in Figure 5-5 does not suggest that the valence-band offset of a-Si:H(p) and CdTe could form a hole-blocking barrier. If we agree that the heavily doped a-Si:H(p) layer is favorable to collect holes (rather than block holes),
the issue could be due to the chemical reaction when depositing the a-Si:H(p) layer on the CdTe surface, or the contacting issue at the a-Si:H(p)/Te interface.

Figure 5-4. J-V characteristics of the CdTe solar cells without and with a-Si:H(p) layer. For each of the two device structures, a number of cells were fabricated on the same CdTe glass sample.

Figure 5-5. Simulated band diagram and J-V characteristics without and with a-Si:H(p) layer by using AFORS-HET software [140].
Another experiment with the poly-crystalline CdTe absorbers from First Solar also indicates that depositing a-Si:H(p) contact directly on CdTe absorbers can degrade the device performance on $V_{OC}$ and FF. It also indicates that the poor performance is due to the CdTe/a-Si:H(p) interface, not the a-Si:H(p)/ITO or a-Si:H(p)/metal interface at the rear side.

### 5.4 CdMgTe Passivating Layer for Poly-Crystalline CdTe Cells

After unsuccessful trials by putting a-Si:H(p) contact direct on poly-crystalline CdTe absorbers, we think it is important to add an intermediate CdMgTe passivating layer on the CdTe absorber before implementing the hole-selective a-Si:H(p) contact. Learning from mono-crystalline CdTe cell experience (Section 5.1), we know the high $V_{OC}$ values are attributed to high-quality CdTe absorber, wide-bandgap CdMgTe barriers, and heavily doped $p$-type a-Si:H contact. Therefore, developing a high-quality CdMgTe layer—confining the minority carriers and reduce interface recombination velocity—is essential to gain high $V_{OC}$ for poly-crystalline CdTe cells as well.

The following part of work is in collaboration with First Solar, where I spent three month working on developing CdMgTe electron reflector films (ERF) for poly-crystalline CdTe cells. Detailed processing steps at First Solar are omitted for the intellectual property protection, but the main experimental results are shown as below.
First, we have developed an epitaxially grown, continuous CdMgTe film on poly-crystalline CdTe substrates by MBE. From scanning electron microscope (SEM) imaging, Figure 5-6(a) shows the CdTe/CdMgTe/CdTe layer stack growth is epitaxial as evidenced by the propagating grain and twin boundaries at the growth interface, and Figure 5-6(b) shows that the CdTe/CdMgTe/CdTe layer stack has the right targeted thickness via controlling the ion gauge fluxes of the MBE system. Meanwhile, the ~750-nm-thick CdMgTe layer of the stack is used to get a calibrated Mg ratio from Electron Energy Dispersive Spectroscopy measurement. Even when thinning down to ~50 nm (Figure 5-7), we still get an _epitaxially grown, continuous_ CdMgTe film that is very close to our _targeted thickness_.

Figure 5-6. Cross-sectional SEM images of MBE-grown ~750 nm-thick CdMgTe layer, which is sandwiched between CdTe buffer layer and CdTe cap layer. Schematic structure is shown on the right.
Figure 5-7. Cross-sectional SEM images of MBE-grown ~50 nm-thick CdMgTe layer, which is sandwiched between CdTe buffer layer and CdTe cap layer. Schematic structure is shown on the right.

Then, we have integrated such CdMgTe ERF film on poly-crystalline CdTe cell fabrication process. Many critical parameters have been tested and changed to fit the CdTe/CdMgTe structure, and the standard First Solar back contact is integrated for the device completion.

After many trial-and-error experiments, we fabricated poly-crystalline CdTe solar cells with Cd$_{1-x}$Mg$_x$Te ($x=5$-$20\%$) passivating layers with the standard First Solar back contacts in Figure 5-8. With CdMgTe ERF layers, the cells have higher $V_{OC}$ values (+10-15 mV) than the referenced cells. Meanwhile, higher photoluminescence peak intensities and higher bulk time-resolved photoluminescence (TRPL) lifetimes are also observed in these samples before their cell completion. However, the hole-barrier effect of CdMgTe layers results in lower FF values (<75%), especially at a high Mg ratio, which greatly limits to the maximum value of $V_{OC} \times$FF for high efficiency. Note that this FF degradation mechanism was predicted in a separate publication, which was explained as a combination
of CdTe bulk recombination and the hole barrier of CdMgTe [135]. Overall, the 17.6\%-efficient CdMgTe ERF cell is still inferior to the 18.1\%-efficient standard CdTe cell.

Figure 5-8. Typical $V_{OC}$, FF, $J_{SC}$ and efficiency of CdTe cells without/with a 50-nm-thick CdMgTe ERF layer.

To reveal the cause of FF deficiency in CdMgTe ERF cells, we plotted J-V plots for three representative cells: high Mg ratio, low Mg ratio and FS200 without CdMgTe in Figure 5-9. The light J-V curves clearly show the similar J-V performance in Mg=5\% and FS200, but it becomes a bit S-shaped in Mg=15\%. Looking into the dark log($J$)-V curves, we find that the hole blocking effect starts to impact the J-V curve @ ~670 mV in Mg=15\% and @ ~815 mV in Mg=5\%, compared to FS200 cells. We think the FF deficiency is caused by the valence band blocking of holes that begins at lower voltage with higher Mg ratio in the 50-nm-thick CdMgTe ERF.

To alleviate the hole-barrier effect and increase FF of the CdMgTe ERF cells, we thin down the CdMgTe ERF layer to 25 nm. Also, we test thin CdTe absorbers (1 μm
thinner) in addition to the standard CdTe absorbers to better reveal the effect of CdMgTe ERF stack.

Figure 5-9. Dark/light J-V curves (left) and dark log(J)-V curves (right) for representative cells: one FS200 cell without CdMgTe ERF, and two CdMgTe ERF cells.

Figure 5-10 shows the device performance with and without 25-nm CdMgTe ERF. Similar to the previous result (Figure 5-8), higher Voc are still demonstrated in these solar cells with CdMgTe ERF; Impressively, FFs are 74-76% with thin CdMgTe layer, which leads to 18.6±0.6%-efficient cell (5% Mg ratio) in Figure 5-10. This is the first time that CdMgTe ERF cells are better than standard cells without ERF. The advantage of using CdMgTe ERF—to gain high Voc but maintain similar FF—is clearly seen from this experiment!
Figure 5-10. $V_{OC}$, FF, $J_{SC}$ and efficiency of 2.5-$\mu$m-thick CdTe cells without/with a 25-nm-thick CdMgTe ERF layer. Each symbol represents the average value that are calculated from 10-12 cells on the same glass sample, and the error bars indicate the corresponding standard deviation.

Figure 5-11. $V_{OC}$, FF, $J_{SC}$ and efficiency of 1.5-$\mu$m-thick CdTe cells without/with a 25-nm-thick CdMgTe ERF layer. Each symbol represents the average value that are calculated from 10-12 cells on the same glass sample, and the error bars indicate the corresponding standard deviation.
For the thinner CdTe absorbers, the overall recombination becomes less sensitive to the CdTe bulk rather than the quality of CdTe back contact. Figure 5-11 shows the 1.5-μm-thick CdTe device performance with and without 25-nm CdMgTe ERF. This is the first time that CdMgTe ERF cells could have higher FFs than the non-ERF cells. Clearly, using thin CdTe absorbers can further alleviate the hole-barrier effect of CdMgTe ERF. The optimum device performance is 16.9±0.2%-efficient cell (10% Mg ratio).

In short, adding MBE-grown CdMgTe ERF layer into poly-crystalline CdTe solar cells is definitely beneficial to get high \( V_{OC} \) values, but careful device layer optimization is required to alleviate the hole-blocking effect and achieve high FF values.

5.5 a-Si:H/CdMgTe Contacts for Poly-Crystalline CdTe Cells

With the good-quality, MBE-grown CdMgTe passivating layer developed in Section 5.4, this section discusses the possibility of using a-Si:H(p) layer to form a-Si:H/CdMgTe/CdTe solar cell structure.

Similar to the mono-crystalline CdTe cells with record-high \( V_{OC} \)s, the intermediate wide-bandgap CdMgTe layer can work as the buffer to isolate the defects in the a-Si:H(p) and the poly-CdTe absorber, relieve the interface issue of CdTe/a-Si:H(p) in Section 5.3, and establish a new CdTe/CdMgTe/a-Si:H(p) device structure. Meanwhile, it is desirable that the small CdMgTe processing window (only 5-10% Mg ratio) can be ideally solved by adding a heavily doped a-Si:H(p) contact to reduce the valence band blocking of holes. It is our vision that poly-crystalline CdTe cells with wide-bandgap CdMgTe (for example, 25-40% Mg ratio), coupled with a-Si:H(p) hole-selective contact, could have higher \( V_{OC} \) and FF than standard CdTe cells.
The following part of work is in continuous collaboration with First Solar. The main device structure is shown in Figure 5-12.

Figure 5-12. Schematic passivating and hole contact design for poly-crystalline CdTe solar cell. The a-Si:H/ITO contact is standard for SHJ cells. Others include all the possible contact materials at First Solar. The red and blue arrows show two possible post-deposition treatments—one is CdCl$_2$ treatment, and the other is Cu doping—to improve the CdTe bulk quality and contact formation.

After many experiments, the final device results are not satisfying: the $V_{OC}$ is around 700 mV is for Ag/ITO/a-Si:H/CdMgTe/CdTe solar cell structure, which is much lower than the $V_{OC}$ of the referenced CdTe solar cell structure in Section 5.4 (>800 mV). It is to our surprise that a-Si:H(p) looks rectifying and seems to block holes (see Figure 5-13).
5.6 a-Si:H/CdMgTe Interface Characterization

Comparing the device results in Section 5.1 and Section 5.5, it is very surprising to find that poly-crystalline CdTe cells have quite degraded $V_{OC}$s with the same CdMgTe/a-Si:H/ITO contact. To troubleshoot this issue, we need to analyze the device interface quality from imaging and elemental mapping.

Figure 5-14 shows the cross-sectional transmission electron microscopy (TEM) image of poly-crystalline CdTe cells with CdMgTe/a-Si:H/ITO rear contact. Each layer is quite distinct in the low-magnification TEM image. The high-magnification TEM image shows clear crystal structure of CdTe/CdMgTe and the typical amorphous silicon matrix. Note that TEM is diffraction contrast so it cannot distinguish CdMgTe and CdTe, but it appears to be good epitaxy of CdMgTe on CdTe.

To facilitate the comparison, the cross-sectional TEM image of mono-crystalline CdTe cells with CdMgTe/a-Si:H/ITO is also shown (see Figure 5-15). Clearly, in both
poly- and mono-crystalline CdTe cases, the CdMgTe layer is well epitaxy growth and there is no clear defect formation within the CdMgTe/a-Si:H interface.

Figure 5-14. Cross-sectional TEM image of poly-crystalline CdTe cells.

Figure 5-15. TEM image of mono-crystalline CdTe solar cell with CdMgTe/a-Si/ITO contact [141].
The element mapping is also performed on the poly-crystalline CdTe samples in Figure 5-16. This also looks standard: no inter-diffusion of Si or Cd/Te element at the interface.

![STEM HAADF and EDXS Map](image)

Figure 5-16. Energy-Dispersive X-ray Spectroscopy (EDXS) of CdTe/CdMgTe/a-Si:H interface to map the elements from STEM image. Note that Mg element is hard to detect, probably because it is mixed with the background noise, or it is effused all over the CdTe bulk.

To our knowledge, there is no clear interface issue within the CdMgTe/a-Si:H in the poly-crystalline CdTe solar cells.

5.7 SCAPS-1D Simulation of Poly-Crystalline CdTe Cells

Different device results in Section 5.1 and Section 5.5 are puzzling us: what is the root cause of low \( V_{OC} \) and FF in poly-crystalline CdTe cells with the same CdMgTe/a-Si:H/ITO contact? Here we use SCAPS-1D device simulation software [142] to find some clues. Note that the effects of poly-crystalline grain boundary defects are substituted by lowering the CdTe bulk lifetime in the simulation.

Firstly, we try to study the function of CdMgTe ERF using a similar device structure that CSU has developed [135] (See Figure 5-17). Note that the front and rear contacts are not identical to what First Solar has used in Section 5.4.
Figure 5-17. CdTe solar cell layer structure in SCAPS-1D. The left one is CSU’s baseline device structure without CdMgTe, and the right one is with CdMgTe into the device.

Table 5-4 PV parameters of simulated 2.5-μm-thick CdTe solar cells by adding CdMgTe ERF layer: no CdMgTe, 50-nm-thick CdMgTe and 25-nm-thick CdMgTe. The bandgap of CdMgTe is 1.8 eV (~15% Mg ratio in the film). Ni is used as the rear metal electrode in the simulation.

<table>
<thead>
<tr>
<th>ERF in Back Contact</th>
<th>Voc (V)</th>
<th>Jsc (mA/cm²)</th>
<th>FF (%)</th>
<th>Efficiency (%)</th>
</tr>
</thead>
<tbody>
<tr>
<td>no</td>
<td>0.874</td>
<td>27.2</td>
<td>83.1</td>
<td>19.8</td>
</tr>
<tr>
<td>50-nm-thick CdMgTe</td>
<td>0.981</td>
<td>27.3</td>
<td>75.0</td>
<td>20.1</td>
</tr>
<tr>
<td>25-nm-thick CdMgTe</td>
<td>0.966</td>
<td>27.3</td>
<td>76.4</td>
<td>20.1</td>
</tr>
</tbody>
</table>

Table 5-4 shows the simulated CdTe solar cell performance without and with CdMgTe ERF layer. Adding 50-nm-thick CdMgTe can increase the Voc but decrease the FF, which corresponds to the trend in Figure 5-8; thinning down the CdMgTe layer to 25 nm can increase the FF but decrease the Voc slightly, which corresponds to the trend in Figure 5-10. If we have detailed front and rear contacts information, the SCAPS-1D simulation can explain and even match the experimental results in Section 5.4.

Secondly, since the Voc of poly-crystalline CdTe cells with a-Si:H (Section 5.3) or with CdMgTe/a-Si:H (Section 5.5) is quite low, we want to know what rear layer
parameters can play big roles to decrease the $V_{OC}$ and FF of CdTe. Here we use the typical CSU’s baseline device structure (SnO/MZO/CdTe/Te/Metal) as the starting point.

For the CdTe absorber, the bandgap, electron affinity, lifetime, thickness and doping density have impact on the final device; however, we always used the same CdTe absorbers (First Solar, CSU, or Toledo) and we do not think low-temperature a-Si:H deposition and ITO/Ag processing can change the CdTe bulk quality. For the Te or any other possible hole-selective materials, we find the bandgap and electron affinity play the major roles to change the $V_{OC}$ and FF while thickness and doping have some minor impact. For the metal electrode, we find the work function plays the major role to determine the highest achievable $V_{OC}$ and FF, as expected. Indeed, Song et al. also mentioned that the importance of the valence band maximum (i.e. the total value of electron affinity and bandgap in hole-selective contact) and the work function of metal electrode to define the highest achievable $V_{OC}$ [135].

Table 5-5 PV parameters of simulated 2.5-μm-thick CdTe solar cells with different back contacts. The bandgap of 25-nm-thick CdMgTe is 1.8 eV (~15% Mg ratio in the film). The ITO work function is set between 4.7 eV and 5.0 eV.

<table>
<thead>
<tr>
<th>Back Contacts</th>
<th>$V_{OC}$ (V)</th>
<th>$FF$ (%)</th>
<th>Fabricated?</th>
</tr>
</thead>
<tbody>
<tr>
<td>CdMgTe/a-Si/ITO$_{MIN}$</td>
<td>0.833</td>
<td>57.8</td>
<td>Yes, Figure 5-13</td>
</tr>
<tr>
<td>CdMgTe/a-Si/ITO$_{MAX}$</td>
<td>1.043</td>
<td>67.0</td>
<td></td>
</tr>
<tr>
<td>CdMgTe/a-Si/Ni</td>
<td>1.049</td>
<td>68.1</td>
<td>No, for reference only</td>
</tr>
<tr>
<td>a-Si/ITO$_{MIN}$</td>
<td>0.854</td>
<td>64.2</td>
<td>Yes, Figure 5-13</td>
</tr>
<tr>
<td>a-Si/ITO$_{MAX}$</td>
<td>1.053</td>
<td>73.0</td>
<td></td>
</tr>
<tr>
<td>a-Si/Ni</td>
<td>1.054</td>
<td>73.8</td>
<td>No, for reference only</td>
</tr>
<tr>
<td>CdMgTe/ITO$_{MIN}$</td>
<td>0.253</td>
<td>58.7</td>
<td>No, for reference only</td>
</tr>
<tr>
<td>CdMgTe/ITO$_{MAX}$</td>
<td>0.553</td>
<td>69.8</td>
<td>No, for reference only</td>
</tr>
<tr>
<td>ITO$_{MIN}$</td>
<td>0.179</td>
<td>56.2</td>
<td>Yes, Figure 5-13</td>
</tr>
<tr>
<td>ITO$_{MAX}$</td>
<td>0.479</td>
<td>75.0</td>
<td></td>
</tr>
</tbody>
</table>

Thirdly, for $p$-type a-S:H layer that typically have electron affinity of 3.8–3.9 eV and bandgap of 1.7–1.8 eV, we think it can work as an effective hole-selective contact, coupled
with high work-function metal or semi-metal electrode (Ni=5.2 eV, ITO=4.7–5.0 eV). By adding 25-nm-thick a-Si:H layer into the CdTe device, Table 5-5 shows all the simulated results from SCAPS-1D software. Clearly, adding a-Si layer into the back contact structure improves the device \( V_{OC} \) in the simulation. However, this simulated \( V_{OC} \) improvement do not match the experimental results of the fabricated poly-crystalline CdTe cells. While the mismatch could be related to a-Si layer or CdMgTe/a-Si interface, further convincing clues are needed to understand this puzzling conflict (a possible explanation is shown in APPENDIX C).

5.8 a-Si:H/Al\(_2\)O\(_3\) Contacts for Poly-Crystalline CdTe Cells

While we faced some practical challenges for using CdMgTe and a-Si:H back contacts in poly-crystalline CdTe cells, another alternative opportunity of back contact comes to our mind: Al\(_2\)O\(_3\) and a-Si:H back contacts. This part is in collaboration with CSU.

Al\(_2\)O\(_3\) is known to have negative fixed charges that can repel electrons and reduce surface recombination for silicon [143], Cu(In, Ga)Se\(_2\) [144] and Cu\(_2\)ZnSnS\(_4\) [145] solar cells. Recently, CSU demonstrated thin Al\(_2\)O\(_3\) layer also passivates the poly-crystalline \( p \)-type CdTe rear surface, leading to very high PL intensity and improved TRPL lifetimes [146]. However, the Al\(_2\)O\(_3\) passivation does not results into high device \( V_{OC} \) using CSU’s baseline Te rear contact.

At ASU, we tested \( p \)-type a-Si:H hole-selective contact for the samples from CSU. Before the a-Si:H and/or ITO deposition, we first used ellipsometry to measure and fit the Al\(_2\)O\(_3\) thickness on two referenced glasses in Figure 5-18. It shows uniform Al\(_2\)O\(_3\) film
across 36 cm² area. The thickness is 1.16±0.34 nm and 1.18±0.31 nm for A004 and A031 sample, respectively. It indicates that the day-to-day thickness variance is quite negligible.

Figure 5-18. Al₂O₃ thickness mapping. Targeted for 2 nm, the Al₂O₃ film was processed in two different days.

We tested and integrated the a-Si:H and/or ITO deposition into the complete polycrystalline CdTe solar cell fabrication (see Table 5-6). It should be noted that CdCl₂ and CuCl treatments are important to gain the optimized device performance. The schematic CdTe device structures are shown in Figure 5-19.

Table 5-6 CdTe device structures used in experiments. CdCl₂ and CuCl are processing treatments, not actual layers.

<table>
<thead>
<tr>
<th>Sample</th>
<th>Layer and Process Information</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>TEC10/MZO/CdSeTe/CdTe/Al₂O₃/CdCl₂/CuCl/a-Si:H/metal</td>
</tr>
<tr>
<td>2</td>
<td>TEC10/MZO/CdSeTe/CdTe/Al₂O₃/a-Si:H/CdCl₂/CuCl/metal</td>
</tr>
<tr>
<td>3</td>
<td>TEC10/MZO/CdSeTe/CdTe/Al₂O₃/CdCl₂/a-Si:H/CdCl₂/CuCl/metal</td>
</tr>
<tr>
<td>4</td>
<td>TEC10/MZO/CdSeTe/CdTe/Al₂O₃/CdCl₂/a-Si:H/CuCl/ITO</td>
</tr>
<tr>
<td>5</td>
<td>TEC10/MZO/CdSeTe/CdTe/Al₂O₃/a-Si:H/CdCl₂/CuCl/ITO</td>
</tr>
<tr>
<td>6</td>
<td>TEC10/MZO/CdSeTe/CdTe/Al₂O₃/CdCl₂/a-Si:H/CdCl₂/CuCl/ITO</td>
</tr>
<tr>
<td>7</td>
<td>TEC10/MZO/CdSeTe/CdTe/Al₂O₃/a-Si:H/ITO/CdCl₂/CuCl/metal</td>
</tr>
<tr>
<td>8</td>
<td>TEC10/MZO/CdSeTe/CdTe/Al₂O₃/a-Si:H/ITO/CdCl₂/CuCl</td>
</tr>
<tr>
<td>9</td>
<td>TEC10/MZO/CdSeTe/CdTe/CdCl₂/CuCl/Te/metal</td>
</tr>
<tr>
<td>10</td>
<td>TEC10/MZO/CdSeTe/CdTe/Al₂O₃/CdCl₂/CuCl/metal</td>
</tr>
</tbody>
</table>
Figure 5-19. Schematic poly-crystalline CdTe cells with 5 different back contact designs. The Al₂O₃ layer is 2 nm, and a-Si:H(p) layer is 8 nm.

Figure 5-20. Representative I-V curves of poly-crystalline CdTe cells with different back contacts. The Al₂O₃ layer is 2 nm, and a-Si:H(p) layer is 8 nm. The V_{OC} increases from 750–760 mV to 805–815 mV by adding a-S:H layer.

Figure 5-20 shows the typical I-V curves of CdTe cells with the first three different back contacts, depicted in Figure 5-19. Clearly, adding a-Si:H film after Al₂O₃ passivating layer can increase the device V_{OC}, which proves the expected hole-selectivity of p-type a-Si:H layer. The absolute voltage gain here is ~50 mV. With this encourage first experiment,
further processing optimization on Al$_2$O$_3$/a-Si:H/metal device structure could lead to better device performance.

Figure 5-21 shows the typical I-V curves of CdTe cells with the last three different back contacts, depicted in Figure 5-19. While adding the ITO into the device structure may degrade the $V_{OC}$ (again, it need more experiments to confirm), the Al$_2$O$_3$/a-Si:H/ITO/metal device structure has the highest efficiency of all the 5 back contact designs. Interestingly, the Al$_2$O$_3$/a-Si:H/ITO device structure has decent $V_{OC}$ and FF. Without metal electrode layer, this design is promising to work as the rear transparent hole contact/electrode of poly-crystalline CdTe cells, solving the big hurdle for 4-terminal CdTe/Si tandem cell development. Similarly, further processing optimization on Al$_2$O$_3$/a-Si:H/ITO device structure could lead to better device performance.

![Figure 5-21. Representative I-V curves of poly-crystalline CdTe cells with Al$_2$O$_3$/a-Si:H back contacts. The Al$_2$O$_3$ layer is 2 nm, and a-Si:H(p) layer is 8 nm.](image)

5.9 Summary

The $p$-type a-Si:H hole-selective contact layer is one important element to achieve $>1.1$ V $V_{OC}$ for mono-crystalline CdTe cells with wide-bandgap CdMgTe barrier layers.
The $p$-type a-Si:H is also by far the optimum hole-selective contact material for mono-crystalline CdTe cells to gain the maximum $V_{OC}$ and FF. For the industry-preferred poly-crystalline CdTe cells, the development of good-quality CdMgTe passivating layer on the poly-crystalline CdTe substrates enables a broad study on a-Si:H and other various hole-selective contact materials. However, it is very challenging to integrate $p$-type a-Si:H layer into commercial-grade poly-crystalline CdTe cells for $V_{OC}$ and FF enhancement. To explain this puzzling performance difference between mono-crystalline and poly-crystalline CdTe cell with CdMgTe/a-Si:H contacts, we still need more evidence in addition to the a-Si:H/CdMgTe interface imaging and the SCAPS-1D device simulation.

Another back contact formation on poly-crystalline CdTe cells is using Al$_2$O$_3$ and a-Si:H layers, in which promising $V_{OC}$ enhancement is demonstrated. In this structure, Al$_2$O$_3$ exhibits negative fixed charge to passivate the CdTe surface and $p$-type a-Si:H layer works as hole-selective contact to gain higher $V_{OC}$ and decent FF. Interestingly, a Al$_2$O$_3$/a-Si:H/ITO back contact structure enables decent CdTe device performance. This structure can work as the rear transparent hole contact/electrode of poly-crystalline CdTe cells, solving the big hurdle for 4-terminal CdTe/Si tandem cell development.
CHAPTER 6

CONCLUSION AND OUTLOOK

6.1 Conclusion

This work focuses on using the promising a-Si:H contacts for silicon and cadmium telluride (CdTe) solar cells, two important cell technologies in today and future’s PV market. Essentially, passivating and carrier-selective a-Si:H contacts are investigated to gain high device $V_{OC}$ and FF for the PV absorbers.

First, we have increased the hydrogen content of the a-Si:H(i) layer by an in-situ hydrogen plasma treatment, and then applied this modified a-Si:H(i) layer into classical $n$-type SHJ cell structure to increase the device performance. The hydrogen plasma treatment also increases the SHJ solar cell temperature-processing window, which is good for the future advanced or tandem device development. By studying the hydrogen plasma etching and damaging effect, a SiO$_x$ capping layer can be used to alleviate such undesirable effect. Hydrogen plasma treatment is further applied on SHJ precursor with intrinsic and doped a-Si:H layers, and even on the pseudo SHJ solar cells with ITO or IZO layers, but the results are only beneficial for fundamental research rather than improving device performance directly.

Second, we have demonstrated that a-Si:H contact—without any thickness change from standard full-spectrum $n$-type SHJ solar cells—can perfectly apply to make good IR-spectrum silicon solar cells. It is found that the a-Si:H thickness variance lead to narrower efficiency distribution and identical current values in IR-spectrum application than in full-
spectrum application, by a factor of 3 to 4, according to the statistic modeling quantifying the SHJ cell efficiency distribution. Meanwhile, relieving large-area PECVD film uniformity requirement is important for the state-of-the-art SHJ solar cell fabrication and for the future silicon-based tandem cell and module fabrication.

Third, the a-Si:H contacts are applied to commercial-grade $p$-type Si cells, which have much lower bulk carrier lifetimes than the $n$-type Si cells. We have used gettering and bulk hydrogenation to improve the $p$-type Si bulk quality, and then applied a-Si:H contacts to enable excellent surface passivation and carrier transport for solar cell fabrication. With additional high-intensity laser treatment, this leads to an open-circuit voltage of 707 mV, the second highest value ever reported for $p$-type Czochralski silicon cells, and of 702 mV, the world-record open-circuit voltage in $p$-type multi-crystalline silicon cells.

Finally, we have discussed that the major differences between mono-crystalline and poly-crystalline CdTe solar cells. In both cases, a good-quality CdMgTe passivating layer is inserted between the CdTe bulk and a-Si:H contact layer to reduce interface recombination. While $p$-type a-Si:H layer is by far the best hole-selective contact material in mono-crystalline CdTe cells, it is quite challenging to add such $p$-type a-Si:H layer into commercial-grade poly-crystalline CdTe cells to get satisfactory $V_{OC}$. However, if Al$_2$O$_3$ passivating layers are used, the follow-up a-Si:H hole-selective contact becomes promising for poly-crystalline CdTe device integration. The Al$_2$O$_3$ and a-Si:H back contacts lead to $V_{OC}$ improvement, and they can also work as the rear transparent hole contact/electrode of poly-crystalline CdTe cells.

6.2 Outlook
For Chapter 2, hydrogen chemical passivation is always the research topic in the field of silicon solar cells. As one post-deposition method, hydrogen plasma treatment is well studied in various aspects of n-type SHJ cell fabrication process. One possible continuous research thrust is to understand the hydrogen movement and its interaction for other types of passivating contact materials (e.g. a-SiN$_x$:H, a-SiO$_x$:H, a-SiC$_x$:H, Al$_2$O$_3$), and for passivating bilayers of a-Si:H/SiN$_x$:H [147], [148], complex layer stack [149] and other emerging materials (e.g. Nb$_2$B$_5$ [150], [151]).

For Chapter 3, the identical current density and narrow efficiency distribution within a wide a-Si:H thickness range could essentially make SHJ IR-spectrum cells attractive to PV industry. While IR-transparent front TCO and IR-reflective rear reflector can further enhance the IR response of SHJ cells, the continuous promising research thrust here is to choose a top cell candidate to couple with a SHJ bottom cell as the silicon-based tandem cell, and then integrate several cells for a tandem module demonstration. It is important to compare a real silicon-based tandem module with the standard SHJ full-spectrum module to validate the wide processing window of a-Si:H films.

For Chapter 4, a-Si:H contacts on p-type mono- and multi-crystalline silicon wafers that have been pre-gettered and pre-hydrogenated enable very high device $V_{OC}$, indicating good bulk and surface passivation quality. The continuous promising research thrust is to improve the FFs of these p-type SHJ solar cells. Improving the p-type c-Si bulk quality, optimizing a-Si:H layer property, and eventually using contact resistivity metrology [99] to guide the device architecture design are advisable. Enhancing $J_{SC}$ is the final step to develop high-efficiency p-type SHJ cells, which in theory is quite similar to rear-emitter n-type SHJ cell structure (i.e. with a-Si:H (i/n) on the front side). If the surface texturing
hinders multi-crystalline silicon wafers from achieving conformal a-Si:H film deposition, polydimethylsiloxane (PDMS) scattering layer can be used to increase the $J_{SC}$ of any solar cell with flat surface structure [116].

For Chapter 5, using electron reflector film at the rear side of poly-crystalline CdTe cells is a good way to transport the holes while block the electrons. Wide bandgap CdMgTe and Al$_2$O$_3$ films are two examples that could fulfil this function. For CdMgTe film, it is important to unveil the puzzling performance difference between mono-crystalline and poly-crystalline CdTe cell with CdMgTe/a-Si:H contacts. For Al$_2$O$_3$ film, the promising research thrust is to realize a high $V_{OC}$ and FF potential by detailed process optimizations for transparent Al$_2$O$_3$/a-Si:H contacts. Note that poly-crystalline CdTe cells typically need chlorine passivation treatment (e.g. CdCl$_2$ or MgCl$_2$ [152]), as well as Cu doping process and post-fabrication treatment. Complex process-related challenges are worth investigating before summarizing a conclusion for Al$_2$O$_3$/a-Si:H contacts. For example, it seems $p$-type a-Si:H still works well as hole-selective contact even after annealing at ~420 °C. If all goes well, the Al$_2$O$_3$/a-Si:H contacts can be promising for poly-crystalline CdTe solar cells and for future CdTe/Si tandem cell development. Interestingly, the Al$_2$O$_3$/a-Si:H hole-selective contacts may be also tested on other PV absorbers, like silicon, perovskite, copper indium gallium selenide (CIGS), and copper zinc tin sulfide (CZTS).

In addition to silicon and CdTe as PV absorbers, a separate set of experiments were performed on $n$-type indium phosphide (InP) wafer with a-Si:H contact. Some preliminary experiments have shown that a-SiC:H(i)/a-Si(p) contact on InP could lead to $V_{OC}$ of 675 mV after device integration (see APPENDIX D), but $n$-type InP wafer surface treatment and the contact formation need further investigation to achieve >750 mV, a comparable
$V_{OC}$ value to 785 mV in $p$-type InP wafer with electron-selective TiO$_2$ contact [153]. Nevertheless, integrating a-Si:H contacts into other emerging PV absorbers can be a high-risk but high-gain research thrust.
REFERENCES


vol. 119, no. 4, p. 507, 1972.


[56] D. L. Staebler and C. R. Wronski, “Reversible conductivity changes in discharge-


Heterojunction Carrier Collectors,” Arizona State University, 2013.


S. Essig et al., “Raising the one-sun conversion efficiency of III-V/Si solar cells to 32.8% for two junctions and 35.9% for three junctions,” *Nat. Energy*, vol. 2, no. 9, 2017.


A. Abdallah et al., “Towards an optimum silicon heterojunction solar cell


[153] X. Yin et al., “19.2% Efficient InP Heterojunction Solar Cell with Electron-


APPENDIX A

P-5000 PECVD SPECIFICATIONS
P-5000 PECVD SPECIFICATIONS

**Safety:** gas leak detectors

**SPC:** film uniformity (chambers), leak-up rate (chambers and loadlock), lamp (chambers)

**Clean and Condition:** NF₃+N₂ and SiNx coating

- **Temperature:** Typically 200-350 °C. The physical limit is 100 - 400 °C.
- **Pressure:** Typically 2.5 - 3.5 T. Below 0.8 Torr is hard to control the plasma.
- **Power:** Typically 30-100 W. The power supply is 1250 W.
- **Interelectrode gap:** Typically 392 mil for the actual gap. The uniformity could degrade substantially in either direction (parabolic curve).

- **Gas flows:**
  - SiH₄: silane
  - NH₃: ammonia
  - H₂
  - N₂
  - O₂
  - N₂O: nitrous oxide
  - CH₄: methane
  - PH₃: phosphine
  - B(CH₃)₃: TMB, trimethylborane

\[
\begin{align*}
\text{SiN}x & \rightarrow \text{SiH}_4 + \text{NH}_3 + \text{H}_2 \text{ or N}_2 \\
\text{SiO}x & \rightarrow \text{SiH}_4 + \text{N}_2\text{O} + \text{N}_2 \\
a-\text{Si:H(i)} & \rightarrow \text{SiH}_4 + \text{H}_2 \\
a-\text{Si:H(n)} & \rightarrow \text{SiH}_4 + \text{H}_2 + \text{PH}_3 \\
a-\text{Si:H(p)} & \rightarrow \text{SiH}_4 + \text{H}_2 + \text{B}[\text{CH}_3]_3 \\
a-\text{Si:C:H(i)} & \rightarrow \text{SiH}_4 + \text{H}_2 + \text{CH}_4 \\
a-\text{Si:C:H(p)} & \rightarrow \text{SiH}_4 + \text{H}_2 + \text{B}[\text{CH}_3]_3 + \text{CH}_4 \\
\text{H}_2 \text{ plasma} & \rightarrow \text{H}_2 
\end{align*}
\]
APPENDIX B

SUPPLEMENTARY: H₂ PLASMA TREATMENT ON A-SI:H(I)
H2 PLASMA TREATMENT ON A-Si:H(I)

Essentially, hydrogen plasma treatment dissociate molecular hydrogen into atomic hydrogen, which have three effects on the underlying a-Si:H/c-Si materials: 1) etch a-Si:H film (undesirable if the a-Si:H is over-etched); 2) increase the Si-H bond density of a-Si:H film (i.e. hydrogen insertion); 3) decrease the dangling bond density of a-Si:H/c-Si interface (good for passivation). In terms of intrinsic a-Si:H passivation on c-Si substrates, a design of experiment (DOE) can be used to find the optimum H2 plasma treatment recipe.

By studying the temperature, power, time pressure, hydrogen gas flow of the post-deposition hydrogenation treatment (Table B1) on the effective minority carrier lifetimes of a-Si:H/c-Si samples, we find the H2 plasma treatment temperature is the most important parameter to impact the lifetime value in Figure B1.

Table B1. Factors assignment and level setting

<table>
<thead>
<tr>
<th>Factors</th>
<th>Low level setting (-)</th>
<th>High level setting (+)</th>
</tr>
</thead>
<tbody>
<tr>
<td>X1 Temperature</td>
<td>200 °C</td>
<td>350 °C</td>
</tr>
<tr>
<td>X2 RF Power</td>
<td>30 W</td>
<td>180 W</td>
</tr>
<tr>
<td>X3 Time</td>
<td>15 s</td>
<td>60 s</td>
</tr>
<tr>
<td>X4 Pressure</td>
<td>0.5 Torr</td>
<td>5 Torr</td>
</tr>
<tr>
<td>X5 H2 gas flow</td>
<td>200 sccm</td>
<td>800 sccm</td>
</tr>
</tbody>
</table>

FIG B1. Design matrix in JMP software – screen of lifetime after the H2 plasma treatment. (Acknowledgement: Jason Yu conducted the data analysis).
In a separate experiment (Figure B2), we find that 300 °C is the optimum recipe. From 250 °C to 300 °C, the hydrogen-etching rate is decreased but the hydrogen insertion is enhanced. At 350 °C, it is inferred that hydrogen effusion from the a-Si:H film competes with hydrogen insertion into the a-Si:H film, which could explain the low lifetime value. However, since the a-Si:H deposition is typically at 250 °C and ramping up the chamber temperature takes lots of time, we still use 250 °C in the typical H₂ plasma treatment for solar cell fabrication.

![Graph showing lifetime at different H₂ plasma temperatures](image)

**FIG B2.** Effective minority carrier lifetime of a textured c-Si wafer with a-Si:H(i) symmetrical layers on both sides. After 10-nm-thick a-Si:H(i) film deposition, the full-size wafer was cut into 4 pieces, which represent 4 symbols with or without temperature-varied H₂ plasma treatment. All the other H₂ plasma treatment parameters were identical.

Another interesting experiment is that we want to find if H₂ plasma treatment during the a-Si:H(i) growth can lead to better surface passivation for c-Si wafers. Figure B3 shows we used several wafers to verify our assumption. Clearly, the best passivation belongs to the old way: a-Si:H growth first, and post-deposition H₂ plasma treatment afterwards. Besides, the lower lifetime when interrupting the a-Si:H growth at 2 nm indicates the potential hydrogen plasma damage to c-Si substrate, when the underlying a-Si:H(i) is quite thin. The hydrogen plasma damage is also discussed in Section 2.4.
FIG B3. Effective minority carrier lifetime of a textured c-Si wafer with a-Si:H(i) that was treated with H₂ plasma during the a-Si:H layer growth. For H₂ plasma treatment at 2, 4, 6 and 8 nm, the sequence is initial a-Si:H(i) film growth, the H₂ plasma treatment interruption and final a-Si:H(i) film growth. For H₂ plasma treatment at 10 nm, it is the typical a-Si:H(i) growth first and H₂ plasma treatment afterwards. Only the front side of the c-Si wafer was treated by H₂ plasma.
APPENDIX C

POSSIBLE EXPLANATION: A-SI:H CONTACT IN CDTE CELLS
POSSIBLE EXPLANATION: A-Si:H CONTACT IN CDTE CELLS

In Chapter 5, we have applied a-Si:H(p) layer into CdTe solar cells. With CdMgTe passivating layer, it is surprising that adding the boron-doped a-Si:H(p) layer led to poor poly-crystalline CdTe device performance, which is completely different from the mono-crystalline CdTe case. Replacing the CdMgTe layer by thin Al₂O₃ passivating layer, we find the boron-doped a-Si:H(p) became beneficial and promising in the poly-crystalline CdTe device structure.

Here we propose a possible explanation for the observed phenomena in Table C1.

<table>
<thead>
<tr>
<th>Absorber</th>
<th>Pre-treatment</th>
<th>Stack</th>
<th>( V_{OC} ) and FF</th>
</tr>
</thead>
<tbody>
<tr>
<td>Mono-CdTe</td>
<td>-</td>
<td>CdMgTe/a-Si</td>
<td>&gt;1V and &gt;72%</td>
</tr>
<tr>
<td>Poly-CdTe</td>
<td>-</td>
<td>-</td>
<td>800 mV and 75%</td>
</tr>
<tr>
<td>Poly-CdTe</td>
<td>-</td>
<td>a-Si</td>
<td>Degradation (-)</td>
</tr>
<tr>
<td>Poly-CdTe</td>
<td>-</td>
<td>H₂ plasma</td>
<td>800 mV and 75%</td>
</tr>
<tr>
<td>Poly-CdTe</td>
<td>HCl</td>
<td>a-Si</td>
<td>Worse degradation (---)</td>
</tr>
<tr>
<td>Poly-CdTe</td>
<td>-</td>
<td>CdMgTe/a-Si</td>
<td>Slight degradation (-)</td>
</tr>
<tr>
<td>Poly-CdTe</td>
<td>-</td>
<td>Al₂O₃/a-Si</td>
<td>&gt;800 mV</td>
</tr>
</tbody>
</table>

In the initial case of mono-crystalline CdTe with CdMgTe/a-Si contact, the CdTe absorber is In-doped, \( n \)-type material without grain boundaries and Cl-free.

\[
\text{SiH₄+H₂+ B[CH₃]₃} \rightarrow \text{a-Si:H(p)} \quad \text{(with RF plasma in PECVD)} \tag{C.1}
\]

In the case of poly-crystalline CdTe with a-Si contact, the CdTe absorber is \( p \)-type with grain boundaries (GB) and lots of Cl for bulk passivation. It is known that \( p \)-type a-Si:H is doped with boron (B), which could form B-Cl or B-GB reaction within CdTe near surface (note that B is \( n \)-type dopant for CdTe) that negatively impact the device performance. Indeed, applying only H₂ plasma treatment (no SiH₄, no B[CH₃]₃) does not affect the device performance; preparing an oxide-free CdTe surface (HCl pre-treatment) followed by the a-Si:H deposition intensified the device degradation.

In the case of poly-crystalline CdTe with CdMgTe/a-Si contact, the intermediate wide-bandgap CdMgTe is still poly-crystalline. Similarly, the GB and Cl are still there. While the device degradation is slightly alleviated, the \( V_{OC} \) and FF of devices with CdMgTe/a-Si are still inferior to those with CdMgTe only.

In the final case of poly-crystalline CdTe with Al₂O₃/a-Si contact, the intermediate wide-bandgap Al₂O₃ may work as a barrier layer to avoid the possible B-Cl and B-GB reaction. Thus, this contact strategy led to improved \( V_{OC} (>800 \text{ mV}) \), even the condition is not fully optimized.
In short, the possible B-Cl or B-GB reaction within poly-crystalline CdTe near surface may be the reason to explain the different device performance. Even if the B does not compensate the effective $p$-type doping of CdTe absorber, this reaction may reduce the effective $p$-type doping of a-Si layer itself, making undesirable band bending for hole selectivity at the rear contact.
APPENDIX D

A-SI:H IN INDIUM PHOSPHIDE SOLAR CELLS
Indium phosphide (InP) is a direct-bandgap material, making it useful for optoelectronic devices. The bandgap of 1.34 eV is close to the optimum value for one-sun PV application. It has low very low surface recombination velocity even without any passivation [154]–[156]. The surface recombination can even be lower than gallium arsenide (GaAs) [154], [155], in which the highest 28.8%-efficient cell has been ever made [6]. By comparison, the highest InP solar cell has achieve 24.2%-efficient by NREL [6]. In addition, the InP solar cell has superior radiation resistance compared to Si and GaAs solar cells [59], [157], [158], making it very attractive for space application.

Developing high-efficiency InP solar cell was a hot research topic from 1976 to 1995, and since then very few papers were reported on this topic. The reason could be its high cost: most of the InP solar cells used homojunction technology, in which expensive tools like MBE and metal-organic chemical vapor deposition (MOCVD) were used to develop high-performance solar cells. During the past 20 years, the other solar cell technologies like Si, thin film, and GaAs cells, advanced much faster.

Recently, researchers at University of California, Berkeley (UCB) developed a 19.2%-efficient p-type InP solar cell (V_{OC}=785 mV) using electron-selective TiO_2 contact [159]. Such simple TiO_2/InP heterojunction solar cell lowers the solar cell fabrication cost and could activate the interests for InP solar cells. In addition, most of the existing InP solar cells used p-type wafers, rather than n-type wafers. If low-cost heterojunction n-type InP solar cells can be fabricated with good performance, it will pioneer a new field for the PV research community.

As a first step, we are trying to demonstrate high V_{OC} of n-type InP devices using varied hole-selective contact materials. All the experiments here are in collaboration with James Bullock at UCB.

FIG D1. Schematic of InP solar cell.
Figure D1 shows the general structure of $n$-type InP solar cells. We used $n$-type, S-doped mono-crystalline InP wafers (450±25 μm) from AXT. Wafers were typically cleaned in HCl:H$_2$O solution and then put into PECVD chambers. Note that many other acid preclean methods were also tested. The wafers could be treated (or not treated) by NH$_3$, CH$_4$, or PH$_3$ plasma before the a-SiC:H(i)/a-Si:H(p) layer stack deposition. Removing the wafers from PECVD, additional ITO and/or MoO$_x$ layer(s) were formed on top of the passivating and hole-selective a-Si:H layers. On the rear side, the wafers were sputtered with ITO layer and/or evaporated with metal electrode.

We made 9 batches of experiments, varying the wafer pretreatments, front-side a-Si:H contacting layers, front-side ITO/MoO$_x$ layers, and rear-side layers (see Figure D2). To achieve high $V_{OC}$, the two main factors are wafer acid cleaning and a-SiC:H(i)/a-Si:H(p) layer stack. The highest $V_{OC}$ is 675 mV so far. Better ideas on pushing it beyond 750 mV, likely from surface treatment or hole-selective contacting layer formation, are required to use InP(n) wafers for high-efficiency solar cell fabrication.

<table>
<thead>
<tr>
<th>Wafer: InP (n)</th>
<th>Effect</th>
</tr>
</thead>
<tbody>
<tr>
<td>Doping</td>
<td>No clear trend</td>
</tr>
<tr>
<td>Different pre clean by acid</td>
<td>Yes</td>
</tr>
<tr>
<td>Rinsing after acid</td>
<td>Yes</td>
</tr>
<tr>
<td>NH$_3$ plasma before deposition</td>
<td>only NH$_3$ @200°C works a bit</td>
</tr>
<tr>
<td>CH$_4$ plasma before deposition</td>
<td>Negative</td>
</tr>
<tr>
<td>PH$_3$ plasma on thin a-Si(n) layer</td>
<td>No effect</td>
</tr>
<tr>
<td>Passivating Layer: a-Si or a-SiC (i)</td>
<td>Improved if thicker</td>
</tr>
<tr>
<td>Thickness</td>
<td>a-SiC is better than a-Si</td>
</tr>
<tr>
<td>C% in a-SiC:H (i) plays a role</td>
<td>Almost no effect, 50% is good</td>
</tr>
<tr>
<td>H$_2$ plasma</td>
<td>No effect</td>
</tr>
<tr>
<td>Selective Layer: a-Si (p)</td>
<td>Slight difference if thicker</td>
</tr>
<tr>
<td>Thickness</td>
<td>H$_2$ plasma</td>
</tr>
<tr>
<td>MoO$_x$ and ITO</td>
<td>MoO$_x$ to replace a-Si (p)?</td>
</tr>
<tr>
<td>MoO$_x$ to help a-Si (p)?</td>
<td>Almost no effect</td>
</tr>
</tbody>
</table>

**FIG D2.** $n$-type InP solar cell with a-Si:H contacts: process variance and its effect on $V_{OC}$. 