Development of Radiation Hardened High Voltage Super-Junction Power MOSFET

by

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ABSTRACT

In recent years, the Silicon Super-Junction (SJ) power metal-oxide semiconductor field-effect transistor (MOSFET), has garnered significant interest from spacecraft designers. This is due to their high breakdown voltage and low specific on-state resistance characteristics. Most of the previous research work on power MOSFETS for space applications concentrated on improving the radiation tolerance of low to medium voltage (~ 300V) power MOSFETs. Therefore, understanding and improving the reliability of high voltage SJMOS for the harsh space radiation environment is an important endeavor.

In this work, a 600V commercially available silicon planar gate SJMOS is used to study the SJ technology’s tolerance against total ionizing dose (TID) and destructive single event effects (SEE), such as, single event burnout (SEB) and single event gate rupture (SEGR). A technology computer aided design (TCAD) software tool is used to design the SJMOS and simulate its electrical characteristics.

Electrical characterization of SJMOS devices showed substantial decrease in threshold voltage and increase in leakage current due to TID. Therefore, as a solution to improve the TID tolerance, metal-nitride-oxide-semiconductor (MNOS) capacitors with different oxide/nitride thickness combinations were fabricated and irradiated using a Co-60 gamma-source. Electrical characterization showed all samples with oxide/nitride stack gate insulators exhibited significantly higher tolerance to irradiation when compared to metal-oxide-semiconductor capacitors.

Heavy ion testing of the SJMOS showed the device failed due to SEB and SEGR at 10% of maximum rated bias values. In this work, a 600V SJMOS structure is designed that is tolerant to both SEB and SEGR. In a SJMOS with planar gate, reducing the neck
width improves the tolerance to SEGR but significantly changes the device electrical characteristics. The trench gate SJ device design is shown to overcome this problem. A buffer layer and larger P⁺-plug are added to the trench gate SJ power transistor to improve SEB tolerance. Using TCAD simulations, the proposed trench gate structure and the tested planar gate SJMOS are compared. The simulation results showed that the SEB and SEGR hardness in the proposed structure has improved by a factor of 10 and passes at the device’s maximum rated bias value with improved electrical performance.
Dedicated to my parents and my wife Vishnu Priya
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CHAPTER 1

INTRODUCTION

1.1 Importance of Power MOSFETs in Space Missions

Progress in semiconductor devices, through scaling and integration, has contributed to the advancement of modern electronic devices. These devices have become faster and smaller whilst consuming less power. Power electronic devices, which can control and distribute large voltage and currents, play an important role in achieving highly efficient modern electronic systems [1], [2]. The need for scaling is also critical to the need increasing the speed in power devices, e.g., power transistors must now be able to switch at frequencies in the MHz range. The most common use of power transistors is in regulating power supplies. An example of a regulated power supply is the DC-DC buck convertor [3]. A buck convertor is a DC-DC power convertor which steps down a voltage source input to an output voltage across a load, as shown in Figure 0.1.

![Buck DC-DC Converter Circuit](image)

Figure 0.1 Buck DC-DC Converter Circuit.

One of the primary applications for buck convertors is to support a distributed point of load power architecture to increase the power consumption efficiency across a system. The various components present in electronic systems, such as, integrated circuits,
memories, drives and other components have their own voltage and current specifications. In order to reduce the power dissipation across each of these components, a single isolated buck convertor is not enough. Therefore, power convertors must be distributed across the entire system with each convertor placed close to various electronic components and designed specifically to meet their specifications.

The recent growth in the commercial space industry would not be possible without modern electronic systems in which and power devices play an important role. Power devices have several applications in space systems, such as in shunt regulators, buck-boost convertors and power switches. Therefore, understanding how the space radiation environment impact the operation of power devices is critical to ensuring the success of space missions. A brief overview of the harsh radiation environment of space and its effects on semiconductor devices is discussed below.

1.2 Overview of Space Environment

Exploring space and other planetary systems has always been of great interest to human beings, but until recently we did not have the technology to launch into space and make scientific discovery. On October 4, 1957, the first satellite, Sputnik, was launched into space by the Soviet Union and thus the age of space exploration began. Sputnik revolved around the Earth every 96.2 minutes and transmitted radio-frequency signal to Earth for a three-week mission period after which it was decommissioned. Following the launch of Sputnik, the United States launched its first satellite, Explorer 1, on January 31, 1958. Explorer 1 had a Geiger counter to measure the cosmic rays and other energetic particles in space. This satellite helped in discovering that the Earth was surrounded by
high fluxes of energetic particles. Through subsequent missions, the natural radiation environment around the Earth, and other planets in our solar system were mapped and studied.

Analyzing the data from numerous space missions it was found that the energetic particles found in space consisted of all the elements in periodic table ranging from protons and helium ions to heavy ions. In addition to the heavy ions, high energy photons, electrons, neutrons and other sub-atomic particles were also found in the space environment. The origin of these high energy particles is galactic cosmic rays (GCR) and solar energetic particle events such as the solar wind. Figure 0.2. shows the relative abundance of ionized species present in GCR as a function of atomic number. These species have an energy around 2 GeV/atomic mass unit (u). In Figure 0.2 it can be observed there is a significant drop in the relative abundance of ions with the atomic numbers above iron. This is because, the nuclear binding energy reaches the peak at the atomic weight of iron.

![Figure 0.2 Relative Abundance of Different Ion Species in Galactic Cosmic Rays as a Function of Atomic Number at Energies 2 GeV/u [4].](image)
The Earth’s magnetic field prevents most of these ionized particles from reaching the Earth’s surface, however, some of these energetic particles get trapped in the Earth’s magnetic field, thereby forming regions of high particle density in the Earth’s magnetosphere. These regions are called the Van Allen belts. The trapped particles revolve around the magnetic field lines, moving back and forth between the Earth’s poles where the fields terminate. There are two distinct regions in the Van Allen belts, namely the inner belt and outer belt. The inner belt has higher density of protons and low density of trapped electrons. On the other hand, the outer zone contains very high density of trapped electrons as shown in the Figure 0.3.

The composition and density of radiation particles in the Van Allen belts change continuously as a function of time and location due to solar events such as the solar wind and solar flares. The solar wind emits plasma, which contains high energy protons, electrons, sub-atomic particles and sometimes even heavier ions, towards the Earth’s magnetic field. Due to the interaction of this plasma with Earth’s magnetic field, the Van
Allen belt gets compressed on the side facing the Sun and forms an extended tail on the other side of the Earth as shown in Figure 0.4.

Figure 0.4 Space Radiation Environment. Solar Wind Shapes Earth’s Magnetic Field Lines.
After: Nikkei Science, Inc. of Japan, by K. Endo.

Occasionally, the interaction between the plasma from the Sun and its high magnetic field creates huge eruptions of plasma called solar flares and the gigantic solar flares are called Coronal Mass Ejections (CMEs). A huge density of ionized particles, on the order of $10^{10}$ metric tons, with energies of more than $10^9$ eV GeV are ejected during CMEs [9], [10]. Figure 0.5. shows the average particle fluxes of iron and oxygen measured by a solar isotope spectrometer between two solar maxima in years 2001 and 2012. The observed peaks in particle flux, shown in inset graph, correspond to solar flares and the highest one is due to a CME. In addition to solar events, galactic cosmic rays can lead to changes in the particle composition of the Van Allen belts. When ionized particles from solar events and GCRs have high enough energy, they can penetrate the Earth magnetic field and reach below the magnetosphere. This penetration of ionized particle is more pronounced near the Earth poles because the magnetic field lines are more perpendicular to Earth surface and thereby providing less shielding from the energetic particles.
Particle flux is defined as amount of radiation particles crossing per unit area per unit time and the differential particle flux is the differential with respect to solid angle and energy. The differential particle fluxes of different ions such as hydrogen, helium, carbon, silicon and nickel are plotted as function of energy per nucleon in Figure 0.6. for the geostationary Earth orbit (GEO), where the influence of Earth’s magnetic field is less significant. This plot gives a general idea regarding the composition and flux of the particles in GEO between solar maxima and solar minima, caused by difference in Sun’s solar flare activity [8]. The difference observed between maxima and minima is due to the changes in Sun’s magnetic field which causes ions and other charged particles to be deflected. A more detailed description about the Van Allen belts, the ionized particles present in them and variation in the constituents of the particles in accordance with time, location and other solar events can be found in literature.
Figure 0.6 Differential Flux of Selected Galactic Cosmic Ray Particles after 2.54 Mm of Aluminum as a Function of Energy per Nucleon in Near-Earth Interplanetary Space During the Solar Minimum (Solid Line) and the Solar Maximum (Dashed Line) [4].

1.3 Radiation Effects on Microelectronics

Many technological advancements in space systems were developed for communication satellites to support transmission of data back and forth between the satellites and ground stations. The electronic components inside these satellites need to withstand exposure to ionized particles from solar events and GCRs. Damage caused by these particles causes reliability problems and can lead to system failure. The latest major radiation-induced mission failure occurred in January 2012 on the Phobos-Ground mission. Indeed, the space environment, because of the presence of ionizing particles, can cause serious cumulative damage to the electronic devices and lead to transient upset and hard failures. Therefore, a brief study of different phenomena that occurs during the interaction between ionization particles and electronic devices are presented below.

When an energetic ionized particle interacts with matter, it loses its energy through different mechanisms, such as, ionization of target material, recoil loss, electromagnetic radiation, nuclear reactions and chemical reactions. Out of the above mechanisms,
ionization of target material, i.e., creation of electron-hole (e-h) pairs in the target material, is one of the most important phenomena which can lead to upset and failure in electronic devices. In addition to ionization effects by energetic ions in target materials, displacement damage caused by atomic displacements can also cause degradation. Recoil loss and nuclear reactions also contributes to ionization effects during a heavy-ion interaction with the electronic components.

1.3.1 Carrier Generation

When interacting with semiconductor devices ionizing particles transfer some energy to the solid-state material. As a result, e-h pairs (ehps) can be generated in the target material [12], [13]. In ehps generation electrons jump to the material conduction band (CB), leaving mobile holes in the valence band (VB). This mechanism is called ionization and is shown in Figure 0.7.

Since silicon (Si) and silicon dioxide (SiO₂) are the most common material used in current semiconductor devices, the target materials under consideration in this study are Si and SiO₂. At 300K, the energy bandgap (E₉) between the CB and VB in Si and SiO₂ are
approximately 1.1 eV and 9 eV, respectively [14], [13]. The average energy needed to create an ehp, called mean ehp creation energy, can be approximated as,

\[
\text{Mean ehp creation energy} = 2.73E_g + 0.55 \text{ eV}
\]  

(1.1)

Therefore, the mean ehp creation energy value for Si is 3.6 eV and 18 eV for SiO₂. In order for the ionization to take place, three important requirements have to be fulfilled: 1) the energy deposited by the radiation particle must exceed the mean e-h pair creation energy, 2) the density of ehp's generated by ionization process has to be significantly higher than the intrinsic carrier concentration of the target material and, 3) an electric field in the target material to separate the generated ehp's [12].

The mechanism of carrier generation is determined by the particle type. Charged particles such as protons and heavy ions can create carriers through direct ionization which includes, collision and coulombic interactions. When the radiation is in the form of high energy photons, such as X-rays or Gamma rays, three different carrier generations mechanisms may result: 1) photoelectric effect, 2) Compton effect and 3) pair production. In the photoelectric effect, the ehp's are generated by absorbing the full energy of the photon. In case of Compton effect, some of the energy absorbed by the carriers are given back through kinetic energy to the ionizing photons, causing change in the direction of the photon. The Compton effect is the most common type of carrier generation in semiconductor materials when the energy of the photons is in the range of MeV. When a very high energy photon interacts with the matter, a pair production mechanism occurs whereby an electron and positron are created. The positron created decays to become gamma rays which can cause further ionization [13], [14], [15].
As discussed above, in order to ionize a material, the energy from the ionizing particle (or photon through secondary particle emission) needs to be transferred to the target material. This can be quantified by Linear Energy Transfer (LET). LET is the amount of energy deposited by the ionizing particle as it travels through the target material over a unit length and it is normalized to the material density, with unit’s MeV/mg/cm$^2$. LET depends on the mass and energy of the ionizing particle and the density of the target material [16], [17]. As the ionizing particle traverses through the material, it loses its energy to the material and hence the LET continuously decreases as it passes through the material. For an ionizing radiation of fluence $\Phi$ and LET, the density of ehps created in the material with density $\rho$ and mean e-h pair creation energy is given as,

$$\frac{ehp}{cm^3} = \frac{LET \times density \times fluence}{mean \ ehp \ energy} \quad (1.2)$$

1.4 Categories of Radiation Effects in Electronics

In addition to ehp generation, the transport and carrier trapping/recombination properties of the generated carriers also affects the semiconductor material and device response. Radiation effects in devices and circuits, which results from these generation, transport and trapping mechanisms, can be divided into two categories: Cumulative and Single Event Effects (SEE). These effects are discussed below.

1.4.1 Cumulative Effects

When the electronic devices are subjected to ionizing radiation over time, cumulative radiation causes a gradual change in the device properties, such as, shift in threshold voltage, changes in the minority lifetime of the carriers and increase in leakage current [18], [19]. The total cumulative damage caused by ionizing particles is denoted as
Total Ionizing dose (TID). Cumulative damage caused by non-ionizing processes is called Displacement Damage Dose (DDD).

Displacement damage caused by non-ionizing energy loss (NIEL) results when high energy particles collide with the nucleus of the atom in the target material. Energy loss from this collision causes the atoms to get knocked out of their lattice site creating a vacancy. The displaced atom and the vacancy created are called a Frenkel pair [15]. If the incident ion has still significant energy, then it can cause further displacement damage as it travels through the material. When the incident ion loses all its energy, it can replace a dislocated atom in the vacancy, and this is called replacement collision. Also, if the displaced atom has high energy, it can create a cluster of displacement damage. Frenkel pairs can be electrically active, forming traps that cause a reduction in lifetime for minority carriers, decrease carrier mobility, and may decrease major carrier density through dopant compensation. DDD caused by different particles is correlated through NIEL which is calculated as the energy loss per unit mass to lattice displacement as a particle moves through the target material and therefore, NIEL has the same units as LET (MeVcm$^2$/mg) [20]. DDD effects are more pronounced in minority carrier devices like Bipolar Junction Transistors (BJT). Since MOSFETs, the main type of electronic devices studied in this research work, are majority carrier devices, DDD and NIEL effects are not discussed further in this thesis.

In contrast to DDD, cumulative TID effects are observed in both MOS devices and bipolar devices and occur due to buildup of radiation induced defects in solid-state materials [21], [18]. TID is measured in terms of accumulated energy absorbed by the
material from radiation, called dose. The SI unit of dose is a Gray, and it corresponds to amount of dose required to transfer 1 J energy per kilogram in the target material. A more common unit of dose in electronic devices is the rad. 1 Gray equals to 100 rad. Since the effect of dose depends on the material, the dose often specifies the material name in parenthesis after the unit. For instance, when Si is subjected to 100 rad dose, it is represented as 100 rad(Si). As discussed previously, the density of ehps generated by TID depends on incident ion energy and the target material. Although ionization processes can create ehps in both semiconductors and insulators, in MOSFETs the TID damage is primarily due to defect buildup in insulators like SiO$_2$. The primary device parameters that are altered by defects buildup in MOSFETs are surface potential and leakage current [21], [22]. The mechanism of TID and its effects on MOS devices are discussed in detail in chapter 3.

1.4.2 Single Event Effects

When a single energetic charged particle interacts with the electronic devices, the changes observed in the characteristics of the device in response to this ionization event is called a single event effect (SEE). For a SEE, the interaction between the ionizing particle and material is highly localized. In space environment, the particles that cause SEE are primarily high energy protons and heavy ions. In this work, the focus is mainly given to heavy ions.

When an ionizing particle passes through a semiconductor, like Si, ehps are generated along the particle track. This column of ehps can have a radius in the range of nanometers. The total amount of charge generated by a single heavy ion is called deposited
charge and it depends on the LET of the incident ion and other properties of the target material. SEEs can be further divided into two main groups: non-destructive soft errors and destructive hard errors.

1.4.2.1 Soft Errors

When a SEE creates a temporary failure or upset in the electronic circuit functionality, then this event falls under the category of soft errors. The common types of soft errors are: Single Event Upset (SEU), Single Event Transient (SET) and Single Event Functional Interrupt (SEFI) [23]. SEU refers to an event which directly causes a change in stored information, such as a change in the bit state stored in a digital latch, for example, the bit gets flipped from zero to one and vice versa. If multiple bit states are changed by a particle strike, this is called a Multiple Bit Upset (MBU). When a transient signal generated by an ion strike ripples through a circuit, this is called a SET. SEFI is an error which causes loss of device functionality due to resetting of electronic components. When SEU occurs in the control bit or register, then this can cause SEFI [17]. These soft errors can be minimized by incorporating changes in hardware level (circuit design and fabricating process) or in software level (error handling code).

1.4.2.2 Hard Errors

Hard errors refer to the interaction between a single heavy ion and the electronic circuits that create high currents which causes destructive failure. Unlike soft errors, once a hard error occurs, the device functionality is totally or partially lost. The common types of hard errors are, Single Event Latchup (SEL), Single Event Burnout (SEB) and Single Event Gate Rupture (SEGR) [24]. SEL is a destructive effect when a heavy ion creates a
shunt between the power supply and ground. SEL occurs in devices which contains parasitic thyristors, which are present in bipolar and MOSFET technology devices. When a suitable bias condition is present, current generated from the heavy ions can push the parasitic thyristors into current amplification mode with positive feedback. If the power cycling is not done quickly, the high current causes melting of semiconductor lattice and thereby, destroying the device permanently. The current can be stopped only by switching off the power supply.

SEB is a destructive failure mechanism that occurs mainly in power devices due to heavy ion exposure. SEB and SEL are similar, except that instead of requiring a parasitic thyristor structure, a parasitic bipolar transistor is only needed for the SEB to occur [25], [26], [27]. Under a proper bias condition, when a heavy ion hits a sensitive region in a power device, the parasitic bipolar transistor can be switched into a forward active mode. This creates a highly conductive path through the device which can cause permanent damage to the device. N-channel devices are more prone to SEB than P-channel devices, because the parasitic NPN transistor in N-channel devices has higher current gain in forward active mode than the parasitic PNP transistor in P-channel devices. SEGR, as the name suggests, is the breakdown of gate oxide in MOS devices due to passing of heavy ion through the gate oxide [25], [26]. SEGR requires a high electric field across the gate oxide, therefore SEGR occurs mostly in power MOSFETs. Under suitable bias condition, when a heavy ion passes through the device, ehps are created along the ion path in both SiO$_2$ and Si. The ehps created in the gate oxide cause damage to the SiO$_2$ layer and a permanent conductive path connecting the gate electrode and drain electrode is formed. If the LET of the heavy ion is not high enough, then instead of a complete breakdown of gate oxide, the
gate oxide damages are highly localized and only a small increase in gate leakage current is observed. Most times, SEB and SEGR occur simultaneously because one failure can lead to another failure. Both SEB and SEGR mechanisms are described in detail in chapter 4.

1.5 Motivation of the Work

Power BJTs and power MOSFETs are the most common type of power devices available in commercial market. When compared with power MOSFETs, power BJTs are capable of handling higher voltage and currents levels such as 1500V and 1000A, respectively. But one of the main problem in using power BJT is that a constant base current is required to maintain the BJT in on state condition and this causes significant energy loss at high frequency. Therefore, to overcome this limitation, power BJTs are more often being replaced by power MOSFETs in electronic systems. The power MOSFETs can handle voltage up to 1000V and current in the order hundreds of amperes. Unless the application requires very high voltage and current, power MOSFETs are the preferred device over power BJTs. From circuits point of view, designing a gate driven power MOSFET circuit is much simpler than the base current driven power BJTs. Since BJT functionality is depends on the recombination rate of minority carriers, there is a switching delay observed in BJTs. Therefore, the switching speed of power MOSFETs are significantly higher than power BJTs. High switching frequencies help in miniaturization of overall power electronic circuits because, at higher frequencies smaller inductors can be used. Thus, the use of power MOSFET technology has enabled high frequency operation, simpler and smaller power circuits.
The most common type of power MOSFET technology used for in space application purpose are vertical double diffused power MOSFET (VDMOS), which have very thick epitaxial region (low doped drift layer) to block large voltages. This thick epitaxial layer contributes to larger on-state resistance in VDMOS. In late 1990s, a new power MOSFET device technology, called Super Junction power MOSFET (SJ-MOSFET) was introduced in order to decrease the high on-state resistance observed in VDMOS. While this new technology is being used in commercial applications, its usage for space applications are still relatively new. Therefore, the main goal of this work is to develop a high voltage SJ-MOSFET, which can withstand the harsh radiation environment present in space.

Radiation effects mechanisms, such as TID, SEB and SEGR, have more significance on power MOSFET functionality than the other mechanisms, such as DDD, SEU and SEL. Every power device has its own LET requirements, which is based on the duration of the space missions and the location of the satellite orbit. Satellites with longer missions need to withstand higher TID because of the cumulative effect. Based on the location of satellite in Earth’s orbit, the flux and composition of radiation particles vary. Figure 0.8. shows the flux as a function of LET for different satellite orbits (GEO = geostationary orbit; GTO = geotransfer orbit; MEO = middle-earth orbit; EOS = Earth Observing Satellite; LEO = low-earth orbit) and from the figure it can be observed, in most satellite orbits, there is an order of magnitude drop in flux after LET of 25 MeV/mg/cm². Therefore, most power MOSFETs have hardness requirements of passing LET value 40 MeV/mg/cm². Similarly, there is a significant drop in flux at LET 80 MeV/mg/cm². As a result, more critical space missions require the power MOSEFT devices to pass this LET
value. In this work, a radiation hardened (rad-hard) 600V SJ-MOSFET with hardness assurance of TID up to 300 krad(SiO2) and passing LET value of 86 MeV/mg/cm² is developed.

![Integral Flux Vs. LET for Various Orbits During Solar Minimum with 100 Mils Al Shielding](image)

Figure 0.8 Integral Flux Vs. LET for Various Orbits During Solar Minimum with 100 Mils Al Shielding [28].

1.6 Overview of the Work

In chapter 1, the importance of power devices in modern electronic circuits and its use in space applications are discussed. Space is a harsh environment with different types of ionizing radiation particles, such as, photons, electrons, neutrons, protons and heavy ions. Understanding the impact of these particles on electronic devices is important to improve the reliability of the power devices for space applications. Among the power devices, SJ power MOSFETs provide a better solution to improve the performance in space missions and this provides the motivation to develop high power rad-hard SJ MOSFET.

In chapter 2, a detailed discussion of the power MOSFET and the principles behind SJ power MOSFET are discussed. TCAD modelling of the SJ MOSFET studied in this work is performed and the simulation results are compared against the data. In chapter 3, the mechanism of TID and its effect on power MOSFETs are explained. The TID
experimental results of 600V SJ-MOSFET device tested is analyzed and a technique to develop a TID hardened SJ-MOSFET up to 300 krad (SiO2) is provided. In chapter 4, the SEE mechanism and its impact on power MOSFET characteristics are studied. The experiment was conducted on 600V SJ-MOSFET and the results are reported. TCAD simulation is used to analyze the experimental results and to develop a 600V SJ-MOSFET that can survive the impact of heavy ion up to LET value of 86 MeV/mg/cm². Finally, in chapter 5, the summary, conclusion and future work required are offered.
CHAPTER 2
SUPER-JUNCTION POWER MOSFET

Power devices have applications over a wide range of power levels in electronic circuits. Based on these power levels, the applications can be divided into three categories: low current, low voltage and high voltage applications. Applications, such as display drives and communication devices, that require power devices that operate at current levels less than 1A and have the capacity to block voltages up to hundreds of volts, fall into the category of low current applications. These devices are generally small and therefore, can be integrated into the main circuit in a cost-effective way. The second category of low voltage power devices are used in computer power supply convertors and in automotive electronics. These devices have an operating voltage level of less than hundred volts and for these applications, power MOSFETs provide the best solution because of their superior performance and high switching speed. The final category of high voltage and high current applications consists of motor drives, robotic devices and electric trains [29], [30]. Silicon power MOSFETs and silicon BJTs compete for their share in such high-power applications. The above discussion is summarized in Figure 0.1.

As discussed in the previous chapter, silicon power MOSFETs have numerous advantages over power BJTs, such as, faster switching speed, lower switching power loss, better temperature stability, simpler circuit designs and low leakage currents. But in terms of on-state resistance ($R_{DS,ON}$), BJTs outperform the MOSFETs [30]. In this chapter, the fundamentals of power MOSFETs are discussed and then a type of power MOSFET, the Super Junction (SJ) MOSFET, is introduced. The SJ-MOSFET is shown to be superior to
traditional power MOSFET designs for, among other attributes, its reduced $R_{DS,ON}$, which is critical for many high-power applications [31].

![Figure 0.1 Applications of Power Devices for Different Voltage and Current Ratings [30].](image)

2.1 Fundamentals of Power MOSFETs

The power MOSFET was developed in 1970s to overcome the limitations of power BJTs [32]. Figure 0.2 shows the cross-section schematic of N-type Vertical Diffusion MOSFET (VDMOS), which is a vertical, planar gate transistor. The device is named for how it is processed. Ion implantation of the P-body and N-source are self-aligned using the edge of gate electrode, and the channel length is determined by the difference in the extension of P-body and N-source under the gate electrode, which occurs due to the different junction depths and diffusion rates of boron and phosphorous. Similar to conventional MOSEFTs, these are three terminal devices with gate (G), source (S) and drain (D) electrodes and a gate oxide layer located between the gate electrode and active
silicon area. The source and drain electrodes are connected to highly doped N-type regions to obtain a good ohmic contact and the P-body region is also connected to the source electrode. In VDMOS devices, the source and drain are separated vertically by a N-type epitaxial layer. The thickness and doping of this epitaxial layer enable the power MOSFETs to handle high voltages.

Figure 0.2 Cross-section of VDMOS Showing Parasitic Elements.

In a N-type enhancement mode power MOSFET, when a positive bias more than the threshold voltage is applied on the gate electrode, an inversion channel is created at the top of P-body region between the N-source and N-epitaxial layer. When sufficient drain bias is applied, the electrons can flow vertically from the source, through the channel and to the drain contact. In order to achieve high current level during ON state, several thousands of individual transistors are connected in parallel.
All devices contain parasitic elements and VDMOS is no exemption. As shown in Figure 0.2, the parasitic elements present in N-type VDMOS are: NPN BJT and body diode. The N-source, P-body and N-drain acts as the emitter, base and collector of the parasitic NPN BJT. This parasitic transistor is kept mostly OFF by connecting the P-body to the source contact, however this does not remove the parasitic diode. The P-body region connected to the source acts as the anode and the N-epitaxial layer connected to the drain acts as the cathode to form this parasitic body diode [30].

2.2 MOSFET Parameters

The primary figures of merit for the power MOSFETs are voltage blocking capacity, called breakdown voltage (BV or $V_{BD}$) and the magnitude of the device’s intrinsic resistances (including $R_{DS,ON}$) and capacitances. These parameters need to be carefully controlled in power MOSFET design, in order to obtain optimal performance for the device. These parameters for VDMOS devices are discussed in detail below.

2.2.1 Breakdown Voltage

The power MOSFET structure must be able to withstand the high operating voltage levels between the drain and body/source terminals. This is accomplished using the N-epitaxial layer located between the N+ substrate and the P-body. The doping concentration of the N-epitaxial layer and its thickness has to be selected appropriately to attain the necessary $V_{BD}$. To characterize $V_{BD}$, the gate and source electrode are connected together at zero bias and positive bias is applied to the drain terminal. This is the blocking mode. This bias condition creates a reverse bias across the junction between the P-body region and N-epitaxial layer. As the positive bias on the drain electrode is increased, the depletion
region extends mostly into lighter doped N-epitaxial layer until the depletion layer reaches the N⁺-sub region. At $V_{BD}$, the electric field across P-body and N-epitaxial layer reaches a critical electric field value, causing impact ionization and avalanche multiplication which leads to the breakdown of the device. The thickness and doping of P-body region must also be considered, because if the P-body depth is too small or the doping is too low, then the depletion region will extend across the entire P-body region and reach the N⁺-source region, causing breakdown as well [32].

2.2.2 Conduction Losses

Power dissipation in a power MOSFET is due to the resistive elements present in the device. This is called conduction loss. This resistance is between the drain and source and measured when the device is in its ON state, therefore referred to as on-resistance, $R_{ON}$. In a power MOSFET component, thousands of individual devices are connected in parallel to reduce the total $R_{ON}$. Therefore, the die size is inversely proportional to the on-resistance. Since the die size is less dependent on the MOSFET technology, it is common to normalize the resistance of each components to die area and this is called specific resistance. Figure 0.3 shows the eight resistances present between the source and drain electrodes. Since all the resistances are in series, the total on-resistance is the sum of all individual resistances present in the device, i.e.,

$$R_{ON} = R_S + R_{CH} + R_A + R_{JFET} + R_{epi} + R_{SUB} + R_D \quad (2.1)$$

where,
$R_s$ is the source resistance, which includes resistance due to packaging, wire bonding and metallization and the resistance between the source contact and the channel, which depends on the doping of N-source region.

$R_{CH}$ is the channel resistance, which depends on the applied gate bias, threshold voltage of the device and the channel length. In low power MOSFETs, $R_{CH}$ plays the dominant role in total conduction loss.

$R_A$ is the accumulation resistance in the N-epitaxial region, located between the edges of the P-body and below the gate oxide. The electrons passing through the inversion layer get accumulated in the drift region due to the application of positive gate bias. In this region, the electrons start to move from the horizontal to vertical direction.

$R_{JFET}$ is the JFET resistance due to the parasitic JFET created due to the two P-body regions in the device. When the depletion region formed between P-body and N-epitaxial layer increases, the current through the JFET channel decreases, thereby causing an increase in resistance. The JFET resistance depends on the doping of the P-body and N-epitaxial region. It also depends on the distance between the two P-body regions in the device. In order to decrease the $R_{JFET}$ resistance, the doping in this region is made higher when compared to the N-epitaxial layer doping.

$R_{epi}$ is the drift region resistance due to the N-epitaxial layer and is proportional to doping and thickness of this layer. The contribution from this resistance increases as the voltage blocking capability of VDMOS increases.

$R_{SUB}$ is the substrate resistance contributed by the N$^+$ substrate region located below the N-epitaxial layer and the drain contact.
And $R_D$ is the drain contact resistance including the resistance due to packaging, wire bonding and metallization.

In the above list, the resistances, $R_S$, $R_A$, $R_{SUB}$ and $R_D$ are independent of the operating voltage level of power MOSFET and the resistances, $R_{CH}$, $R_{JFET}$ and $R_{epi}$ depend heavily on the drain bias. The Table 0.1 below summarizes the contribution by each resistance for different VDMOS voltage ratings.

![Figure 0.3. Parasitic Resistances of the Power MOSFET Structure.](image)

Table 0.1 Percentage Contributions to $R_{ON}$ for Different Voltage Ratings VDMOS by Various Parasitic Resistor Components.

<table>
<thead>
<tr>
<th>Resistance/Voltage rating</th>
<th>50 V</th>
<th>100 V</th>
<th>500 V</th>
<th>600 V</th>
</tr>
</thead>
<tbody>
<tr>
<td>$R_S + R_D$</td>
<td>22.4 %</td>
<td>14.9 %</td>
<td>4 %</td>
<td>1 %</td>
</tr>
<tr>
<td>$R_{CH}$</td>
<td>34.3 %</td>
<td>28.4 %</td>
<td>4 %</td>
<td>1 %</td>
</tr>
<tr>
<td>$R_{JFET}$</td>
<td>13.4 %</td>
<td>14.9 %</td>
<td>16.4 %</td>
<td>2 %</td>
</tr>
<tr>
<td>$R_{epi}$</td>
<td>22.4%</td>
<td>35.8%</td>
<td>71.6%</td>
<td>95%</td>
</tr>
<tr>
<td>----------</td>
<td>-------</td>
<td>-------</td>
<td>-------</td>
<td>-----</td>
</tr>
<tr>
<td>$R_{sub}$</td>
<td>7.5%</td>
<td>6.0%</td>
<td>4%</td>
<td>1%</td>
</tr>
</tbody>
</table>

From the Table 0.1, it can be observed that as the voltage rating of the device increases, the contribution from $R_{epi}$ to the total resistance of the device increases [29]. Therefore, understanding the relation between the $V_{BD}$ and $R_{ON}$ is of utmost importance and is discussed below.

2.2.3 $V_{BD}$ and $R_{ON}$ Relation

In a 600V VDMOS, $R_{epi}$ contributes to 95% of the total $R_{ON}$. Therefore, it is assumed that for this high voltage device, $R_{ON}$ is approximately equal to $R_{epi}$. The $R_{epi}$ is a function of doping in the N-epitaxial layer. Recall a lower doping in this layer helps the VDMOS device to operate at higher voltages [29], [33]. The properties of the N-epitaxial layer can be analyzed by simplifying the VDMOS vertical section into an p+-n abrupt junction profile, as shown in Figure 0.4.

![Figure 0.4. Ideal Epitaxial (Drift) Region and Its Electric Field Distribution for the Purpose of Calculating the Relation Between $V_{BD}$ and $R_{DS}$.](image)

In the blocking mode, the gate and source terminals are kept at zero bias and a positive bias is applied to the drain terminal. This correlates to reverse biasing the parasitic
body diode. The depletion width, $W_D$, extends into the N-drift (epi) region because of its low doping when compared to the P-body. If it is assumed that the doping in the N-drift region is uniform, the electric field ($E$) has a triangular field profile, with the $E=E_M$ at $x=0$ (the metallurgical junction) and $E=0$ at $W_D$. By solving Poisson’s equation (shown in Equation 2.2), the electric field profile and the maximum voltage that can be supported by the device can be calculated as follows:

$$\frac{\rho}{\varepsilon} = \frac{dE}{dx} = -\frac{d^2V}{dx^2} \tag{2.2}$$

The charge density is

$$\rho = q \ast N_D \tag{2.3}$$

The electric field is obtained by integrating the charge density, with the boundary conditions $E=E_M$ at $x=0$ and $E=0$ at $W_D$

$$E(x) = \frac{-q \ast N_D}{\rho_s} \ast (W_D - x) \tag{2.4}$$

$$E(0) = E_M = \frac{-q \ast N_D}{\rho_s} \ast W_D \tag{2.5}$$

Similarly, by integrating the electric field, the voltage profile can be obtained.

$$V(x) = \frac{q \ast N_D}{\rho_s} \ast \left( W_D \ast x - \frac{x^2}{2} \right) \tag{2.6}$$

$$V(W_D) = V_M = \frac{q \ast N_D}{\rho_s} \ast \left( \frac{W_D^2}{2} \right) \tag{2.7}$$
The breakdown occurs when $E_M$ in the drift region reaches the critical electric field value, $E_C$, that can be supported by the semiconductor material. Therefore,

$$W_{D,max} = \left(\frac{E_C \varepsilon_S}{q N_D}\right)^2$$  \hfill (2.8)

$$V_{BD} = \frac{\varepsilon_S E_C^2}{2 q N_D}$$  \hfill (2.9)

At $E_C$, the material undergoes impact ionization, and this is the cause of breakdown in the device [34]. The impact ionization value is given by Baliga’s power law as,

$$\alpha = 3.507 \times 10^{-35} \times E^7$$  \hfill (2.10)

At breakdown, the ionization integral becomes unity

$$\int_0^W \alpha dx = 1$$  \hfill (2.11)

Combining Equation 2.8, 2.9, 2.10 and 2.11,

The depletion layer width at breakdown is,

$$W_{D,max} = 2.404 \times 10^{10} \times \frac{7}{8} N_D$$  \hfill (2.12)

By substituting the depletion layer width into $E(x)$, the $E_C$ for breakdown of a one-dimensional junction is given by Baliga’s power law,

$$E_C = 3700 \times \frac{1}{8} N_D$$  \hfill (2.13)

By combining Equations 2.8, 2.9, 2.12 and 2.13, $V_{BD}$ for one-dimensional junction calculated by Baliga’s power law is given as,
\[ V_{BD} = 5.34 \times 10^{13} \times N_D^{-\frac{3}{4}} \]  \hspace{1cm} (2.14)

For the high voltage power devices, \( R_{ON} \) is expressed in terms of specific on-resistance (\( R_{ON,SP} \)) which is the resistance times area (unit \( \Omega \cdot \text{cm}^2 \)). For the N-drift (epitaxial layer) region \( R_{ON,SP} \) can be expressed as,

\[ R_{ON,SP} = \frac{W_{D,max}}{q \times \mu_n \times N_D} \]  \hspace{1cm} (2.15)

By substituting, \( W_{D,max} \) and \( N_D, \mu_n = 1500 \); the relation between \( V_{BD} \) and \( R_{ON,SP} \) is given as,

\[ R_{ON,SP} = 8.37 \times 10^{-9} \times V_{BD}^\frac{5}{2} \]  \hspace{1cm} (2.16)

The above expression is called the silicon limit and shows the trade-off between \( R_{ON,SP} \) and \( V_{BD} \), which limits the performance of the VDMOS [29].

2.2.4 Switching Losses

The losses that occur in power MOSFETs due to the parasitic capacitances present in the device are called switching losses. One of the key advantages of power MOSFETs over power BJTs are their ability for faster switching speeds. However, rate at which the power MOSFET can be turned ON and OFF depends on the rate of charging and discharging of the parasitic capacitances [29]. The different parasitic capacitance present in VDMOS are shown in Figure 0.5.
The definition of these capacitances is given as follows:

\( C_{N+} \) is the capacitance created by the overlap of gate electrode with the N-source region. During all bias condition, \( C_{N+} \) is equal to the gate oxide capacitance.

\( C_P \) is the capacitance of the overlap gate electrode with the P-body region. This capacitance is a strong function of gate bias, because during positive gate voltage an inversion layer is created in this region. Therefore, \( C_P \) is a function of gate oxide capacitance and the depletion layer capacitance created in the P-body.

\( C_{SM} \) is the capacitance created by the overlap of source electrode over the gate electrode. This overlap is designed to reduce the source contact resistance and avoids the need for narrow metal contacts. This capacitance can be decreased by using a thick inter-electrode oxide.
Since $C_{N+}$, $C_P$ and $C_{SM}$ are connected in parallel so their sum makes the gate-source capacitance, $C_{GS}$

$C_{GD}$ is the gate-drain capacitance due to the overlap of gate electrode with the N-epitaxial layer. The P-body and the N-epitaxial layer creates a depletion region in the JFET region of VDMOS. The total value of this capacitance depends on the gate oxide capacitance and the capacitance created due to the depletion layer formed in the N-epitaxial layer, which are connected in series. The width of the depletion layer depends on the bias applied on the drain terminal. As the positive bias on the drain is increased, the depletion layer thickness increases and therefore, $C_{GD}$ decreases. Also, this capacitance strongly depends on the gate width because the area of overlap between gate and N-epitaxial layer increases as the gate width increases and this causes the $C_{GD}$ to increase.

$C_{DS}$, the drain-source capacitance, refers to the capacitance created in the depletion region formed between the P-body and N-epitaxial region. Since this depletion layer width increases with drain bias, $C_{DS}$ decreases as the bias on the drain terminal is increased. The depletion layer of this capacitance is larger than the depletion layer below the gate oxide because significant part of the drain voltage is supported across this junction.

Figure 0.6 shows the equivalent circuit in MOSFET with the intrinsic capacitances. The capacitance values that are specified in datasheets are input capacitance ($C_{ISS}$), output capacitance ($C_{OSS}$) and the reverse transfer capacitance ($C_{RSS}$).
These capacitance specification can be related to the intrinsic capacitors with the following formula:

\[
C_{ISS} = C_{GS} + C_{GD} \quad (2.17)
\]

\[
C_{OSS} = C_{DS} + C_{GD} \quad (2.18)
\]

\[
C_{RSS} = C_{GD} \quad (2.19)
\]

Figure 0.7 plot the behavior of these capacitance as a function of drain bias. It can be observed that \(C_{ISS}\) is almost constant as function of drain bias while \(C_{OSS}\) and \(C_{RSS}\) decreases for lower \(V_{DS}\) eventually saturating as drain bias increases.
From the above discussion it is clear that the main power dissipation during switching occurs due to the charging and discharging of the capacitance $C_{GD}$, which can be reduced by decreasing the gate overlap over the N-epitaxial region. This causes the switching loss at high frequency to decrease significantly. But decreasing the gate overlap with N-epitaxial layer, increases the effect of parasitic JFET resistance and thereby increasing the $R_{ON}$. Therefore, careful optimization of the power MOSFET design parameters is necessary to achieve better performance of the device.

### 2.3 Fundamentals of SJMOS

The high blocking voltage capability for VDMOS transistors is achieved by increasing the thickness and decreasing the doping concentration of the N-epitaxial layer. However, both of these methods lead to an increase in the epitaxial layer resistance, $R_{epi}$. In 600V VDMOS, $R_{epi}$ contributes to 95% of the total $R_{ON}$. In conventional VDMOS devices, the $V_{BD}$ and $R_{ON}$ are related as $R_{ON} \propto V_{BD}^{2.5}$, which is called the silicon limit. To overcome this fundamental limit of VDMOS devices, a new technique called Super-Junction was introduced in 1990s [35].
Figure 0.8 shows the cross-section schematic of a N-type SJ power device. The key difference between VDMOS and the SJ structure is the replacement of N-epitaxial layer in VDMOS with an alternating columns of P- and N-type doping. The addition of the P-column in the N-epitaxial layer aids in the distribution of the electric fields when a positive bias is applied to the drain terminal. The physics behind the improvement in $V_{BD}$ for SJ structure is achieved by charge balance concept which is discussed below.

![Cross-section of SJMOS Device Showing Parasitic Resistors.](image)

2.3.1 Charge Balance

In VDMOS devices, the depletion region extends in one-dimension at the P-body and N-epitaxial layer junction. In the case of SJ-MOSFET devices, the depletion width extends in two-dimensions, one at the P-body and N-epitaxial layer junction and the other at P-column and N-epitaxial layer junction. Therefore, instead of obtaining a triangular electric field profile with maximum field at the p-n junction like VDMOS, a rectangular electric field profile with uniform field can be achieved in the SJ-MOSFET. Figure 0.9
shows the flatter (rectangular) field obtained for 600V SJ-MOSFET at different drain biases. The location of the cutline is shown in the Figure 0.8.

According to Poisson’s equation (Equation 2.2), the voltage is the integral of the electric field. Therefore, $V_{\text{BD}}$ is the area under the electric field profile when the peak of electric field is equal to the critical electrical field of the semiconductor material. For VDMOS devices the $V_{\text{BD}}$ is the area under the triangular electric field profile and for SJ-MOSFET devices $V_{\text{BD}}$ is the area under the rectangular field profile. Thus, for a value of $E_C$ (0.2 MV/cm in the figure), significantly higher $V_{\text{BD}}$ can be achieved in SJ-MOSFET when compared with VDMOS.

![Figure 0.9 Comparison of Electric Field Profile of VDMOS and SJMOS at 100V and at $V_{\text{BD}}$ (150V for VDMOS and 600V for SJMOS).](image)

The ratio between the charges in each column is called charge balance and is given in Equation 2.20. For a SJ-MOSFET of specific dimension, maximum $V_{\text{BD}}$ can be achieved when the field profile is rectangle. In order to obtain rectangular electric field profile, the net charge present in both P and N columns should be equal, that is, the charge balance
(CB) should be equal to zero. The charge balance depends on the dimensions and doping concentration of the P and N columns [29]. Positive and negative CB causes changes in the rectangular field profile by creating electric field peak at bottom and top of the N-type SJ structure, respectively.

\[
CB = \frac{P \text{ layer charge} - N \text{ layer charge}}{N \text{ layer charge}}
\]  \hspace{1cm} (2.20)

2.3.2 Relation Between \( V_{\text{BD}} \) and \( R_{\text{ON}} \) in SJMOS

The main purpose of SJ-MOSFET is to overcome the silicon limit of VDMOS devices. Similar to VDMOS, the dominant factor in \( R_{\text{ON}} \) of high power SJ-MOSFET is also the resistance across the epitaxial region. The relation between \( V_{\text{BD}} \) and \( R_{\text{ON}} \) is discussed below [29], [35].

In order to achieve good rectangular electric field profile, the depletion width must extend across the entire P and N columns at critical electric field. Therefore,

\[
E_C = q * N_D * \frac{W_N}{2} * \varepsilon_S = q * N_A * \frac{W_P}{2} * \varepsilon_S
\]  \hspace{1cm} (2.21)

This above equation provides the criteria for choosing the doping concentration and the thickness of P and N columns. The width of P and N columns are inversely proportional to their doping concentration. Therefore, the width of the N-column should be made as small as possible because this allows an increase of its doping concentration which helps in decreasing the \( R_{\text{ON}} \).

Using Baliga’s formula for impact ionization, the \( E_C \) can be given as,
where \(L_D\) is the thickness of the drift (epitaxial layer) region.

In a SJ-MOSFET, when rectangular electric field profile is achieved by charge balance, the maximum voltage blocking capacity is given by the area under the electric field profile.

\[
V_{BD} = E_C \times L_D
\]  \hspace{1cm} (2.23)

and

\[
V_{BD} = 8.36 \times 10^4 \times L_D^{\frac{6}{7}}
\]  \hspace{1cm} (2.24)

Therefore, the critical electric field for a given \(V_{BD}\) is,

\[
E_C = 5.53 \times 10^5 \times V_{BD}^{-\frac{1}{6}}
\]  \hspace{1cm} (2.25)

The optimum doping concentration for a given \(V_{BD}\) can then be given as,

\[
N_D = 1.106 \times 10^6 \times \frac{\varepsilon_S}{q \times W_M} \times V_{BD}^{-\frac{1}{6}}
\]  \hspace{1cm} (2.26)

and the specific \(R_{ON,SP}\) is given as,

\[
R_{ON,SP} = \rho_{ND} \times L_D \times \left(\frac{W_{cell}}{W_N}\right) = \frac{L_D}{q \times \mu_n \times N_D} \left(\frac{W_N + W_P}{W_N}\right)
\]  \hspace{1cm} (2.27)

By writing \(L_D\) and \(N_D\) in terms of \(E_C\) and \(V_{BD}\),

\[
R_{ON,SP} = \frac{V_{BD}}{\varepsilon_S \times \mu_n \times E_C^2} \left(\frac{W_N + W_P}{2}\right)
\]  \hspace{1cm} (2.28)

Since it is common in SJ-MOSFETs to have the width of P and N column the same,
$$R_{ON,SP} = 3.27 \times 10^{-12} \frac{V_{BD}^{4/3} \cdot W}{\varepsilon \cdot \mu_n}$$  \hspace{1cm} (2.29)$$

Figure 0.10 shows the $R_{DS,ON}$ vs. $V_{BD}$ relation plot of SJ-MOSFET for different column thickness and is compared against the silicon limit of VDMOS devices. From the figure, it can be observed that as $V_{BD}$ increases the SJ-MOSFET has lower $R_{DS,ON}$ than the VDMOS devices.

2.4 Different SJMOS Structures

The SJ-MOSFET can be implemented using different techniques. A brief discussion of the different types of fabrication methods are discussed below.

2.4.1 Multi-Epitaxy SJMOS

The first commercial SJ-MOSFET was developed by Infineon using multi-epitaxial fabrication technique and was called CoolMOS transistor [31]. Figure 0.11 shows the general process flow of the multi-epitaxial SJ-MOSFET. To begin with, the N-type
epitaxial layer is grown on the substrate and followed by masked Boron implantation to
develop the P-column. This structure is subjected to thermal process to allow the diffusion
of Boron atoms. This step is repeated several times depending on the depth of P and N
columns. It is important to notice that the first Boron atoms are subjected to thermal drive-
ins multiple times depending on the number of Boron implantation steps. Therefore, the
cell pitch in multi-epitaxial SJ-MOSFET is restricted by the Boron implantation process
[31], [36].

![Figure 0.11 Schematic Process flow of Multi-Epitaxy Technology for SJ Device Fabrication CoolMOS](image)

2.4.2 Deep Trench SJMOS

Another common technique used to build the SJ-MOSFET structure is by using
deep trenches. There are several ways to implement this technique.

2.4.2.1 Deep Trench Combined with Epitaxial Growth

Figure 0.12 shows the process steps involved in the deep trench epitaxial growth
type of SJ-MOSFET fabrication. In this technique, deep trenches are etched on the N-type
epitaxial wafer and then followed by a high temperature bake to remove the native oxides.
Finally, epitaxial P-type silicon is grown and thus forming alternate P and N columns. By
careful optimization of gas flows, high aspect ratio trenches can be formed [37], [38].
2.4.2.2 Deep Trench Combined with Vapor Phase Doping

Figure 0.13 shows the process steps involved in the deep trench vapor phase doping. In this technique, Boron implantation is performed on the N-type epitaxial wafer, followed by etching to form deep trenches [40]. A high temperature bake is done to remove the native oxides. Using vapor phase doping, Boron is diffused into the sidewalls of the trench and thermal drive-in is conducted to form the necessary P-column doping profile. Finally, the trenches are filled by depositing TEOS [41], [42].
2.4.2.3 Deep Trench Combined with Multiple Ion Implantation

Figure 0.14 shows the process steps involved in the deep trench multiple ion implantation type of SJ-MOSFET fabrication. In this technique, deep trenches are first formed and followed by growth of native oxides in the deep trench. Multiple Boron implantation steps at various angles are performed based on the aspect ratio of the trench. A thermal drive-in step is done so that the implanted Boron forms the required P-column profile. The native oxide was grown prior to implantation step to avoid the diffusion of Boron towards the trench. Finally, the trenches are filled by depositing TEOS [43], [44], [45].
2.5 TCAD Modelling of SJMOS

TCAD tools provide the opportunity to simulate various electronic devices fabrication profiles and the corresponding electrical and thermal characteristics of the devices in different electrical conditions. The TCAD tool used in this work for simulating the SJ power MOSFET characteristics is a general purpose commercial Silvaco TCAD software tool.

The SJ-MOSFET was designed in the TCAD tool using the device structure dimensions and the doping profiles that were obtained from the commercial manufacturer of the SJ-MOSFET device used in this work. The device structure was developed by manually defining the various regions of the MOSFET and its doping profile. Initially, the doping concentration, doping distributions and junction depth used in TCAD simulation were based on manufacturer specifications and the simulated device characteristics matched the device experimental data. But for the purpose of ease of simulation, the doping profile used in later stage simulation structure development was an abrupt profile junction.
The Silvaco’s device simulator module, Atlas, is used to simulate the electrical characteristics of the electronic devices. It solves fundamental equations such as continuity and Poisson’s equations. The Atlas module solves these equations based on the finite element method at every discrete node, called mesh points. The mesh nodes have to be properly defined so that consistent solution is obtained. In device regions with junction boundaries and surfaces a more refined mesh is required to get accurate results. In the Atlas tool electrical contacts and other physical modules such as electric field and doping concentration dependent mobility models, Shockley-Red-Hall and Auger recombination models, impact ionization models for avalanche effect are included to simulate more realistic device electrical characteristics [46], [47].

Once the power MOSFET structure is built in TCAD and necessary physical models are included in the Atlas device simulator module, the SJ-MOSFET’s electrical characteristics such as $I_D-V_{GS}$ and $I_D-V_{DS}$ relationship can be simulated. Also, important electrical parameters such as breakdown voltage, threshold voltage and source to drain on-state resistance can be extracted. Figure 0.15 and Figure 0.16 shows a comparison of experimental data and TCAD simulation results of the $I_D-V_{GS}$ and breakdown voltage curve. Table 0.2 compares the $V_{TH}$, $BV$ and $R_{DS,ON}$ values of the experimental data and the simulated results. From the figures and table, it could be observed that the TCAD results matches with the data and thus validating the accuracy of the simulated device structure.
Figure 0.15 Comparison of Data and TCAD Simulated $I_{DS}$ vs. $V_{GS}$ for the SJMOS Studied in this Work.

Figure 0.16 Comparison of Data and TCAD Simulated $V_{BD}$ for the SJMOS Studied in this Work.

Table 0.2 Comparison of $V_{TH}$, $V_{BD}$ and $R_{DS,ON}$ Between Data and TCAD Simulation for SJMOS.

<table>
<thead>
<tr>
<th>Characteristics</th>
<th>Data</th>
<th>Simulation</th>
</tr>
</thead>
<tbody>
<tr>
<td>$V_{TH}$ (V)</td>
<td>3.3</td>
<td>3.3</td>
</tr>
<tr>
<td>$R_{DS,ON}$ (Ω)</td>
<td>0.06</td>
<td>0.06</td>
</tr>
<tr>
<td>$BV$ (V)</td>
<td>700</td>
<td>700</td>
</tr>
</tbody>
</table>
CHAPTER 3
RADIATION HARDENING AGAINST TOTAL IONIZING DOSE

Due to larger feature sizes of power MOSFETs, exposure to continuous ionizing radiation can significantly affect their electrical functionality [48], [49]. The mechanisms of total ionizing dose (TID) on SJ power MOSFETs will be discussed in the first part of this chapter. The second part discusses about hardening techniques that can be used to address TID damage.

3.1 TID Mechanisms

When electronic devices are subjected to TID, e-h pairs are created in a uniform manner across the entire semiconductor and insulator regions. The density of e-h pairs generated in the target material depends on the energy, charge and mass of the incoming ionizing particle and also the density and the electronic properties of the target material. TID can be caused by photons or high energy, electrons, protons, or other heavy ions. This study mainly focusses on TID caused by photons. Based on the kinetic energy of the photon, three different effects can occur when photon interacts with the target material. These are the photoelectric effect, Compton effect and the pair production [19], [50]. The photoelectric effects occur when the photon is lower in energy. The kinetic energy of the photon is absorbed by the target material and knocks the inner core electrons of the target material. This electrons are called photoelectrons and when they have enough energy, they can also help in creation of e-h pairs. Compton scattering involves higher energy photons, typically associated with gamma rays, interacting with the target material and emitting a Compton electrons and a photon with less energy, both of which help in e-h pair creation. Pair production occurs when a very high energy photon of energy greater than 1.02 MeV,
which is the sum of rest mass energy of electron and positron, interacts with the target material and thereby creating an electron and positron. Figure 0.1 marks the zones for these different ionizing mechanisms as a function of photon energy vs. the atomic number of the target material. In this study, a Cobalt-60 gamma source which emits photons of energy 1.25 MeV was used, thus Compton scattering mechanism is the main carrier generation mechanism in the target materials of interest, i.e., silicon and silicon dioxide.

![Figure 0.1 Plot of Photon Energy Vs Atomic Number of Target Material Indicating the Probability of Occurrence of Different Mechanisms in the Target Material [13].](image)

When power MOSFETs are exposed to ionizing radiation, the amount of cumulative degradation in their electrical characteristics can be related to the density of e-h pairs generated in the gate and isolation oxides. Figure 0.2 shows the different processes occurring in an oxide when exposure to ionizing radiation. The figure shows the band structure of MOS system under positive gate bias. The e-h pairs created in the oxide can either recombine or can get trapped in the dielectric. The density of electrons and holes that recombine is a strong function of electric field present in the oxide and the fraction that do
not undergo recombination is called charge yield. A higher electric field causes less recombination and therefore higher charge yield [51].

![Figure 0.2 Schematic Energy Band-Diagram of a MOS Structure Showing Different Mechanisms When Subjected to TID Under Positive Gate Bias [12].](image)

The carriers that escape recombination may undergo trapping in the oxide or may leave the oxide system. The mobility of electron is much higher when compared with hole mobility in SiO$_2$ and therefore, the generated electrons are quickly swept out of the oxide. Depending on the direction of electric field, the electrons move either to the gate terminal or to the silicon substrate. Holes may also move towards or away from the Si-SiO$_2$ interface by hopping through defects and traps present in the oxide and some fraction of this unrecombined holes get trapped in the defect centers. Hole transport in SiO$_2$ normally occurs in the range of seconds but because the hole mobility in SiO$_2$ is highly dispersive, this transport can occur over much longer time periods. When the holes move towards the Si-SiO$_2$ interface, the electrons from the silicon substrate tunnel through the oxide and neutralize some of the holes present in trap centers. The remaining unrecombined holes get locked in the deep trap levels present in the oxide bulk, as positive oxide trapped charges [52]. Another form of degradation that occurs in the gate oxide due to TID are the interface traps which are caused by the presence of silicon dangling bonds present at the Si-SiO$_2$
interface. During MOSFET processing, hydrogen gas is used to decrease the density of dangling bonds present in the gate oxide. But when MOSFETs are subjected to TID, hydrogen ions are released in the oxide bulk due to molecular reactions with holes. These hydrogen ions then interact with Si-H bonds and form H₂, exposing dangling bonds at the interface. These dangling bonds act as interface traps when their energy levels are located in the silicon bandgap. The occupancy and their charge contribution to the MOS system depends on the silicon substrate doping and varies as a function of applied bias [12]. In addition, there are type of traps called border traps which are oxide trapped charges that are located near the Si-SiO₂ interface and act in ways similar to interface traps [53]. All the three types of charge trapping centers, their mechanism and the effect on device parameters are explained below.

3.1.1 Oxide Trapped Charges (N_OT)

Oxide trapped charges are defect sites located in the oxide bulk and near the Si-SiO₂ interface, which contribute positive charge to the MOS system. The main precursor defect that can trap holes is the E’ center or an oxygen vacancy [54], [55]. Different possible structures of E’ are possible in SiO₂ and among them the main contributor to the precursors are E’γ configuration which is a trivalent silicon atom. It is bonded to three oxygen atoms and to another silicon atom through a strained bond configuration [56]. The oxygen vacancies are created either by ion implantation, incomplete oxidation during oxide growth or high temperature annealing during device processing. Therefore, the density of precursors in a given device depends mainly on the process technology [57]. When the trivalent silicon atoms are subjected to irradiation, the strained Si-Si bond breaks down by capturing a hole and becomes an Electron Paramagnetic Resonance active state, where one
of the silicon atom traps the hole created by TID and the other silicon contains a dangling bond with one unpaired electron. This is shown in Equation 3.1, where the left side of the equation shows two trivalent silicon atom with a strained bond configuration and the right side contains one silicon atom with a positive charge hole and the other silicon atom with a dot indicating the presence of unpaired electron. Both these silicon atoms relax in their current state and the silicon with the hole trapped becomes a positive oxide trapped charge [58], [54]. Figure 0.3 shows the trivalent Si atom configuration which acts as precursor and the Electron Paramagnetic Resonance active state.

\[
\equiv \text{Si} - \text{Si} \equiv + \overset{\text{irradiation}}{h^+} \rightarrow \equiv \text{Si} \cdot \text{Si} \equiv \quad (3.1)
\]

Figure 0.3 Schematic Showing the Formation of E’ Center from Si-Si Bond [12].

In a MOS capacitor with no \( N_{OT} \), the gate voltage needs to be more than the threshold voltage to create an inversion layer. On the other hand, when the \( N_{OT} \) density increases due to TID, the positive charge in the oxide creates an additional electric field which causes shift in threshold voltage that is required to create an inversion layer [59], [60]. In the p-type silicon substrate where the \( V_{TH} \) is positive, \( N_{OT} \) causes a decrease in \( V_{TH} \) and in the case of n-type silicon substrate where the \( V_{TH} \) is negative, \( N_{OT} \) causes increases in \( V_{TH} \).
3.1.2 Interface Traps (N_{IT})

The interface traps are defects located near the Si-SiO$_2$ interface having energy levels in the silicon bandgap. The precursors for interface traps are P$_b$ centers. The P$_b$ center is a trivalent silicon with the silicon bonded to three other silicon atoms in the substrate and the fourth bond being a dangling bond extending into the oxide layer [61], [62]. There are two types of P$_b$ centers, P$_{b0}$ and P$_{b1}$ and their origin depends on the fabrication process of the device. The difference between the two centers is that for P$_{b0}$ the dangling bonds are normal to the Si-SiO$_2$ interface, whereas, the dangling bonds in P$_{b1}$ are at an oblique angle to the Si-SiO$_2$ interface [63]. Figure 0.4 and Figure 0.5 shows the two P$_b$ centers present in the Si (111) and Si (100) substrates, respectively [64]. In order to reduce the density of dangling bonds, hydrogen passivation is performed during a post-fabrication process and therefore, the dangling bond of trivalent silicon atoms gets attached to a hydrogen atom.

![Figure 0.4 Schematic Representation of P$_{b0}$ Defect Center With Dangling Bond Extending at a Normal Angle at the SiO$_2$/Si (111) Interface [65].](image_url)
The most accepted model of interface trap formation during irradiation is described by two stage model. In the first step, the holes created during TID exposure interact and break the passivated Si-H bonds present in oxide bulk as they transport. The interaction produces free hydrogen ions. In the second step, the released hydrogen ions undergo hopping, some towards the Si-SiO$_2$ interface where they break another Si-H bond, forming a neutral H$_2$ molecule and leaving an unbalanced dangling bond [64], [66]. Figure 0.6 describes the two-stage mechanism in graphically. Two types of reactions can occur when a hydrogen interacts with another Si-H bond as shown in the Equations 3.2, 3.3 and 3.4. In the first case, the hydrogen released in fist stage remains as positive ion and interact with another Si-H bond, thereby forming a silicon dangling bond with positive charge (Equation 3.2). In second case, the hydrogen ions released in first stage can undergo chemical reaction and become neutral hydrogen, where the electron is obtained from the silicon substrate. This neutral hydrogen breaks a Si-H bond creating H$_2$ molecule and a silicon dangling bond with negative charge (Equation 3.3 and 3.4).

First case,
\[ \text{H}^+ + \text{H} - \text{Si} \equiv \text{Si} \rightarrow \text{H}_2 + \text{Si}^+ \equiv \text{Si} \]  
(3.2)

Second case,

\[ \text{H}^+ + \text{e}^- \rightarrow \text{H}^0 \]  
(3.3)

\[ \text{Si} \equiv \text{Si} - \text{H} + \text{H}^0 \rightarrow \text{Si}^- \equiv \text{Si} + \text{H}_2 \]  
(3.4)

Figure 0.6 Schematic Showing the Mechanism of Formation of Pb Center at the SiO\textsubscript{2}/Si Interface Using Hydrogen Model [12].

The interface traps are considered to be active when their energy levels lie between the silicon bandgaps. There are two types of traps. The traps in the lower half of the silicon bandgap, below the intrinsic Fermi level, are donor like and the traps in the upper half of the bandgap, above the intrinsic Fermi level, are acceptor type [12]. The charge contribution of donor type \( N_{IT} \) is positive when they are empty and neutral when filled by an electron. The charge contributions of acceptor type traps are negative when filled with electron and neutral when the trap is empty. At room temperature, most of the interface traps below the Fermi level are filled and the traps above the Fermi level are empty.
Therefore, the density of charged and uncharged N\textsubscript{IT} in a MOS device depends on the bias applied to the gate terminal because the bias modifies the position of the intrinsic Fermi level (and surface potential) with respect to Fermi level. In a MOS device with a p-type silicon substrate and biased in accumulation, donor type N\textsubscript{IT} will be empty contributing to additional positive charge. When the device is in inversion, acceptor type N\textsubscript{IT} are filled with electrons, thereby contributing to negative charge which in turn causes increase the \( V\text{\textsubscript{TH}} \). In a n-type silicon substrate MOS device biased in accumulation, acceptor type N\textsubscript{IT} will be filled creating additional negative charge and when the device is in inversion, donor type N\textsubscript{IT} will empty contributing to positive charge which causes increase in \( V\text{\textsubscript{TH}} \). Therefore, increase in N\textsubscript{IT} density causes increase in \( V\text{\textsubscript{TH}} \) in both p-type and n-type substrates [33], [67]. In addition to causing a shift in \( V\text{\textsubscript{TH}} \), since the contribution of charges from N\textsubscript{IT} varies with the biased applied, unlike N\textsubscript{OT}, change in charged N\textsubscript{IT} density also causes a stretch out in the slope of the I-V and C-V curve in MOSFETs and MOSCAPs, respectively. Figure 0.7 shows the schematic representation of acceptor and donor N\textsubscript{IT} in a p-type MOSCAP for different applied bias condition.
3.1.3 Border Traps

Border traps are oxide trapped charges that are present near the Si-SiO$_2$ interface that can exchange charge with silicon substrate like an interface trap, although at much slower times [69], [70]. Therefore, the electrical signature of border trap resembles that of N$_{IT}$, but the charging and discharging ranges over a wide time period. Although research is still ongoing to determine the structure of the border trap defect, there is growing evidence that the precursors for border traps are similar to N$_{OT}$, i.e. E$_{\gamma}'$ centers. Border traps, because of their spatial distribution in the oxide produces a hysteresis effect in C-V and I-V measurements and depend strongly on the voltage sweep rate [69]. Figure 0.8 shows the schematic location of border traps in MOS system.
3.1.4 Charge Separation Technique

It is helpful to determine the densities of N_{OT} and N_{IT} created due to TID in a MOS device because it supports the analysis of TID effects and susceptibilities for a given MOS technology. The mid-gap charge separation technique is used to calculate the density of N_{OT} and N_{IT} in a MOS device by observing the shift produced by these traps [59]. As discussed earlier, the charge contribution from N_{IT} depends on the Fermi level position. At a particular gate voltage applied to a MOS device (during either an I-V and C-V measurement sweep), the Fermi level at the silicon interface is the same energy as the intrinsic Fermi energy. This gate voltage is called mid-gap voltage (V_{MG}) [59]. At V_{MG}, the acceptor like N_{IT} and donor like N_{IT} are charged neutral as shown in the Figure 0.7. Therefore, the change in V_{MG} is solely caused by an increase in N_{OT} density and is given as

\[ \Delta V_{OT} = \Delta V_{MG}, \]  

Figure 0.8 Shows Physical Location of N_{OT}, N_{IT} and Border Traps and Their Electrical Response in a MOS Structure [70].
where $\Delta V_{OT}$ is the voltage shift caused by the increase in $N_{OT}$ density.

At $V_{TH}$, the shift is due to both $N_{OT}$ and $N_{IT}$ charge contribution and therefore can be expressed as

$$\Delta V_{IT} = \Delta V_{TH} - \Delta V_{MG}, \quad (3.6)$$

where $\Delta V_{IT}$ is the voltage shift caused by the increase in $N_{IT}$ density.

Assuming that the $N_{OT}$ is present as a sheet charge along the Si-SiO$_2$ interface, the density of $N_{OT}$ and $N_{IT}$ created during TID can be calculated as,

$$\Delta N_{OT} = -C_{OX} \times \frac{\Delta V_{OT}}{q}, \quad (3.7)$$

$$\Delta N_{IT} = -C_{OX} \times \frac{\Delta V_{IT}}{q}, \quad (3.8)$$

where $C_{OX}$ is the oxide capacitance per unit area.

### 3.2 TID Effects on SJMOS

From the above discussion about TID mechanisms and effects on MOS devices, it is clear that the ionizing dose affects electrical characteristics through defect creation in gate oxides. The thickness of the gate oxide also determines the density of $N_{OT}$ and $N_{IT}$ created in the oxide layer and therefore, plays an important role in the ability of the MOS device to withstand TID [48], [49]. In early generations of commercial CMOS devices, the gate oxides were significantly thick and thus, the density of defects created were high. But in current highly-scaled CMOS technologies, the thickness of the gate oxide is well below. These thin gate oxides are typically extremely hard to doses of more than 1 Mrad [SiO$_2$].
On the other hand, in case of high power MOSFET devices, because of their need to support high gate voltages, the gate oxide thickness is typically greater than 80nm. For the 600V SJ power MOSFET considered in this work, the $t_{ox}$ is approximately equal to 100nm. As a result, these devices are very susceptible to TID, which makes them particularly vulnerable in space missions. In the section below, TID results on a 600V SJ-MOSFET are presented and methods for hardening them for dose levels above 300 krad [SiO$_2$] are discussed.

3.2.1 TID Experimental Setup

TID experiments were conducted at the Gamma cell 220 irradiator facility in Arizona State University. The 600V N-type SJ power MOSFETs discussed in previous chapter were irradiated using the Cobalt-60 gamma rays at a dose rate of 340 rad (SiO$_2$)/min. Two different bias conditions were applied during irradiation and three devices were irradiated for each bias condition. In the first case, all the device terminals were grounded during irradiation and in the second condition, the drain and source terminals were grounded while the gate terminal was maintained at -1V. The temperature during irradiation was kept constant at room temperature. Electrical characterizations were carried out prior to irradiation and after radiation doses of 20 krad [SiO$_2$] , 50 krad [SiO$_2$] , 100 krad [SiO$_2$] , 150 krad [SiO$_2$] , 200 krad [SiO$_2$] , 250 krad [SiO$_2$] , and 300 krad [SiO$_2$] . The devices were electrically characterized within 30 minutes of each irradiation step. The electrical characterization was carried out using an Agilent 4156 and the source measurement units (SMU) were used to measure the currents within the device. Drain to source current ($I_{DS}$) vs. gate to source voltage ($V_{GS}$) characteristics with $V_{DS} = V_{GS}$ was measured. This characteristics can be used to measure threshold voltage shifts and other
effects. The maximum current capability of the Agilent 4156 is 0.1 A which limited the range of voltages used to characterize the devices. In addition to this measurement, $V_{BD}$ and $R_{DS,ON}$ also were measured to identify whether TID causes any change in these critical device characteristics. Since the TID response of all the irradiated devices were identical, the electrical characteristics of only one device for each bias condition is plotted. The electrical measurements were carried out again after 90 days to examine whether annealing has occurred during this time period. After these later tests, the devices characteristics remained essential unchanged, implying an absence of annealing.

3.2.2 TID Experimental Results

Figure 0.9 shows the drain current vs gate to source voltage plot before irradiation and after radiation dose levels of 20 krad [SiO$_2$], and 50 krad [SiO$_2$] for the case where all the terminals were grounded. The $V_{TH}$ according to datasheet is defined as the $V_{GS}$ at which $I_{DS}=250\mu$A and it can be observed that there is a decrease in threshold voltage as the TID increases. As discussed earlier, a decrease in $V_{TH}$ is due to increased $N_{OT}$ in gate oxide due to TID. In the $I_{DS}$-$V_{GS}$ measurement, no change in the sub-threshold slope was observed, which reveals negligible $N_{IT}$ buildup in the gate oxide-silicon interface. In addition to the decrease to in $V_{TH}$, an increase in leakage current was observed as TID increases, which can be attributed to increase of $N_{IT}$ in the inter-device isolation oxide. Similar characteristics were observed for the case where the gate terminal was connected to -1V, except less shift in $V_{TH}$ was observed.
Figure 0.9 $I_{DS}$-$V_{GS}$ Characteristics of the SJ Power MOSFET for Pre-rad and After 20 and 50 krad [SiO$_2$] with $V_{DS}$=$V_{GS}$. The Current Compliance of the Instrument Used for Characterization is 0.1A.

Using TCAD device simulation tools form Silvaco and the mid-gap voltage technique, the density of $N_{OT}$ created is extracted at different dose levels. This is listed in Table 0.1. The $V_{BD}$ and $R_{DS,ON}$ were also measured post irradiation but no change was observed in $V_{BD}$ and $R_{DS,ON}$ characteristics.

Table 0.1 Density of $N_{OT}$ and $N_{IT}$ Created in the Gate Oxide and Isolation Oxide Due to TID.

<table>
<thead>
<tr>
<th>TID (krad)</th>
<th>$N_{OT}$ in gate oxide (cm$^{-2}$)</th>
<th>$N_{IT}$ in isolation oxide (cm$^{-2}$)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>5.6x10$^{10}$</td>
</tr>
<tr>
<td>20</td>
<td>2.6x10$^{11}$</td>
<td>2.8x10$^{12}$</td>
</tr>
<tr>
<td>50</td>
<td>4.7x10$^{11}$</td>
<td>2.8x10$^{12}$</td>
</tr>
</tbody>
</table>

According to the device datasheet, the maximum range of $V_{TH}$ allowed for nominal operation of the device is between 2V to 4V. But due to TID, the $V_{TH}$ of the device goes out of specification limit before 20 krad [SiO$_2$] when all device terminals were grounded and before 100 krad [SiO$_2$] when gate terminal was fixed at -1V during exposure. This is shown in Figure 0.10.
Figure 0.10 $V_{TH}$ in 600V SJ Power MOSFET for Different TID Level When $V_{GS} = 0V$ and -1V.

The TID passing criteria for application of power MOSEFTs in space environment is 100 krad $[\text{SiO}_2]$ for common short missions and 300 krad $[\text{SiO}_2]$ for longer missions. Therefore, the tested commercial 600V SJ-MOSFET device is considered to be extremely soft. Thus, in order to qualify for space applications, the device has to be radiation hardened. In the following section, techniques to make SJ-MOSFET rad-hard will be discussed.

3.3 Radiation Hardening Technique

Based on the TID experiment results of 600V commercial N-type SJ-MOSFET, it was concluded the $V_{TH}$ parameter and the leakage current of the device was degraded due to TID. The $V_{TH}$ shift is due to $N_{OT}$ created in gate oxide and increase in leakage current is due to $N_{IT}$ in isolation oxide. Therefore, in order to improve the radiation tolerance of the device, the buildup of $N_{OT}$ and $N_{IT}$ must be significantly reduced. Among the effective ways of improving radiation hardness through processing [71], [72], [73], the addition of nitrides in the gate insulator along with the $\text{SiO}_2$ has shown better results in thin gate
insulators of thickness less than 50nm [74], [75]. Few studies have considered the TID response of nitride-oxide stacks for thickness greater than 50nm [76] and since power MOSFETs have gate oxide thickness of 100nm, the TID response of thicker oxide-nitride stack is examined in this work.

3.4 TID Tolerance of Stacked Si$_3$N$_4$-SiO$_2$ Gate Insulators

3.4.1 Fabrication of Stacked Nitride-Oxide Capacitors

In order to study the TID effect on thicker oxide-nitride stacks, different combinations of metal-nitride-oxide-semiconductor (MNOS) capacitors were fabricated at Arizona State University in the Nanofab cleanroom of class 100 facility. The capacitor stacks were fabricated on a four inch, 525µm thick, Si (100) orientation, p-type wafer which is doped with boron concentration ranging between 4 x 10$^{15}$ to 2 x 10$^{16}$. The SiO$_2$ layer is grown using dry oxidation method in the TYTAN 4600 Mini Furnace system at 1000°C and atmospheric pressure. Prior to oxidation, the wafers were cleaned using industry standard RCA cleaning procedure to remove the native oxides and other particles present on the surface of the wafer. Following SiO$_2$ layer growth, the Si$_3$N$_4$ layer is deposited using low pressure chemical vapor deposition at 1000°C in the same TYTAN 4600 Mini Furnace system. An aluminum gate electrode of 150nm was deposited on the nitride film using Leskar e-beam evaporation tool. Aluminum was also deposited on the backside of the wafer to form the p-silicon substrate contact. Capacitors with different area were patterned using standard photolithography and lift-off techniques, but all the results presented in this dissertation were taken on capacitors with a gate electrode area of 400 µm x 400 µm. Rapid thermal annealing at 380°C for 2 minutes was performed in the forming gas environment to reduce the density of N$_{OT}$ and N$_{IT}$ in the samples prior to exposure.
Figure 0.11 is a representational cross-section of a MNOS capacitor, showing a gate insulator stack of Si$_3$N$_4$ and SiO$_2$ layers sandwiched between an aluminum gate and a p-type silicon substrate. For the purpose of TID testing with different bias conditions during irradiation, all the samples were diced and packaged as shown in the Figure 0.12.

The permittivity of Si$_3$N$_4$ is higher than that of SiO$_2$. Therefore, a thicker nitride layer is required to obtain the equivalent oxide-only capacitance. The equivalent oxide (SiO$_2$) thickness (EOT) for a given nitride thickness is given by

\[ T_{\text{eq,oxide}} = T_{\text{nitride}} \times \frac{\varepsilon_{\text{oxide}}}{\varepsilon_{\text{nitride}}}, \]

where \( T_{\text{eq,oxide}} \) is the EOT for a given a nitride layer, \( T_{\text{nitride}} \) is the actual thickness of nitride layer, and \( \varepsilon_{\text{oxide}} \) and \( \varepsilon_{\text{nitride}} \) are the permittivity of oxide and nitride layers, respectively (\( \varepsilon_{\text{oxide}} = 3.9 \text{F/cm} \) and \( \varepsilon_{\text{nitride}} = 7.5 \text{F/cm} \)). The total EOT for a nitride-oxide stack is given as

\[ \text{Total}_{\text{eq,oxide}} = T_{\text{eq,oxide}} + T_{\text{oxide}}. \]

Table 0.2 lists the different combinations of MNOS capacitors fabricated. The EOT of the insulator regions were chosen to be 80 nm, 100 nm and 120 nm. For comparison against MNOSCAPs, a conventional MOSCAP with 100 nm of SiO$_2$ was also fabricated (sample A) having no nitride deposition in the above-mentioned process.


### Table 0.2 List of Different Oxide-Nitride Stacks Fabricated and Tested at ASU.

<table>
<thead>
<tr>
<th>Sample</th>
<th>SiO$_2$ thickness (nm)</th>
<th>Si$_3$N$_4$ thickness (nm)</th>
<th>Total EOT (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>100</td>
<td>0</td>
<td>100</td>
</tr>
<tr>
<td>B</td>
<td>30</td>
<td>135</td>
<td>100</td>
</tr>
<tr>
<td>C</td>
<td>10</td>
<td>173</td>
<td>100</td>
</tr>
<tr>
<td>D</td>
<td>30</td>
<td>173</td>
<td>120</td>
</tr>
<tr>
<td>E</td>
<td>10</td>
<td>135</td>
<td>80</td>
</tr>
</tbody>
</table>

Figure 0.12 Shows the Packaged Samples (A-E) for TID Testing at Different Bias Conditions Including the Control Samples.

3.4.2 TID Experimental Setup for Stacked Nitride-Oxide Capacitors

The capacitors were irradiated at the Gamma Cell 220 irradiator facility in Arizona State University (shown in Figure 0.13) using the Cobalt-60 gamma rays at a dose rate of 340 rad (SiO$_2$)/min up to a dose level of 450 krad [SiO$_2$]. During irradiation, five different bias conditions (-10V, -5V, 0V, 5V and 10V) were applied to the gate terminal and two devices from every sample were tested for each bias condition. In addition, two capacitors from each stack were left floating during irradiation while the temperature was maintained at room temperature. Electrical characterization was carried out using an Agilent 4284A LCR meter. High frequency capacitance-voltage (CV) characteristics at 1 MHz were measured prior to irradiation and after irradiation doses of 20 krad, 50 krad, 100 krad, 200 krad, 450 krad [SiO$_2$] . The effects of TID can be studied by observing the shift and change
in slope of the CV curves. Irradiations using the same procedure were repeated after 100 days on two un-irradiated capacitor samples from the same wafer lot for each thickness combination to assess whether post-fabrication annealing had any impact on the TID response. The CV characteristics were essentially identical for the later tests. Since there was little difference in the TID response for each capacitor variant, even after a 100-day room temperature anneal, the electrical characteristics of only one device for each combination is shown below.

3.4.3 TID Experimental Results of Stacked Nitride-Oxide Capacitors

Figure 0.14 show the normalized CV curves for all the MOS capacitor samples (sample A – sample E) at different dose levels. The radiation response of sample D showed similar characteristics to sample B and sample E was similar to sample C. The black square, red circle and blue triangle symbols in the Figure 0.14 correspond to pre-rad, 100 krad [SiO2] and 400 krad [SiO2] results, respectively. The TID response of oxide-only sample reveals a significant shift to the left in the CV curve as the dose increases. In addition, the slope of the CV curve in the transition region between C_{max} and C_{min} decreases as TID
increases. The mechanism for this decrease in slope is similar to the cause of increase in S for MOSFETs, i.e., radiation-induced interface traps that build-up near the mid-gap energy of silicon (deep traps). The TID response for MNOS devices shows essentially no shift in the CV curve and no change in slope in the transition region between $C_{\text{max}}$ and $C_{\text{min}}$ as a function of TID. There is also a decrease in the inversion region capacitance as the dose level increases. This characteristic is specific only to MNOS devices. In case of samples B and D, which have an SiO$_2$ thickness of 30nm, at 400 krad [SiO$_2$] the inversion region capacitance reaches the theoretical minimum capacitance. For samples with a 10nm oxide layer (sample C and E), the capacitance at the inversion region, though decreasing as TID increases, still did not reach the theoretical minimum.
Figure 0.14 Normalized CV Characteristics of All the Samples (A-E) for Different Dose Levels.

Figure 0.15 shows the CV hysteresis effect observed in MNOS sample E prior to irradiation. The black squares correspond to a voltage sweep from positive bias to negative bias. The blue circle symbols correspond to a negative to positive voltage sweep. The
hysteresis effect in inversion indicates the presence of spatially distributed shallow interface traps near the conduction band prior to exposure. The trapping and de-trapping of electrons into and out of these traps cause this bias dependence hysteresis. Similar characteristics were observed in all MNOS samples.

![Normalized CV Characteristics of Sample E (10nm Oxide and 135 nm Nitride) Showing Hysteresis Effect at Pre-rad Condition.](image)

Figure 0.15 shows the shift in voltage at the capacitance of 40 pF when different bias values are applied during irradiation. We can observe in all the cases, the oxide-nitride stack has better tolerance to TID than oxide-only sample. In the next section, analyses of the TID behavior of the capacitors are discussed and TCAD simulations are used to support the discussion.
Figure 0.16 Shift in Voltage for All the Samples at Various Bias Conditions for Different Dose Levels.
3.5 Analysis and Discussion

It can be observed that for all MNOS devices, the change in $V_{MG}$ with TID is very small when compared to the response of the oxide-only device. This indicates that using $Si_3N_4/SiO_2$ stacks may provide excellent protection against TID threats in power MOSFETs, which are fabricated with thick gate insulators. Using the mid-gap voltage technique [59], the $N_{OT}$ and $N_{IT}$ densities created for all the samples at different dose levels were extracted. TCAD simulations were used to verify the density of $N_{OT}$ and $N_{IT}$ calculated using mid-gap voltage technique by matching the simulation results to the data. TCAD simulation was performed with Silvaco’s Victory Device software [47].

3.5.1 Effect of Trapped Charge ($N_{OT}$)

When MOS and MNOS devices are irradiated, electron-hole pairs (ehps) are created in both oxide and nitride layers. In MOSCAP (sample A), the electron mobility in the oxide is several times higher than the hole mobility and the lack of barrier between $SiO_2$ and gate electrode causes most of the electrons to transport out of the oxide-only device. On the other hand, many of the holes are trapped in the $SiO_2$ film [77], [78]. Therefore, the net trapped charge in the MOS gate insulator is positive after exposure. This buildup in $N_{OT}$ increases the surface potential and causes the negative voltage shift in the CV curve as TID increases [77], [49]. Figure 0.14 shows the TID response of 100 nm MOS capacitor fabricated and tested at ASU when the device terminals are left at floating bias condition. For this case, the total negative shift at 400 krad [$SiO_2$] dose is around 9V. Figure 0.17 shows the $N_{OT}$ buildup in oxide-only sample for different bias conditions during TID. From the figure it can be observed, the $N_{OT}$ is positive irrespective of the polarity of the bias applied.
In oxide-nitride stack capacitors, depending on the bias applied during irradiation, the generated electrons and holes move either towards the gate terminal or towards the silicon substrate. A fraction of the generated carriers gets trapped at the oxide-nitride interface because of the presence of a high density of electron and hole trap centers at the oxide-nitride interface. Figure 0.18 shows the change in $N_{OT}$ as a function of TID for both MOS and MNOS devices when the device terminals are left floating. It can be observed that for the oxide-only device $N_{OT}$ increases monotonically as TID increases. On the other hand, for all the MNOS samples the $N_{OT}$ change is very small and saturates after 50 krad [SiO$_2$] dose. At 400 krad [SiO$_2$], the $N_{OT}$ created in the MOS capacitors is 20 times greater than the $N_{OT}$ created in MNOS capacitors. The negligible shift observed in the CV curves of MNOS samples can be explained by the offsetting effects of trapped electrons and holes in the oxide-nitride interface and will be discussed below.
Figure 0.19 shows $N_{OT}$ buildup in MNOSCAPs for different bias conditions during TID. In the figure it can be observed, in all the oxide-nitride stacks (sample B – sample E), the $N_{OT}$ buildup is positive when a negative bias or zero bias is applied during TID. On the other hand, $N_{OT}$ is negative when a positive bias is applied during TID.

Figure 0.18 Change in $|N_{OT}|$ vs. TID for Samples Listed in Table 0.2 When the Devices are Left Floating.
Figure 0.19 Change in NOT vs. TID for All MNOS Samples Listed in Table 0.2 for Different Bias Conditions.

Figure 0.20 shows a schematic of the energy band diagram of MNOSCAPs for negative and positive bias conditions, respectively. In the figure, filled squares and circles correspond to electrons generated in oxide and nitride respectively and similarly, unfilled squares and circles correspond to holes generated in oxide and nitride respectively. For the case of -5V and -10V, the electric field will be in the direction pointing towards the gate terminal. Therefore, the electrons of oxide reach Si substrate and the holes in the nitride get trapped either in the nitride bulk traps or reach the gate terminal. However, the holes
generated in the oxide and electrons generated in the nitride will be trapped at the oxide-nitride interface. As a result, the net trapped charges will be positive in MNOSCAPs for the negative bias conditions. For the case of 5V and 10V, the electric field will be pointing towards the silicon interface. Therefore, the holes generated in the oxide will be trapped either in the oxide bulk or at the Si/SiO$_2$ interface and the electrons generated in nitride will be trapped in the bulk nitride due to presence of bulk electron traps in nitride layer. However, the electrons generated in the oxide and holes generated in the nitride layer will get trapped at the oxide-nitride interface due to the presence of electron and holes traps at the interface. As a result, the net trapped charges will be negative in MNOSCAPs for the positive bias conditions. For the 0V bias case, since the intrinsic electric field is small and electrons have higher mobility than holes in oxide and nitride, the net trapped charge is mostly positive.

Figure 0.20 Schematic Energy Band Diagram of MNOSCAPs for Negative and Positive Bias Conditions Showing Balance of Positive and Negative Trapped Charges.

Figure 0.21 show density of additional N$_{OT}$ created for 450 krad[SiO2] total ionizing dose at different bias conditions and for different oxide and nitride thickness
combinations. From the Figure 0.21, it can be observed as the thickness of SiO$_2$ layer increases, N$_{OT}$ density increases independent of nitride layer thickness.

From the Figure 0.22, it can be observed that for $t_{ox}=10$nm, the 135nm $t_{ni}$ stack has higher net N$_{OT}$ because less charges are created when $t_{ni}=135$nm and therefore, there is less charge compensation. When $t_{ox}=30$nm: both $t_{ni}$ stack has similar net N$_{OT}$ because the density of N$_{OT}$ created in SiO$_2$ layer is significantly higher when compared with charges created in nitride layer. As a result, the opposite charge compensation by nitride is independent of the thickness of nitride layer. Therefore, it can be concluded that thickness of nitride layer as less effect on net N$_{OT}$ as the oxide layer thickness increases.
3.5.2 Effect of Interface Traps (N_{IT})

The presence of hydrogen-passivated bonds at the oxide-silicon interface combined with the release of protons and subsequent reactions between protons and the passivated bonds creates interface traps [79]. When the interface traps are spread uniformly throughout the bandgap of silicon, the slope of the CV curve between the maximum and minimum capacitance decreases as N_{IT} increases [49]. From Figure 0.14 (sample A) it can be observed, in addition to the CV shift to the left due to the trapped charges, there is a decrease in the slope of the MOS capacitor CV curve as TID increases, indicating a measurable increase in N_{IT}. This characteristic was observed in MOSCAPs (sample A) for all bias conditions and the density of N_{IT} created was independent of the bias applied during irradiation. This radiation-induced buildup of interface traps in the MOS samples throughout the bandgap of silicon is illustrated conceptually in Figure 0.23. The unfilled square and circle symbols correspond to acceptor-type and donor-type interface traps, respectively.
In Figure 0.14, it can be observed there is no change in the slope of the MNOS samples’ CV curves when the terminals are left floating. This indicates that for all MNOS capacitors there are very few interface traps created after TID, particularly the deep traps with energies within a bulk potential difference of the silicon midgap. This characteristic of negligible $N_{IT}$ buildup was observed in all MNOSCAPs for all bias conditions during irradiation. Using TCAD simulations and the midgap voltage technique [59], the $N_{IT}$ density is extracted for all the samples at different dose levels (pre-rad, 50, 100 and 400 krad [SiO$_2$]) by matching simulations with the data. For these simulations, the interface traps were uniformly distributed across the entire silicon bandgap.

Figure 0.24 shows the change in $N_{IT}$ as a function of TID. Black square, red circle, green upward triangle, blue downward triangle and navy star symbols correspond to samples A-E, respectively, for the case where the terminals are left floating. It can be observed that for the oxide-only sample $N_{IT}$ increases monotonically with dose. For the 400 krad [SiO$_2$] dose level, the increase in $N_{IT}$ for the MOS device is approximately $8 \times 10^{12}$
cm². For MNOS samples there is no change in \( N_{IT} \) as dose increases. The reasons for this enhanced tolerance to \( N_{IT} \) is explained in the next section.

![Graph showing change in \( N_{IT} \) vs. TID for Samples Listed in Table 0.2 When the Devices are Left Floating.](image)

3.5.3 Effect of Shallow Traps in MNOS Devices

In all the MNOS samples, Figure 0.14 (sample B-sample E), an increase in capacitance is observed in inversion (\( V_{GS} > 0 \text{V} \)). This effect may be caused by a high density of shallow interface traps charged when the silicon surface is inverted. This increase in capacitance can be understood using the equivalent circuit model shown in Figure 0.25 [80]. In the figure, \( C_{OX} \) is the oxide-nitride stack capacitance and \( C_S \) is the substrate capacitance formed across the maximum depletion width in silicon during inversion. In the absence of shallow interface traps, the total capacitance of the MNOS devices in inversion is a series combination of \( C_{OX} \) and \( C_S \). When shallow interface traps near the conduction band are present, an additional capacitance \( C_{IT} \) is added in parallel to the substrate capacitance. \( C_{IT} \) is given as [80]

\[
C_{IT} = q * D_{IT},
\]  

(3.11)
where $D_{it}$ is the distribution of shallow interface traps in energy [81]. The existence of this shallow trap distribution in the MNOS devices is consistent with the hysteresis effect observed in Figure 0.15.

![Figure 0.25 Schematic Model for Modified Capacitance Due to Single Energy Level Interface Traps in the MNOS Structure.](image)

The increase in capacitance observed in MNOS samples can be simulated in TCAD by adding acceptor-like interface traps near the conduction band and using the Heiman model [46], [81]. The Heiman model incorporates the exchange of carriers between the channel and the traps located close to oxide-silicon interface [82]. By matching the TCAD simulation results with the data, the total density of spatially distributed acceptor-type interface traps was found to be $4 \times 10^{13}$ cm$^{-2}$ for the pre-irradiated parts. Figure 0.26 compares the pre-rad data and simulation results for sample B (30 nm oxide and 135 nm nitride stack). The filled black square, unfilled blue triangle and unfilled red circle symbols correspond to pre-rad data and TCAD simulation results with and without the Heiman model, respectively. It can be observed there is a close match between the data and simulation using the Heiman model.

Therefore, it may be concluded that high density of shallow acceptor-type interface traps which are spatially distributed in the oxide layer are present in all pre-rad MNOS samples. This is conceptually illustrated in Figure 0.27, which shows the spatial distribution of shallow acceptor-type interface traps in the silicon bandgap. The unfilled square symbols correspond to acceptor-type interface traps. The TID effect on the CV
characteristics for samples A-E is plotted in Figure 0.14. These figure show that the capacitance in the inversion region ($V_{GS} > 0V$) decreases as the dose level increases. This could be due to a decrease in the shallow interface trap density and/or a reduction in the spatial distribution of the traps. This decrease is in stark contrast to the normally observed buildup of interface trap density in MOS devices as the radiation dose increases [83], [81]. In Al$_2$O$_3$ dielectric devices with high density of interface traps, a similar decrease in trap density as TID increased has been reported in previous literatures [84], [85]. To our knowledge, this is the first instance where decrease in interface traps is reported in oxide-nitride capacitors.

![Figure 0.26 Normalized Pre-rad CV Data of Sample B (30 nm Oxide and 135 nm Nitride Stack) and TCAD Simulation Result With and Without Heiman Model.](image_url)

The decrease in interface traps can be related to hydrogen passivation of the spatially distributed interface traps [53]. Protons near the oxide-silicon interface can passivate an already existing interface trap. Because of passivation, both the spatial distribution and the density of interface traps decreases, thereby causing a decrease in capacitance in MNOS devices in inversion [85], [53]. Figure 0.27 shows a conceptual
energy band-diagram of MNOS structure after irradiation which depicts the decrease in the shallow trap density and the reduction in spatial distribution. The unfilled square symbols in the figure correspond to acceptor-type interface traps. From the TID response of MNOS samples with 30 nm SiO$_2$ (sample B and D), it can be observed at 400 krad[SiO$_2$] that the capacitance value in the inversion region reaches the theoretical minimum. On the other hand, in MNOS devices with 10 nm SiO$_2$ thickness (sample C and E), the capacitance value is still higher than the expected minimum. Therefore, it can be inferred that for MNOS stacks with thicker oxides a higher amount of interface trap passivation occurs during irradiation. This may be because more protons are released during irradiation in thicker oxides, thereby causing more hydrogen passivation of dangling bonds at the oxide-silicon interface.

Figure 0.27 Energy Band-Diagram of MNOS Structure Before and After Irradiation Showing the Spatial and Energy Distribution of Shallow Acceptor-type Interface Traps.

3.6 TID Hardened 600V Super-Junction Power MOSFET

In this chapter, TID test results of the commercially available 600V SJ power MOSFET tested at ASU Co$^{60}$ gamma chamber facility was presented. The reason for
degradation (change in threshold voltage and increase in leakage current) was discussed and analyzed. It was observed the DUT failed at 20 krad [SiO$_2$]. The target TID specification for the SJ device to qualify for space applications is typically at least 300 krad [SiO$_2$]. Therefore, the DUT’s radiation hardness level must be improved from 20 krad to 300 krad. Radiation hardening through process was selected as the choice of hardening methodology. In the past, experiments have been conducted on using oxide-nitride stack as a replacement for gate oxide to improve TID hardness in less than 50nm gate insulator devices. Therefore, replacing the oxide layer with oxide-nitride stack was seen as a viable choice to improve the TID hardness of SJ devices which has thick gate oxides.

In this work different combinations of oxide-nitride capacitors were fabricated at ASU cleanroom facility to study the TID response of oxide-nitride stacks as a replacement for thick gate oxides. All the devices were TID tested using a Cobalt-60 source at a dose rate of 340 rad [SiO$_2$]/min up to a total dose 400 krad [SiO$_2$]. A 100 nm oxide-only sample was also fabricated, irradiated and measured. During irradiations, different bias was applied to the samples and the temperature was kept constant at room temperature. CV characterizations were performed at different dose levels. For the oxide-only devices, the CV curves showed significant shifts to the left and decreases in slope as TID was increased, irrespective of the bias applied. On the other hand, less shift in voltage was observed in MNOS devices and the direction of shift was based on the bias applied during irradiation. In all the cases of MNOS samples, no change in CV curve slope was observed.

Using TCAD, the $N_{OT}$ and $N_{IT}$ densities were extracted by matching data with simulation. For the case of 0V applied during irradiation, at 400 krad [SiO$_2$], the change in
NOT in the oxide-only sample is approximately 20 times greater than that of MNOS devices. The significant decrease in NOT created in MNOS samples is due to the trapping of the electrons and holes generated by TID at the oxide-nitride interface and as a result, less charges leave the gate insulator system and hence less device degradation. Similarly, for the case of 0V applied during irradiation, at 400 krad [SiO₂] the increase in N_{IT} in the oxide-only sample is around 8x10^{12} cm^{-2} whereas for MNOS samples, no change in the deep interface traps density was observed. MNOS devices, in the pre-rad condition, exhibited an increase in inversion region capacitance, which may be due to a high density of shallow acceptor-type traps close to the conduction band. The increase in capacitance can be modelled by adding an extra capacitance in parallel to the substrate capacitance. The Heiman model in the Silvaco tool, which spatially distributes the interface traps in the oxide layer is used to simulate the inversion characteristics seen in MNOS devices. Using these simulation results we have identified the likely presence of a high density of spatially distributed acceptor-type traps present in all the MNOS devices at pre-rad conditions. Though the TID response of MNOS samples showed no shift in voltage or change in slope, a decrease in the inversion region capacitance was observed when the samples were irradiated. This may be due to the protons released during irradiation which move towards the oxide-silicon interface where they passivate the already existing Si dangling bonds. Thereby decreasing the density and the spatial distribution of traps in the MNOS parts.

The 10nm SiO₂ and 173nm Si₃N₄ stack combination produced the highest TID tolerance. For this sample, in all the bias cases, the total shift in voltage for a 400 krad [SiO₂] dose level was less than 2V and no significant N_{IT} was generated. Whereas, for the oxide-only sample, when 10V was applied during TID, a 40V shift in CV curve was
observed. Thus, replacing 100nm SiO$_2$ layer in 600V SJ MOSFET with 10nm SiO$_2$ and 173nm Si$_3$N$_4$ stack combination will make the device TID tolerant up to dose level of 400 krad [SiO$_2$], and making the device suitable for space applications.
CHAPTER 4
RADIATION HARDENING AGAINST SINGLE EVENT EFFECTS

Power MOSFET devices have large parasitic capacitances and operate at high voltage and current levels when compared with modern, ultra-scaled CMOS devices [86]. As a result, Single Event Effects (SEEs) from heavy ion strikes that occur in power MOSFETs are more destructive [25], [87], [88], [24]. These effects are Single Event Latchup (SEL), Single Event Burnout (SEB) and Single Event Gate Rupture (SEGR). Power MOSFETs can be protected against heavy ions by either modifying the circuit design of the power electronics or modifying the design of power MOSFET structure. Hardening against SEL in power MOSFETs is achieved by modifying the circuit design [89]. Therefore, when designing power MOSFETs for space applications, SEB and SEGR are the two SEE threats that must be addressed through structural design. In this chapter the SEB and SEGR mechanisms and hardening approaches against heavy ions are discussed.

4.1 Single Event Burnout Mechanism

SEB occurs when a heavy ion strikes the power MOSFET, thereby causing activation and self-continuous operation of the parasitic BJT present in the VDMOS and SJ-MOS structure [25], [26], [27]. Figure 0.1 shows the parasitic NPN BJT present in the n-type SJ-MOSFET, with the source, body and drain acting as emitter, base and collector, respectively. Since the gate and source terminals are tied together in power MOSFETs, it corresponds to emitter and base terminal of the parasitic BJT being externally connected together though a parasitic resistor in the P-body, $R_b$ in the Figure 0.1.
The bias conditions required to cause SEB are: $V_{GS} = 0\text{V}$ and positive bias applied between the drain and source terminals ($V_{DS} > 0\text{V}$). As the heavy ion travels through the power MOSFET (as shown in Figure 0.1), cdps are generated along the ion track, which creates an ionized plasma filament. Due to the applied reverse bias at the drain terminal, the generated electrons move through the N epitaxial layer and reach the drain (collector) terminal. The holes move through the P-body (base) region and are collected at the source (emitter) terminal. As the holes transport, they flow through the resistance $R_b$, creating a voltage drop $V_{BE}$ between the P-body and the source region. Since the body-drain junction is reverse biased from the application of external bias, when there is a sufficient voltage drop to forward bias the body-source junction, the parasitic BJT will be triggered into the forward active mode. This activation of the BJT is the first step in causing the SEB. But in order for SEB to occur, the BJT must sustain in its activation mode operation through feedback mechanisms for a long enough time to create a thermal meltdown in the devices. If the currents are high enough, then it is possible that SEB might not occur even if the parasitic BJT is activated for a short period of time.
When the power MOSFET operates in blocking mode the externally applied $V_{DS}$ bias causes the depletion width to expand in the N epitaxial layer. The device can handle the external bias until the electric field at the blocking junction, formed between N epitaxial layer and the P-body region, reaches the critical breakdown field. Therefore, for $V_{DS} < V_{BD}$, an approximately uniform electric field is present in the epitaxial layer and a higher electric field is present at the N epitaxial layer and the P-body region junction. But when a heavy ion interacts with the device, the depletion region has to expand to accommodate the deposited charge from the heavy ion. Depending on the ehps created and the $V_{DS}$ bias, the depletion region will expand throughout the N epitaxial layer and even into highly doped N+ substrate and P-body region. As a result, the electric field at the blocking junction crosses the critical electric field value, causing impact ionization and avalanche multiplication. This phenomena increases the rate of ehps created and thus, the current
density flowing through the P-body region increases which leads to the larger voltage drop further forward biasing the body-source junction. In this condition, the electrons will start to flow from the source to the drain terminal and if the gain of the parasitic BJT is too high, then the device will be pushed into high injection region. During high injection, the density of electrons flowing through the epitaxial layer is higher than the doping of the region itself and this shifts the depletion region even further into the N+ substrate, causing further increase in impact ionization rate. The holes generated by this impact ionization process causes an additional hole current, which flows through the body (base) region and thereby increasing the electron injection even higher from the source, creating an amplification effect. This positive feedback mechanism pushes the BJT into a self-sustaining operation mode and this sustained high current in the power MOSFET causes burnout to occur. The entire mechanism is shown as process flow in the Figure 0.2. It has been observed that SEB is more prevalent in N-type devices than in P-type devices because electrons and holes have different ionization rates. In silicon, the electron ionization rate is three time more than that of holes ionization rate for a given electric field.
4.2 Single Event Gate Rupture

SEGR is a destructive case of a single event condition which causes permanent damage to the gate insulator layer in the power MOSFETs [86], [88], [90], [26], [91], [92], [93]. Electrical breakdown of the gate oxide is referred as SEGR. It occurs when a heavy ion strikes the power MOSFET, passing through the oxide layer across the neck region (the region in the N- epitaxial layer beneath the gate oxide between the two P-body regions). In a n-type MOSFET, when the device is in off-state bias condition, i.e. $V_{GS}$ is zero or negative and $V_{DS}$ is positive, the charges created by the heavy ion separate due to the electric field. The holes drift upwards towards the gate and the electrons transport towards the drain terminal. Holes are removed from the P-body slowly due to weaker lateral field. Therefore, holes accumulate under the oxide-silicon interface as shown in the Figure 0.3. This accumulation of holes causes an increase in the oxide field. When the field is greater than a critical field, the gate oxide breaks down, creating a conduction path between silicon
and gate electrode. The entire mechanism is shown as process flow in the Figure 0.4. The critical field for a given gate oxide depends on the thickness of the oxide layer.

Figure 0.3 Cross-section of SJMOS Showing Heavy Ion Impact and Hole Accumulation.

The SEGR response in power MOSFETs can be separated into two components, capacitor response and the epilayer response. The capacitor response is the interaction of the heavy ion with the gate insulator, causing dielectric breakdown due to the ion strike. The capacitor response depends on the thickness of the gate oxide, the applied gate bias and the LET values of the heavy ion strike. The epilayer response is the coupling of the drain bias to the transient electrical field in gate oxide, which aids in the SEGR occurrence. When the drain bias is increased, the vertical electric field increases, as a result the hole accumulation under the gate oxide increases. Thus, the SEGR threshold of the power device decreases when the drain bias is increased. The epilayer response depends on the thickness of the substrate region and the range of the heavy ion. Semi-empirical
expressions have been developed for vertical devices that relates the SEGR threshold voltage as a function gate bias, drain bias, gate oxide thickness and LET of the incident heavy ion.

![Diagram of SEGR mechanism](image)

Figure 0.4 Overview of SEGR Mechanism.

4.3 SEE Experimental Setup

The sensitivity of power MOSFETs to SEE can be determined by irradiating with a single energy heavy ion beam. The atomic number and the energy of the ion beam used for the SEE testing depends on the mission requirement of power MOSFET devices. The standardized testing procedure for SEB and SEGR can be found in U.S. Department of Defense Test Method Procedure, MIL-STD 750E Method 1080 test method for SEB and SEGR testing of power MOSFETs [94], [95]. This document provides various test specifications such as fluence of ion beam, test measurement unit and circuit, beam uniformity, resolution of current and voltage measured and the procedure for data collection. The goal of the SEE testing is to determine the safe operating area (SOA) of the
power MOSFET devices. SOA is the plot of highest \( V_{DS} \), at which the device did not undergo any SEE for a particular heavy ion, as a function of \( V_{GS} \).

In this work, 600V N-type SJ-MOSFET was tested at the Lawrence Berkeley National Laboratory facility. The 88-inch cyclotron facility at LBNL provided high energy ion beams with a cocktail of ions up to 30 MeV/nucleon. Table 0.1 shows the characteristics of different ions tested and their corresponding LET and range of penetration of the ions.

<table>
<thead>
<tr>
<th>Ion</th>
<th>Energy (MeV.amu)</th>
<th>LET (MeV.cm(^2)/mg)</th>
<th>Range (µm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>(^{107}\text{Ag})</td>
<td>10</td>
<td>48.15</td>
<td>90</td>
</tr>
<tr>
<td>(^{197}\text{Au})</td>
<td>10</td>
<td>85.76</td>
<td>105.9</td>
</tr>
</tbody>
</table>

Electrical parameters for the power MOSFET, such as, threshold voltage, breakdown voltage, drain current, gate leakage current of devices under test (DUT) were measured using Keithley 2657A and 2635A current-voltage source measurement unit which has greater than 1nA current resolution and Keysight 34970A switching unit was used to switch between multiple test devices. The electrical characteristics of each tested device were measured before and after irradiation. The test was carried out in air and the device surface were placed normal to the ion beam. Figure 0.5 shows the test equipment and test setup with 6 DUT in the LBNL facility. The test was carried out at room temperature with a fluence of \(10^5\) ions/cm\(^2\) and flux of \(5\times10^3\) to \(10^4\) ions/cm\(^2\)/s. The package of the DUT were removed using laser decapsulation technique to ensure the heavy ions can penetrate the entire device thickness.
The testing was initially started with 50% of the maximum rated drain voltage and $V_{GS}=0V$. For SEB testing, the drain current was monitored to identify whether a SEB has occurred. If the DUT survives the applied $V_{DS}$, then the $V_{DS}$ is increased 10V and the SEB test was carried out until the maximum $V_{DS}$ failure voltage for a given $V_{GS}$ is found. During SEGR testing, the gate leakage current is measured to identify the breakdown of gate oxide. If no increase in leakage current is observed, then a post-irradiation gate stress test is performed where $V_{DS}=0V$ and $V_{GS}$ is swept from 0V to 20 V and from 0V to -20V, with each voltage step held for 500ms. If the gate leakage current is still within 100nA of the specification limit of the device, then the device is considered to have no SEGR for that particular $V_{GS}$ and $V_{DS}$ bias. Following this, the $V_{DS}$ is increased by 10V until SEGR is observed. Once the passing and failing $V_{DS}$ is determined for a given $V_{GS}$, the experiment is repeated for different values of gate bias. This process helps in determining the SOA for a heavy ion with particular LET. At each bias point, three devices were tested to identify
any device-to-device variability and the experiment is repeated for different heavy ions. Figure 0.6 shows the testing procedure for both SEB and SEGR.

![Flowchart showing test procedure for SEB and SEGR testing](image)

Figure 0.6 Flowchart Showing Test Procedure for SEB and SEGR Testing [95].

In addition to the heavy ion testing at LBNL, another set of experiments was conducted to compare the performance of VDMOS and SJMOS devices to SEGR. The devices under test were commercially available 650 V silicon planar gate power device. The devices were tested at FNRL JINR, Moscow, Russia using a U-400 cyclotron [96], [97]. The tests were performed with different heavy ions of varying energies to obtain a range of Linear Energy Transfer (LET) values. Table 0.2 lists the ions, energies and
corresponding LETs used in this experiment. The MIL-750 standard testing procedure was followed while testing [95]. The experiment was conducted for different gate-source ($V_{GS}$) bias levels (0V and -10V) and drain-source ($V_{DS}$) biases. The temperature was 25 ± 10 °C.

Heavy ion testing of SJ devices for LET= 45 and 69 MeV cm$^2$/mg was also conducted at different incident angles (0°, 15°, 30°, 45° and 60°) to better understand the effect of the unique SJ P-column on SEGR.

Table 0.2 List of Heavy Ions and Their Characteristics Used During SEE Testing at FNRL JINR Facility.

<table>
<thead>
<tr>
<th>Ion</th>
<th>Energy (MeV.amu)</th>
<th>LET (MeV.cm$^2$/mg)</th>
</tr>
</thead>
<tbody>
<tr>
<td>$^{209}$Bi</td>
<td>10.4</td>
<td>89</td>
</tr>
<tr>
<td>$^{132}$Xe</td>
<td>3.82</td>
<td>69</td>
</tr>
<tr>
<td>$^{132}$Xe</td>
<td>7.76</td>
<td>64</td>
</tr>
<tr>
<td>$^{132}$Xe</td>
<td>19.58</td>
<td>45</td>
</tr>
<tr>
<td>$^{84}$Kr</td>
<td>22.1</td>
<td>20</td>
</tr>
</tbody>
</table>

4.4 SEE Simulation

The TCAD simulator used in this work to simulate the transient effects of heavy ion impact, such as SEB and SEGR on power MOSFET is commercial software called Silvaco Atlas device simulator. Figure 0.7 shows the cross-section of the commercial 600 V planar gate silicon SJ power MOSFET used for this experiment and the device parameters of the planar gate SJ structure used in TCAD simulations are listed in Table 0.3. SJ and VDMOS devices have very similar structural feature except, the lightly doped N-type epitaxial layer in VDMOS is replaced with highly doped alternating P and N columns.
Figure 0.7 SJMOS Cross Section Showing Different Simulated Ion Strike Locations and Cutline Location.

Table 0.3 Parameters of the SJMOS Used for TCAD Simulations.

<table>
<thead>
<tr>
<th>Device parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cell width</td>
<td>12 µm</td>
</tr>
<tr>
<td>Device depth</td>
<td>40 µm</td>
</tr>
<tr>
<td>Oxide thickness</td>
<td>100 nm</td>
</tr>
<tr>
<td>Epitaxial layer doping</td>
<td>$1.76 \times 10^{15}$ cm$^{-3}$</td>
</tr>
<tr>
<td>Epitaxial layer thickness</td>
<td>36 µm</td>
</tr>
<tr>
<td>P-column doping</td>
<td>$5.48 \times 10^{15}$ cm$^{-3}$</td>
</tr>
<tr>
<td>P-column width</td>
<td>2.3 µm</td>
</tr>
<tr>
<td>P$^+$ - plug doping</td>
<td>$2.1 \times 10^{19}$ cm$^{-3}$</td>
</tr>
<tr>
<td>P$^+$ - plug depth</td>
<td>1.85 µm</td>
</tr>
<tr>
<td>P$^+$ - plug width</td>
<td>2.5 µm</td>
</tr>
<tr>
<td>Neck width</td>
<td>5.4 µm</td>
</tr>
</tbody>
</table>
The device simulator solves the drift-diffusion current equations using finite element method. The physical models used in the simulations were those for field mobility, Shockley-Read-Hall recombination, and Fermi-Dirac carrier statistics, Auger recombination and Selberherr impact ionization. The full-width at half maximum radius of the ion track is 0.1 µm. The LET value was assumed constant throughout the ion track. Within the radius of the ion track, the charge generation was assumed constant and dependent on the LET value. Beyond the radius of the ion track, the charge generation follows an exponential decay. The temperature in the simulation was 300 K. The angle of the incident ion was altered by changing the entry and exit point of the ion through the device.

4.4.1 SEB Simulation

When a heavy ion strikes the device, SEB occurs through the activation of the parasitic BJT present in the power MOSFET and this causes an increase in drain current [46]. Figure 0.8 shows the TCAD simulated SEB response of the SJ power MOSFET for two drain bias values (V_{DS}=60 V and V_{DS}=70 V), one passing and the other failing voltage condition. When an LET 86 MeV·cm²/mg ion strikes the SEB sensitive region (V3 in Figure 0.7) and V_{DS} is sufficient to cause SEB, the parasitic BJT turns on and the current will be maintained at a high level as shown in Figure 0.8 with the black up triangle symbols. On the other hand, if V_{DS} is lower than the SEB threshold voltage, the drain current returns to OFF state current and this is indicated as blue down triangle symbols in Figure 0.8.
Figure 0.8 Evolution in Simulation of Drain Current as a Function of Time Following a Heavy Ion Strike of LET 86 MeV cm²/mg in 600V SJMOS Device.

The quasi-stationary avalanche breakdown simulation is another method to predict SEB failure threshold voltages in power MOSFET [91]. The simulated secondary breakdown voltage caused by an avalanche effect in the power MOSFET correlates with the voltage that triggers SEB. Figure 0.9 shows the TCAD simulated secondary breakdown voltage curve of the SJ device and the relationship between secondary breakdown curve and SEB. The curve has three important regions. Region A corresponds to the point when avalanche breakdown is started, and it occurs at the maximum rated voltage of the device. Region B corresponds to the point when the parasitic BJT is turned on. Region C corresponds to the point of secondary breakdown voltage value of the device [91]. In the absence of a heavy ion strike, the MOSFET can survive drain bias up to the region A since the current level is low. But when the interacting heavy ion beam causes the current level to reach above the parasitic BJT turn on current, the MOSFET can survive only up to the secondary breakdown voltage. This is because, if the drain bias is higher than secondary breakdown voltage during heavy ion strike, the device operates in negative resistance.
regime, which permanently destroys the device. In order for a power MOSFET to perform well against heavy ions, it is essential to have high parasitic BJT turn on current and high secondary breakdown voltage value.

![Figure 0.9 TCAD Simulation of Secondary Breakdown Voltage in 600 V SJMOS Device, Showing SEB Failure.](image)

4.4.2 SEGR Simulation

In simulation, SEGR is identified when the maximum transient field \(E_{\text{max}}\) in the gate oxide exceeds the critical oxide electric field and causes oxide breakdown [98], [99]. The \(V_{GS}\) SEGR breakdown value for a given oxide layer thickness and an ion that can cause gate rupture is given by the Titus-Wheatley semi-empirical equation [100] and is shown in Equation 4.1. Using past literature studies, it has been found that for a 100 nm oxide, the critical intrinsic field is \(10^7\) V/cm [98], [101], [24]. Exceeding this value is assumed to cause SEGR. The Titus-Wheatley semi-empirical equation is,

\[
V_{GS} = \frac{E_{\text{critical}} \cdot T_{OX}}{1 + \frac{LET}{53}}
\]  

(4.1)
where, $T_{OX}$ is the thickness of the gate oxide and $E_{critical}$ is the oxide breakdown field. Figure 0.10 shows the SJ planar gate structure response when an LET 86 MeV cm$^2$/mg ion strikes the SEGR sensitive region (V6 in Figure 0.7). The evolution of $E_{max}$ as a function of time following the ion strike for two different drain bias conditions ($V_{DS}=50$ V and $V_{DS}=40$ V) at $V_{GS}=-5$ V, one a passing voltage condition and the other a failing voltage condition, is shown in Figure 0.10. The black up triangle symbols correspond to SEGR failure since the $E_{max}$ crosses the critical field value. On the other hand, the blue down triangle symbols represent no SEGR failure since the $E_{max}$ is below the critical field value.

![Figure 0.10 Evolution of $E_{max}$ in the Gate Oxide as a Function of Time Following a Heavy Ion Strike of LET 86 MeV cm$^2$/mg in 600V SJMOS Device.](image)

4.5 VDMOS vs. SJMOS

The addition of a P-column in SJ power MOSFETs improves the breakdown-$R_{DS,ON}$ tradeoff relation. The reason for this better performance was discussed in Chapter 2. In this chapter, we will compare the SEB and SEGR responses of VDMOS and SJ-MOS devices.
4.5.1 SEB in VDMOS vs. SJMOS

From earlier discussions, it was established that using secondary breakdown voltage characteristics of a power MOSFET is an easy method to determine the SEB threshold voltage of the device. Figure 0.11 compares the secondary breakdown voltage characteristics of VDMOS and SJMOS devices. From the Figure 0.11, it can be observed that the secondary breakdown voltage is the same for both the types of device. The addition of the P-column contributes only to an increase in the primary breakdown voltage (VBD) and has no effect on secondary breakdown voltage. Ikeda et al. [102] showed the SEB experimental results for SJ and VDMOS devices indicating no improvement in tolerance to heavy ions as predicted by the TCAD results.

![Comparison of Secondary V_{BD} in SJMOS and VDMOS Structure.](image)

4.5.2 SEGR in VDMOS vs. SJMOS

Experimental results from previous research have focused only on the SEB results between the VDMOS and SJMOS [103], [102], [104], [50]. In this study, the SEGR experimental results from the heavy ion testing conducted at FNRL JINR, Moscow, Russia
test facility are used to compare the VDMOS and SJMOS responses. SEGR is measured for a 650 V commercial silicon SJ power MOSFET. Technology Computer Aided Design (TCAD) simulations are used to analyze the results and explore the angular dependence for SEGR in the SJ power MOSFET. These results are compared to the heavy ion response of a VDMOS power device to better understand the impact of the SJ P-column on SEGR.

Ion strikes, normal to the silicon surface at locations V1-V7 (Figure 0.7), were simulated. This was done to identify the most sensitive location for normal incident strike in the SJ MOSFET. Figure 0.12 shows the $E_{\text{max}}$ for different strike locations for LET 69 MeV cm$^2$/mg when $V_{\text{GS}}= 0$ V and $V_{\text{DS}}= 60$ V. The worst case occurs when the ion strike is in the middle of the neck region (V6). However, strikes at locations V5 and V7 through the gate oxide also caused the maximum transient field to increase above $10^7$ V/cm. Since V6 is the most sensitive incident strike location, this position is chosen as the entry point for angular heavy ion simulations in further analysis. The simulation was repeated for different LETs and $V_{\text{GS}}$ and the corresponding $V_{\text{DS}}$ at which $E_{\text{max}}$ crosses the 10 MV/cm threshold is recorded as the simulated SEGR failure point for that LET and $V_{\text{GS}}$. 
Figure 0.12 Identification of SEGR Sensitive Region in SJMOS for Vertical Ion Strike Locations. $E_{\text{max}}$ at Different Vertical Ion Strike Locations (V1-V7 as Shown in Figure 0.7) for LET 69 MeV cm$^2$/mg, $V_{GS} = 0$ V and $V_{DS} = 60$ V in SJ Devices.

Figure 0.13 compares the SEGR experimental data and TCAD simulation results when the incident ion strikes are perpendicular to the gate oxide, denoted by symbols and solid lines, respectively. The plot shows the $V_{DS}$ and $V_{GS}$ bias at which SEGR failure occurs for different LET values. For LET = 69 and 89 MeV cm$^2$/mg, the experiment was conducted at $V_{GS} = 0$ V and for LET= 20, 45 and 64 MeV cm$^2$/mg, the experiment was performed at $V_{GS} = -10$ V. These are marked using black square and red circle symbols in Figure 0.13, respectively. The SEGR TCAD simulations were performed for both $V_{GS} = 0$ V and -10 V and are plotted using black and red solid lines respectively. Both the experimental data and TCAD results are in good agreement.
Figure 0.13 SEGR Failure $V_{DS}$ Bias of SJ Device at $V_{GS}=0V$ and -10V for Vertical Ion Strikes at Different LETs.

Figure 0.14 shows the $V_{DS}$ at which SEGR failure occurs in the SJ device and in a commercial VDMOS device for different incident ion angles at $V_{GS} = 0$ V. The black square and blue circle symbols correspond to the SJ and VDMOS device, respectively. The data for the VDMOS device used an ion LET of 40 MeV cm$^2$/mg and was obtained from the work of Nichols, Coss, and McCarty [27]. The SJ data was measured at the U-400 cyclotron in Moscow for an ion LET 45 MeV cm$^2$/mg. A comparison of the SJ and VDMOS data indicates that the SEGR tolerance of SJ device to angular ion strikes is better than that of VDMOS devices. The reason for this difference will be discussed in the next section.
To understand the improved tolerance of SJ devices to angular heavy ion strikes, SEE TCAD simulations were performed for SJ and VDMOS devices for different incident ion angles (0° - 60°). Since the neck region of the device is the most SEGR sensitive, the entry point of ions for all angles was chosen at the middle of the neck region.

The $E_{\text{max}}$ for different angles were found and normalized to $E_{\text{max}}$ at 0°. Figure 0.15 shows the normalized $E_{\text{max}}$ at different incident ion angles and LET = 45 MeV·cm²/mg, $V_{GS} = 0$V and $V_{DS} = 60$ V. The black and red dashed lines correspond to SJMOS and VDMOS devices, respectively. In both SJ and VDMOS devices the worst case SEGR occurs ($E_{\text{max}}$ is highest) when the ion strike is normal to the gate oxide. As the angle of incidence increases the $E_{\text{max}}$ in the gate oxide decreases. Therefore, devices have better tolerance to SEGR when the incident ion is at an angle other than normal to gate oxide [26], [93]. From Figure 0.15, the $E_{\text{max}}$ drops more quickly in SJ devices compared to VDMOS as the ion angle strike increases. This suggests a higher SEGR tolerance in SJ MOSFETs for angular strikes that is consistent with the data in Figure 0.14. But when the
incident ion angle is greater than 30°, the normalized $E_{\text{max}}$ of both SJ and VDMOS start converging and at around 60° incident ion angle, both the curves merge. The simulations were repeated for different LETs for SJMOS and VDMOS devices and similar normalized $E_{\text{max}}$ characteristics were observed for all LETs.

The increased SEGR tolerance in SJMOS can be attributed to the presence of the P-column in SJ devices. Figure 0.16 shows a cross-section of VDMOS device with the depletion layer marked. The SJMOS has an additional P-column which extends the body-drain depletion layer vertically (see Figure 0.7). Figure 0.17 compares the simulated electric field profile of SJ and VDMOS at $V_{GS} = 0$ V and $V_{DS} = 0$ V along the horizontal cutline shown in Figure 0.7 and Figure 0.16. The red and black dashed line corresponds to VDMOS and SJMOS. When the ion strike angle is 10° or greater the ion passes through the SJMOS P-column. The presence of horizontal field in SJMOS (shown in Figure 0.17) created by the P-column prohibits a fraction of holes generated from transporting towards the gate oxide. This causes the concentration of holes accumulated under the gate oxide to
be less for the SJMOS when compared to the VDMOS at strike angles between 10° and 60°. Therefore, the \( E_{\text{max}} \) for SJMOS devices is lower than the VDMOS devices when the ion strike is at an angle in this range.

As the incident ion angle increases (greater than 30°), the portion of the ion track that passes through the depletion layer caused by P-body and N-epitaxial layer (shown in Figure 0.7 and Figure 0.16) increases. Since this depletion layer is present in both types of devices the difference in concentration of holes accumulated under the gate oxide will decrease as the fraction of charge deposited by the ion track. At an ion strike angle of 60° or more, the entire ion track lies within this common depletion layer and thus, the difference in normalized \( E_{\text{max}} \) between SJMOS and VDMOS devices will be significantly reduced as observed in Figure 0.15.

![Figure 0.16 Cross Section of VDMOS Device (Drawing Not to Scale) Showing the Depletion Width. Different Ion Strike Angles (0°, 10°, 15°, 30°, 45° and 60°) are Indicated. The Angles are Distorted Because the Device is Not Drawn to Scale.](image)
SJ power MOSFETs have better tolerance to SEGR when compared with VDMOS devices for non-normal incident strikes. This is because the P-column in SJ device creates an electric field which prevents a fraction of the generated holes from transporting and accumulating under gate oxide. This reduces the $E_{max}$ in the SJ gate oxide. But when the incident ion angle is 60$^\circ$ or greater, the entire ion track passes through the depletion layer created by P-body and N-epitaxial layer, which is present in both SJ and VDMOS devices. Therefore, both SJ and VDMOS have same tolerance to SEGR when incident ion strike angle is 60$^\circ$ or higher. It can be concluded that SJMOS and VDMOS have similar tolerance to SEGR at small and large angles of incidence, but for intermediate angles between 10$^\circ$ and 60$^\circ$, the SJMOS will have better tolerance to SEGR than VDMOS.

4.6 SEE results of 600V SJ MOSFET tested at LBNL

Figure 0.18 shows the SOA of 600V SJ-MOSFET for silver ion and gold ion with corresponding LET of 48 MeV.cm$^2$/mg and 86 MeV.cm$^2$/mg tested at LBNL. When $V_{GS}$=0V, the failure of the device is due to SEB, which is determined by observing the
increase in drain current. For all the other gate bias, SEGR causes device failure which can be observed by an increase in gate leakage current. Using TCAD simulation, the SEB and SEGR for LET 48 and 86 was simulated and from the Figure 0.18, it can be observed there is a very good match between data and simulation. The device tested at LBNL failed due to SEB at $V_{DS}=70\text{V}$ and due to SEGR at $V_{DS}=50\text{V}$ for a gold ion with LET=86. This passing voltage is around 10% of maximum rated $V_{DS}$ of the device.

![Figure 0.18 SOA of the 600V Commercial SJMOS Tested Using Silver and Gold Ion Cocktail With LET 48 and 86 MeV.cm$^2$/mg, Respectively.](image)

The SEB and SEGR passing criteria for power MOSEFTs operating in the space environment is that the device should be able to withstand the gold ion which corresponds to LET 86 at the maximum rated $V_{DS}$ and $V_{GS}$, which is 600V and -20V, respectively, for this technology. Based on the experimental and simulation results, the tested commercial 600V SJ-MOSFET device is considered to be extremely susceptible to heavy ions and if it needs to qualify for space applications, the device has to be radiation hardened. In the following section, techniques to make SJ-MOSFET rad-hard will be discussed.
4.7 SEGR Hardening of Power MOSFET

The tolerance of power MOSFETs to SEGR can be improved by reducing the neck width (distance in a cell between the two p-body regions) for a planar gate structures [26], [105], [106]. Using TCAD simulation, for a 600 V device as shown in Figure 0.7, the neck width needs to be less than 0.4 µm to make the device resistant to SEGR. But when the neck width is reduced this drastically it causes a significant decrease in the drain current of the device as shown in the Figure 0.19 and thereby making the device totally inoperable.

![Figure 0.19 I-V Characteristics of the Initial 600V Commercial Planar Gate SJMOS and the Modified SEGR Hardened 600V Planar Gate SJMOS.](image)

The reason for this drastic decrease in drain current is due to the blocking of the channel by the depletion layer created by p-body and n-epitaxial layer junction. As a result of reducing the neck width, the JFET resistance located between the two P-body increases dramatically causing a significant increase in the drain current as shown in Figure 0.20.
To overcome this problem, the planar gate structure can be replaced with a trench gate structure with the distance between the two p-body regions less than 0.4 µm as shown in Figure 0.21. By changing from a planar to trench gate, the SEGR tolerance can be improved without affecting the electrical characteristics of the device.
4.8 SEB Hardening of Power MOSFET

SEB occurs when the parasitic BJT present in the SJ power MOSFET is activated. Past studies on VDMOS devices have shown that adding a buffer layer between the epitaxial layer and substrate, increasing the dimensions of the P$^+$-plug region and increasing the P$^+$-plug doping improves the SEB tolerance of the device [91], [107], [108]. By adding a buffer layer with an optimized doping concentration, the maximum electric field will decrease. The peak will shift from epitaxial layer-substrate interface to buffer layer-substrate interface and this helps the device to operate at a higher potential. The doping and the thickness of the buffer layer was optimized for the 600V SJMOS using TCAD simulation. An additional method for increasing SEB tolerance is by modifying the P$^+$-plug. The first modification is enlarging the P$^+$-plug under the source diffusion both in lateral and vertical directions. The maximum lateral extension is dictated by the edge of source-channel junction. The reason for this improved performance is that the charge
collecting capacity of the P⁺-plug increases with increasing dimension, thereby reducing
the emitter injection efficiency and current gain of the parasitic BJT. The final hardening
step is to increase the doping of the P⁺-plug, which reduces the emitter injection efficiency
and resistance of the parasitic BJT’s base region. This modification requires more base
current from a higher LET ion to activate the parasitic BJT.

4.9 Single Event Hardened 600V Super-Junction Power MOSFET

All the above-mentioned techniques are used here in conjunction with the trench
gate to improve the SEB and SEGR tolerance of the 600 V SJ device tested at LBNL. The
proposed single event hardened trench gate SJMOS structure is shown in Figure 0.22. By
optimizing the buffer layer thickness, buffer layer doping, P⁺-plug dimensions and P⁺-plug doping, the SEB threshold for LET 86 MeV·cm²/mg has been improved from \( V_{DS} = 60 \text{ V} \) in the generic commercial planar gate SJ structure to \( V_{DS} = 600 \text{ V} \) in the single event hardened trench gate SJ structure. The device parameters of the proposed rad-hard trench
gate SJ structure used in our TCAD simulations are listed in Table 0.4. When compared
with the parameters listed in Table 0.3 for the planar gate structure, the proposed rad-hard
trench gate structure has a buffer layer of thickness 45 µm and doping \( 3.52 \times 10^{16} \text{ cm}^{-3} \).
Also, the dimensions of the P⁺-plug and its doping and the neck width dimension has been
modified.
Figure 0.22 Cross Sectional View of the Proposed Rad-hard Trench Gate 600V SJMOS (Drawing Not to Scale). Perpendicular Ion Strike Locations (V1-V7), Horizontal Ion Strike Locations (H1-H9) and Ion Strike Angles (A1-A9) Are Indicated.

Table 0.4 Parameters of 600V Rad-hard Trench Gate SJMOS Used for TCAD Simulations.

<table>
<thead>
<tr>
<th>Device parameters</th>
<th>Values</th>
</tr>
</thead>
<tbody>
<tr>
<td>Cell width</td>
<td>12 um</td>
</tr>
<tr>
<td>Oxide thickness</td>
<td>100 nm</td>
</tr>
<tr>
<td>Epitaxial layer doping</td>
<td>$1.76 \times 10^{15}$ cm$^{-3}$</td>
</tr>
<tr>
<td>Epitaxial layer thickness</td>
<td>46 um</td>
</tr>
<tr>
<td>Buffer layer thickness</td>
<td>45 um</td>
</tr>
<tr>
<td>Buffer layer doping</td>
<td>$3.52 \times 10^{16}$ cm$^{-3}$</td>
</tr>
<tr>
<td>P-column doping</td>
<td>$5.48 \times 10^{15}$ cm$^{-3}$</td>
</tr>
<tr>
<td>P-column width</td>
<td>2.3 um</td>
</tr>
<tr>
<td>P$^+$ - plug doping</td>
<td>$2.26 \times 10^{19}$ cm$^{-3}$</td>
</tr>
<tr>
<td></td>
<td></td>
</tr>
<tr>
<td>---------------</td>
<td>--------</td>
</tr>
<tr>
<td>P⁺ - plug depth</td>
<td>1.42 um</td>
</tr>
<tr>
<td>P⁺ - plug width</td>
<td>6.5 um</td>
</tr>
<tr>
<td>Neck width</td>
<td>0.3 um</td>
</tr>
</tbody>
</table>

Ion strikes were simulated at different strike locations and at different incident ion angles (as shown in Figure 0.22) to analyze SEGR and SEB susceptibility. The $E_{\text{max}}$ for each simulation ion strike at maximum rated $V_{\text{GS}}$ and $V_{\text{DS}}$, -20V and 600V, respectively, and for LET= 86 MeV cm$^2$/mg are shown in Figure 0.23. In all cases, the $E_{\text{max}}$ remains below the critical oxide breakdown field indicating that no SEGR occurs. This demonstrates that the trench gate device shown in Figure 0.22 has a high SEGR tolerance to energetic heavy ions and is survivable at maximum rated voltages ($V_{\text{GS}}$=-20 V and $V_{\text{DS}}$=600 V) for LETs up to 86 MeV cm$^2$/mg.
Figure 0.23 Maximum $E_{\text{max}}$ for LET 86 MeV cm$^2$/mg, $V_{\text{GS}}$=−20 V and $V_{\text{DS}}$=600 V in Rad-hard Trench Gate SJMOS Device for Different Vertical (V1-V12), Horizontal (H1-H7) and Angular (A1-A9) Ion Strike Locations Shown in Figure 0.22.

Figure 0.24 compares the TCAD simulation results for $E_{\text{max}}$ between the planar gate structure and the proposed trench gate structure due to a heavy ion strike at the most sensitive SEGR location in Figure 0.7 and Figure 0.22, respectively (both worst case for the respective device designs). The modified structure passes at the maximum rated gate and drain voltage for LET= 86 MeV cm$^2$/mg.
Figure 0.24 Evolution in Simulation of $E_{\text{max}}$ in the Gate Oxide as a Function of Time Following a Heavy Ion Strike of LET 86 MeV cm$^2$/mg in the Initial 600V Commercial Planar Gate SJMOS and the Proposed Single Event Hardened Trench Gate SJMOS.

Figure 0.25 shows the evolution of drain current at $V_{\text{GS}} = 0$ V and $V_{\text{DS}} = 600$ V (maximum rated voltage) as function of time after an ion of LET= 86 MeV cm$^2$/mg strikes at 2 ps. In the figure, the red squares correspond to the generic commercial planar SJ power MOSFET and the green circles correspond to the proposed single-event hardened trench gate SJ power MOSFET. The drain current of the generic planar structure remains high indefinitely after the ion strike due to activation of the parasitic BJT, indicating device failure due to SEB. The drain current of the modified trench gate structure returns to pre-ion strike values, which indicates that the device does not fail at the maximum rated drain bias for LET 86 MeV cm$^2$/mg. Figure 0.26 compares the TCAD simulated secondary breakdown voltage curve of the 600V planar gate SJ device (red squares) and the proposed single-event hardened trench gate SJ power MOSFET (green circles). This confirms that the SEB threshold voltage for the proposed trench gate structure is greater than 600V.
Figure 0.25 Evolution in Simulation of Drain Current as a Function of Time Following a Heavy Ion Strike of LET 86 MeV cm²/mg in the Initial 600V Commercial Planar Gate SJMOS and the Proposed Single Event Hardened Trench Gate SJMOS.

Figure 0.26 Simulated Secondary $V_{BD}$ Characteristics of the Initial 600V Commercial Planar Gate SJMOS and the Proposed Single Event Hardened Trench Gate SJMOS.

Figure 0.27 compares the safe operating area (SOA) of the generic commercial planar SJ power MOSFET with the proposed single event hardened trench gate SJ power MOSFET for LET 86 MeV cm²/mg. The figure shows the maximum $V_{DS}$ for surviving the ion strike for different $V_{GS}$ values. The red and green symbols correspond to the planar
gate and the hardened trench gate devices, respectively. The red circle corresponds to the SEE data obtained from LBNL SEE testing of the 600V commercial SJMOS device. The radiation hardened device survives at the maximum rated voltages, illustrating that it is much more likely to survive destructive single event effects (SEE) at LETs up to 86 MeV cm$^2$/mg.

![Graph showing SOA of different devices](image)

Figure 0.27 SOA of the Initial 600V Commercial Planar Gate SJMOS and the Proposed Single Event Hardened Trench Gate SJMOS for LET 86 MeV cm$^2$/mg.

Figure 0.28 and Figure 0.29 compare the un-irradiated $I_{DS}$-$V_{GS}$ characteristics and breakdown voltages characteristics of the 600 V planar gate and the hardened trench gate SJ power MOSFET, respectively. The trench gate structure shows superior sub-threshold current characteristics (e.g., higher sub-threshold slope) and a higher breakdown voltage when compared with the planar device. The improvement observed in sub-threshold characteristics for trench gate structure in Figure 0.28 is due to the effective removal of neck that is present in planar gate device, which contributes to an additional resistance component. This indicates that even the un-irradiated power MOSFET performance is improved by the rad-hard design.
Figure 0.28 Simulated $I_{DS}$-$V_{GS}$ Characteristics of the Initial 600V Commercial Planar Gate SJMOS and the Proposed Single Event Hardened Trench Gate SJMOS.

Figure 0.29 Simulated $V_{BD}$ Characteristics of the Initial 600V Commercial Planar Gate SJMOS and the Proposed Single Event Hardened Trench Gate SJMOS.
CHAPTER 5

CONCLUSION

This work discusses the development of a 600V SJ power MOSFET device which is radiation tolerant to both TID and destructive SEEs. Commercially available 600V SJMOS devices were irradiated using Gamma cell 220 Cobalt-60 irradiator. As a result of irradiation, a decrease in $V_{TH}$ and increase in sub-threshold leakage current was observed in all the devices. The decrease in $V_{TH}$ is due to buildup of $N_{OT}$ in the gate oxide and the increase in sub-threshold leakage current is due to increase of $N_{IT}$ in the inter-device isolation oxide. The maximum range of $V_{TH}$ allowed for nominal operation of the SJMOS device is between 2V to 4V. But due to TID, the $V_{TH}$ of the device goes out of specification before the 20 krad [$SiO_2$] dose level. The TID passing criteria for application of power MOSEFTs in the space environment is 300 krad [$SiO_2$] for typical space missions. Therefore, the tested commercial 600V SJMOS is considered to be radiation soft. In order to qualify for space applications, the device has to be redesigned to be radiation hardened.

In order to make the power MOSFET TID tolerant, a hardening-by-process technique was developed that uses nitrides in gate insulator. In this work, different combinations of oxide-nitride capacitor stacks and a 100 nm oxide-only capacitor were fabricated. All the devices were TID tested using a Cobalt-60 Gamma source up to a total dose 400 krad[$SiO_2$]. During irradiation, different bias conditions (-10V, -5V, 0V, 5V, 10V and floating terminals) were applied to the gate terminal and two devices from every sample were tested for each bias condition. High frequency capacitance voltage (CV) characterizations were performed at different dose levels. For all the MNOS devices and bias conditions, the shift in CV curves is small when compared to the response of the
standard oxide-only device. The smaller shift observed in CV curves of MNOS samples is due to the offsetting effects of trapped electrons and holes present in the oxide-nitride interface. Similarly, for all the MNOS devices with different bias conditions, a negligible change in slope was observed with increasing TID, whereas, for the oxide-only devices, the CV curves showed significant decrease in slope as TID was increased. The negligible change in slope observed in MNOS samples is due to the limited buildup of $N_{IT}$ in the MNOS samples.

The 600V commercial planar gate SJ power MOSFETs were tested for SEB and SEGR effects using silver ion and gold ion that correspond to LETs of 48 and 86. Two devices were tested for each failure and passing point. The MIL-750 standard testing procedure was followed while testing. The failure due to SEB is confirmed by observing the spike in drain current and the failure due to SEGR is confirmed by observing the increase in gate current due to gate oxide breakdown. For LET 86 MeV.cm$^2$/mg, the device failed due to SEB at $V_{DS}=70$V and due to SEGR at $V_{DS}=50$V. This passing voltage is around 10% of maximum rated $V_{DS}$ of the device. The required SEB and SEGR passing criteria for application of power MOSEFTs in space environment is that the device should be able to withstand the gold ion which corresponds to LET 86 MeV.cm$^2$/mg at maximum rated $V_{DS}$ and $V_{GS}$, which is 600V and -20V respectively. Therefore, the tested SJMOS device is considered to be extremely susceptible to heavy ions and if it needs to qualify for space applications, the device has to be made SEB and SEGR hardened.

In this work, single event hardening techniques for a 600V SJ power MOSFET were identified through TCAD simulations. The simulation accuracy for the base-line
planar device structure was validated via comparisons to experimental data. The SEGR tolerance of SJMOS can be improved by reducing the neck width to less than 0.4 µ. This can be achieved using trench gate SJ power MOSFET instead of planar gate devices. Adding a buffer layer and increasing the doping, thickness and width of the P+-plug improves SEB tolerance. The SEB and SEGR on the optimized trench gate SJ structure and the commercial SJ structure was analyzed and simulated using TCAD.

My major contributions are 1) proposed 10nm oxide and 173nm nitride stack combination as a replacement for thick insulators in power MOSFETs that are tolerant to TID. For this sample, in all the bias cases, the total shift in voltage for a 400 krad [SiO₂] dose level was less than 2V and no significant NIT was generated. Thus, replacing 100nm SiO₂ layer in 600V SJ MOSFET with 10nm SiO₂ and 173nm Si₃N₄ stack combination will make the device TID tolerant up to dose level of 400 krad [SiO₂], thereby making the device suitable for space applications. 2) proposed single-event hardened trench gate SJ power MOSFET showed a more than 10X improvement is SEB and SEGR. Although the complexity in processing of radiation trench gate devices is greater when compared to planar gate devices, the proposed device design significantly improves tolerance to destructive single event effects and improves the device electrical performance.
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