TEM Characterization of Electrically Stressed
High Electron Mobility Transistors

by

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ABSTRACT

High electron mobility transistors (HEMTs) based on Group III-nitride heterostructures have been characterized by advanced electron microscopy methods including off-axis electron holography, nanoscale chemical analysis, and electrical measurements, as well as other techniques. The dissertation was organized primarily into three topical areas: (1) characterization of near-gate defects in electrically stressed AlGaN/GaN HEMTs, (2) microstructural and chemical analysis of the gate/buffer interface of AlN/GaN HEMTs, and (3) studies of the impact of laser-liftoff processing on AlGaN/GaN HEMTs.

The electrical performance of stressed AlGaN/GaN HEMTs was measured and the devices binned accordingly. Source- and drain-side degraded, undegraded, and unstressed devices were then prepared via focused-ion-beam milling for examination. Defects in the near-gate region were identified and their correlation to electrical measurements analyzed. Increased gate leakage after electrical stressing is typically attributed to “V”-shaped defects at the gate edge. However, strong evidence was found for gate metal diffusion into the barrier layer as another contributing factor.

AlN/GaN HEMTs grown on sapphire substrates were found to have high electrical performance which is attributed to the AlN barrier layer, and robust ohmic and gate contact processes. TEM analysis identified oxidation at the gate metal/AlN buffer layer interface. This thin $a$-oxide gate insulator was further
characterized by energy-dispersive x-ray spectroscopy and energy-filtered TEM. Attributed to this previously unidentified layer, high reverse gate bias up to $-30 \text{ V}$ was demonstrated and drain-induced gate leakage was suppressed to values of less than $10^{-6} \text{ A/mm}$. In addition, extrinsic $g_m$ and $f_t \cdot L_G$ were improved to the highest reported values for AlN/GaN HEMTs fabricated on sapphire substrates.

Laser-liftoff (LLO) processing was used to separate the active layers from sapphire substrates for several GaN-based HEMT devices, including AlGaN/GaN and InAlN/GaN heterostructures. Warpage of the LLO samples resulted from relaxation of the as-grown strain and strain arising from dielectric and metal depositions, and this strain was quantified by both Newton’s rings and Raman spectroscopy methods. TEM analysis demonstrated that the LLO processing produced no detrimental effects on the quality of the epitaxial layers. TEM micrographs showed no evidence of either damage to the $\sim 2 \text{ μm}$ GaN epilayer generated threading defects.
This dissertation is dedicated to my mother, Shirley, and to the memory of my father, Darrell; their encouragement and love made this achievement possible.
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1.1 Background and Motivation

Wide bandgap semiconductors are receiving increased attention due to several compelling performance advantages over more established semiconductor technologies. The high electron mobility transistor (HEMT), a member of the broader class heterojunction field effect transistor (HFET), is a heterostructure device which advantageously combines a wide bandgap material with a narrower bandgap material. The HEMT is characterized by a highly conductive channel formed by a two-dimensional electron gas (2DEG) near the interface between the two materials. Group III-nitride HEMT technology enables high frequency and high power performance superior to that of GaAs-based HEMTs as a direct result of the larger energy bandgap, large conduction band offset, and concomitant low ionization coefficient and high breakdown voltage. Commercial AlGaN/GaN HEMT devices are already being produced for operation in the X- and K-band (8-12 GHz and 12-18 GHz, respectively) while K-band (27-40 GHz) devices are presently under development. Furthermore, InGaN/GaN- and InAlN/GaN-based HEMT devices promise to extend operating frequencies to 100 GHz and beyond.

After an initial spate of activity in the early 1990s, the relatively nascent GaN technology has undergone considerable recent development. Two critical advances occurred during that early period. First, a means for achieving p-type doping was discovered by Nakamura, thus enabling practical blue and ultraviolet
(UV) light-emitting diode (LED) and laser diode (LD) devices. Second, Khan et al. (1992) successfully demonstrated an AlGaN/GaN heterostructure exhibiting a 2DEG, thus stimulating interest in Group III-nitrides for other device applications. Beyond the remarkable transport properties of a 2DEG device, the wide energy band gap of the Group III-nitrides affords high breakdown voltage and high saturation carrier velocity. These three properties are particularly advantageous for high voltage devices and also for high frequency applications, both of which are described later in more detail. The 2DEG in these material systems arises from superposition of the spontaneous polarization inherent to the wurtzite Group III-nitride materials, and piezoelectric polarization induced by lattice-mismatch strain between the two heterostructure constituents. Resulting 2DEG sheet charge densities exceeding $2 \times 10^{13} \text{ cm}^{-2}$ have been reported, and this value exceeds that obtained with GaAs-based systems by at least a factor of four.

Before the potential of Group III-nitride HEMTs can be fully realized several issues must be resolved:

- **Substrates:** Whereas GaAs- or Si-based devices have available large (150 mm diameter or larger) substrates of native material, development of GaN substrates of practical size has proven problematic. Early HEMT research was performed using sapphire substrates and these are still commonly used. However, sapphire presents problems for lattice mismatch (as well as poor templating of
the epitaxial layers), mismatch of thermal expansion coefficients and poor thermal conductivity. SiC substrates are superior to sapphire substrates in most performance areas but are significantly more costly. Despite the large lattice mismatch, Si can be used if suitable buffer/transition layers are incorporated. However, defectivity of the epitaxial layers remains high.

- Metal Contacts: Ohmic contacts for GaN-based devices have improved considerably in recent years but research to reduce contact resistance continues to be a very active area of research. Schottky contacts on GaN-based devices are subject to unacceptably high leakage current under electrical stress conditions.\textsuperscript{9,10}

- Current Collapse and Dispersion: A phenomenon known as current collapse often occurs in Group III-nitride HEMT devices. This effect is characterized by a decrease of the saturation current at high values of $V_{ds}$ with a concurrent increase in the knee voltage. Another manifestation of the phenomenon is dispersion between DC and pulsed measurements and/or reduced RF output power.\textsuperscript{11-13}

Group III-nitride HEMTs have lately re-emerged as serious leading contenders for high power, high frequency applications, even though there are other practical issues remaining to be resolved such as compatible materials for metallization, passivation dielectrics, and device integration. As functional
electronic devices have been fabricated and electrical performance evaluated, issues related to HEMT reliability have been identified as requiring closer attention. A wide range of techniques has been used to identify, define, and understand degradation and failure mechanisms in GaN HEMTs. Electrical measurements such as (pulsed) I-V, leakage, and deep-level transient spectroscopy (DLTS) are routinely performed. These measurements directly evaluate device performance and can often provide useful insights regarding failure and reliability issues. However, they fail to provide a complete picture of longer term device behavior.

Accelerated life testing (ALT) is commonly used to establish reliability. For example, mean-time-to-failure (MTTF) values of $10^7$ hours at a junction temperature of 150 °C have recently been reported for GaN HEMT devices operating at 40 V. However, as the performance envelope for these devices is expanded, especially for high frequency and high power applications, methodologies for accelerated life testing have not yet been fully evaluated. Relatively high activation energies of up to 2 eV have been reported, but applicability to the reliability of fielded GaN HEMTs has not yet been determined. Thus, degradation mechanisms are currently being assessed and the challenging task of identifying assignable causes is ongoing.

The present ambiguity associated with the primary degradation drivers does not allow device reliability to be predicted or specified with sufficiently high levels of certainty. A better understanding is needed of which physical
mechanisms play major roles in temperature-accelerated testing, and quantitative measures of the validity and usefulness of MTTF values are required. Failure mechanisms dependent on hot electron effects have been postulated, similar to the situation for III-V FETs. Hot electrons may be trapped in the AlGaN (or barrier) or buffer layers, at the Si$_x$N/AlGaN (or dielectric/barrier) interface, or even inside the Si$_x$N (or dielectric). Alternately, hot electrons may contribute to the formation of traps at these locations. Although hot electrons appear to play a role in device degradation, the relative importance of that role is still unclear. One characteristic of hot-electron degradation is an exponential dependence proportional to $(V_{DS} - V_{DS,\text{sat}})^{-1}$, but this has not yet been observed. Similarly, correlation with gate current, as observed in Si MOSFETs, GaAs HEMTs, and InP HEMTs, has not been demonstrated. Evidence is accumulating for a reliability mechanism that also involves defect formation but through the inverse piezoelectric effect.

For elucidating the link between electrical performance, particularly ALT and reliability test data, and the underlying degradation and failure mechanisms, characterization techniques are required that can provide microstructural and microanalytical information, preferably with sub-micrometer or better lateral resolution. Several techniques, such as scanning electron microscopy (SEM) and atomic force microscopy (AFM), provide imaging and topographical information. However, these techniques do not afford the desired subnanometer-scale lateral resolution that is crucial for identifying defects and other factors that often impact
device performance and reliability. The transmission electron microscope (TEM) combines imaging and electron diffraction for microstructural analysis as well as energy-dispersive x-ray spectroscopy (EDXS) and electron-energy-loss spectroscopy (EELS) for analytical purposes. More specialized techniques, such as energy-filtered imaging and electron holography, are also available which can provide an even more comprehensive picture of the device regions or materials of interest. These TEM capabilities, especially as they relate to developing a better understanding of device reliability for Group III-nitride HEMTs, are the basis for most of the results presented in this dissertation.

1.2 Nitride HEMT Materials

The Group III-nitrides have long presented a strong potential for realizing optoelectronics applications in the blue and UV wavelengths, but they also offer attractive properties for other types of devices, particularly HEMTs. Of the Group III-nitrides, GaN has been studied most extensively and was first synthesized in 1932 as small needles and platelets by Johnson et al. The achievement of Maruska and Tietjen (1969) of growing a layer of significantly greater area on a sapphire substrate ushered in the first GaN research for semiconductor devices: initially for bulk GaN in the 1960s, then for the development of epitaxial growth techniques in the 1980s.32
1.2.1 Crystallography and Basic Properties

Although Group III-nitrides occur in each of the rock-salt, zincblende, and wurtzite crystal structures, the last of these is by far the most common and currently of most interest for electronics applications. Wurtzite is the thermodynamically preferred structure at and near standard temperature and pressure for AlN, GaN, and InN.\textsuperscript{32-34} The enthalpies of formation for AlN and GaN (see Table 1.1) indicate that their temperature stability is superior to that of other semiconductors, which has positive implications for both high temperature processing and high temperature operation. Also of note are the high breakdown voltages for AlN and GaN (as well as SiC) due to the lower impact ionization coefficient of those materials. Saturation velocities are higher and, although the bulk mobilities are lower, when a two-dimensional electron gas is formed in Group III-nitride heterojunctions, the electron mobilities obtained are 2000 cm\(^2\)(V\(\cdot\)s\(^{-1}\)) or higher, which is superior to Si.
Wurtzite is a hexagonal crystal structure for binary compounds corresponding to space group P6₃mc (C₆ᵥ), comprising two interpenetrating hexagonal-close-packed (HCP) sublattices, as shown in Fig. 1.1. Consider a wurtzite crystal composed of elements A and B. Each of the two elemental constituents of the binary compound is represented by one of these sublattices. Sublattice A is offset from sublattice B by 3/8 of the cell height along the c axis. Each element A atom is tetrahedrally coordinated with atoms of element B and conversely. The ratio $c/a$ of the lattice parameters is $\sqrt{8/3}$. The foregoing describes the crystallographic relations for an ideal wurtzite structure; actual wurtzite materials deviate slightly from these ideal values.
1.2.2 Spontaneous and Piezoelectric Polarization

The wurtzite structure is non-centrosymmetric, lacking inversion symmetry along the $c$-axis ([0001]) direction. Consequently, wurtzite crystals exhibit electrical polarization along this axis. This effect is termed spontaneous polarization, because it manifests in the absence of external stress. Considering specifically the Group III-nitrides, the difference in electronegativity between the Group III elements (with the exception of boron) and nitrogen is 1.2-1.4, indicating the significant ionic character of the Group III-N bond. As a result of these two factors, it is predicted that a large polarization field parallel to the $c$-axis will be induced microscopically and also manifest as a macroscopic polarization.\textsuperscript{37} As early as 1998, photoluminescence measurements confirmed the presence of polarization-induced built-in electric fields with strengths of 2 MV/cm and higher in AlGaN/GaN and InGaN/GaN quantum wells.\textsuperscript{38-40}
Table 1.2. Calculated polarization coefficients for the Group III-nitride materials.37

Piezoelectricity is characterized by a change in the electrical polarization of a material, most commonly associated with strain. The piezoelectric tensor of each of the wurtzite Group III-nitrides, InN, GaN, and AlN, has three independent components—two of which, $e_{31}$ and $e_{33}$, represent the piezoelectric polarization resulting from strain along the $c$-axis. The piezoelectric polarization, $P_{PE}$, is given by

$$P_{PE} = 2 \frac{a-a_0}{a_0} \left( e_{31} - e_{33} \frac{C_{13}}{C_{33}} \right),$$  \hspace{1cm} (1)$$

where $a_0$ and $a$ are lattice constants in the basal plane for the relaxed and strained crystals, respectively; and $C_{13}$ and $C_{33}$ are elastic constants.41 The total polarization is the sum of the spontaneous and piezoelectric polarization.

The spontaneous polarization coefficient, a parameter which characterizes the strength of the spontaneous polarization electric field, is much higher for the AlGaN barrier than for the GaN buffer. Due to the differences in lattice constants
of both layers, AlGaN barriers pseudomorphically grown on GaN are under
tensile strain, resulting in piezoelectric polarization. The discontinuity of the total
polarization at the heterointerface (due to spontaneous and piezoelectric
contributions) gives rise to a fixed positive electrostatic polarization charge $\rho_p$
given by\textsuperscript{41,42}
\[ \rho_p = -\nabla P. \quad (2) \]

The corresponding two-dimensional polarization charge density $s$, is given by

\[ \sigma_{AlGaN/GaN} = P_{GaN} - P_{AlGaN} \]
\[ = (P_{GaN}^{sp} + P_{GaN}^{pz}) - (P_{AlGaN}^{sp} + P_{AlGaN}^{pz}). \quad (3) \]

Figure 1.2 illustrates the relationships between polarization fields and
2DEG locations for different heterostructure material systems and for both growth
polarities for the bottom GaN.\textsuperscript{41,42}
1.2.3 Energy Band Structure

The bandgap energies of AlN, GaN, and InN are 6.2 eV, 3.4 eV, and 0.7 eV, respectively. Ternary variants of these basic binary compounds thus enable bandgap engineering over the range 0.7 eV to 6.2 eV using Group III-nitride materials. These materials are of particular interest as wide band gap materials, where “wide band gap” is generally understood to refer to bandgap energies beyond those of the conventional semiconductors: Si (1.12 eV) and GaAs.

\footnote{The bandgap of InN was long held to be \( \sim 1.9 \) eV but following the work of Davydov et al. (2002) it is accepted to be the lower value 0.7 eV.}
(1.42 eV). The wurtzite Group III-nitrides, including alloys of the representative binary compounds, are direct gap semiconductors, giving them a clear advantage over indirect gap semiconductors such as Si, Ge, and SiC, for optoelectronic applications.

Polarization-induced fields cause a reduction of the effective band gap as a result of quantum-confined Stark effect\textsuperscript{43} and Franz Keldysch effect,\textsuperscript{44} which in turn causes a red-shift of the optical absorption and emission spectra.\textsuperscript{45}

1.2.4 Heterostructures and 2DEG

Structures comprising two dissimilar semiconductors in intimate contact—almost invariably one layer grown or deposited upon the other—are known as heterostructures. Heterostructures are often used in device applications where the difference in energy band gaps across the interface between the two materials is used advantageously in various ways for applications such as photovoltaic devices, semiconductor lasers, and the subject of this work: HEMTs. A schematic diagram of an exemplary HEMT based on a Group III-nitride material system is depicted in Fig. 1.3. Because Group III-nitride HEMTs are often used for high power applications, it is necessary to mitigate the effects of high local fields in the active area of the device. The field plate structure which extends from the source side over the gate effectively helps to distribute the electric field over channel area thereby reducing its magnitude in peak field locations. Shown in Fig. 1.4, the bandgaps of the Group III nitrides—AlN, GaN, and InN—span a large range of energy, potentially covering the region from 0.7 eV to 6.2 eV.
Fig. 1.3. Schematic cross-sectional diagram of an AlGaN/GaN HEMT.

Fig. 1.4. Energy band gap as a function of lattice constant for Group III-nitrides and other, representative semiconductors.
1.2.5 Substrates for Epitaxial Growth

The ideal substrate for epitaxial growth of III-nitride layers is native, freestanding GaN. However, this is still not a practical alternative primarily due to the difficulty in growth of a GaN crystal boule related to the low solubility of nitrogen in liquid Ga and the high vapor pressure of nitrogen over GaN. AlN is marginally better in terms of nitrogen solubility and vapor pressure but still suffers from the same problems as GaN for bulk growth. Despite difficulties associated with lattice mismatch and thermal incompatibility, sapphire was the first substrate widely used for this purpose and is still in widespread use. Although (0001)-oriented (c-plane) sapphire substrates have been by far the most common, (21\overline{3}1)-, (1\overline{1}02)- (m-plane), and (11\overline{2}0)-oriented (a-plane) wafers have also been used. Other substrates that have been employed for Group III-nitride epitaxy include GaP, InP, LiAlO$_2$, LiGaO$_2$, MgAl$_2$O$_4$, MgO, NaCl, Si, SiC, TiO$_2$, and ZnO. Of these, Si and SiC are most prevalent. Although SiC offers considerably smaller lattice mismatch and better thermal compatibility as compared to Si and sapphire, its use is cost-prohibitive for many applications and problems persist with the quality of both the bulk crystal and surface finish.$^{32}$

1.2.6 Epitaxial Growth Techniques

Maruska and Tietjen (1969) produced the first single-crystal epitaxial GaN film using hydride vapor phase epitaxy (HVPE). HVPE deposition of GaN typically involves flowing the precursors NH$_3$ and GaCl (formed by flowing HCl
over a Ga melt) in a carrier of purified N₂ with the substrate temperature elevated to ~1100°C, according to the reaction:

\[
GaCl + NH₃ \Rightarrow GaN + HCl + H₂. \tag{4}
\]

This technique is characterized by relatively high growth rates which tend to run counter to the requirements for epitaxial growth: if arrival and surface reaction rates increase they must be balanced by increased surface mobility.

Metal-organic chemical vapor deposition (MOCVD) is a refinement of HVPE in which the precursors take the form of organic compounds or metal-organics and metal hydrides. The precursors are flowed over a substrate heated to ~1000°C, react with each other, and the organics leave the substrate through pyrolytic decomposition. In the case of Group III-nitrides, the Group III precursor normally takes the form of trimethylaluminum (TMA), trimethyngallium (TMG), or trimethylindium (TMI), or their triethyl analogs. The nitrogen precursor is often NH₃ but may also be phenyl- or dimethyl-hydrazine.

Molecular beam epitaxy takes place at a pressure of 10⁻¹⁰ torr or lower. MBE deposition rates are characteristically low, typically less than 1 μm/h, which allows the films to grow epitaxially at significantly lower temperatures than with MOCVD and HVPE—commonly 650 °C to 800 °C. However, the lower growth rates also necessitate lower pressures in order to maintain levels of unintentionally incorporated impurities similar to other deposition techniques. MBE growth of Group III-nitrides employs an ultra-pure Al, Ga, and/or In source as required.
This metal source is heated to beyond its sublimation temperature in a Knudsen effusion cell, forming a directed beam of the element(s) which is trained on the substrate. Ultra-pure molecular nitrogen may serve as a precursor but it does not chemisorb on GaN below 950 °C due to the strength of the N-N bond. If molecular nitrogen is the precursor, a means for dissociating the molecule (e.g., electron cyclotron resonance (ECR) plasma) must be used. Alternatively, nitrogen-containing compounds having more weakly bonded nitrogen are used.

1.2.7 Microstructure

The lack of a native, freestanding GaN or otherwise lattice-matched substrate for GaN epitaxy has direct and obvious implications for the quality of those epitaxial layers and the performance of electronic and optoelectronic devices which incorporate them. In order to accommodate lattice-mismatched substrates, it is important to consider each of the substrate material and crystallographic orientation, buffer/transition layer inclusion prior to Group III-nitride growth, and growth conditions for subsequent deposition of epitaxial layers. Early research into GaN epitaxy was typically performed on sapphire substrates. By growing GaN on a hemispherical sapphire substrate, Madar et al. (1977) established a comprehensive set of relationships between substrate orientation and the quality of the epitaxial layers grown on them. Although the best overall quality was observed for (0001) sapphire, it was found that superior surface morphology was obtained for (11̅20) sapphire tilted ~15 toward the [1̅100] axis.
The most common defects introduced into the Group III-nitrides during growth are dislocations, impurities, and point defects.\textsuperscript{48} Dislocations initially occur at the GaN heterointerface due to lattice mismatch between the substrate and GaN, and due to the GaN grain structure. To the extent that these dislocations propagate into the GaN away from the interface, they are called threading dislocations (TDs). Dislocation densities in GaN typically range from $10^8$ to $10^{10}$ cm$^{-2}$, mostly independent of the growth technique used (other than HVPE). Such high defect densities would wreak havoc in Si and GaAs systems, particularly for optoelectronic and photovoltaic applications for which relatively long carrier recombination lifetimes are critical, yet still allow acceptable LED performance for Group III-nitride materials operating at or above wavelengths of 400 nm.

In contrast to the lattice-strain-induced TDs, the appearance of impurities and point defects is governed by the processing conditions, both during epitaxial growth and subsequent annealing. These defects adversely impact device performance by generating mid-bandgap traps, especially those at deep energy levels and also by creating current leakage pathways. Traps are particularly deleterious in the context of high frequency performance. For GaN HEMTs, the appearance of traps in proximity to the 2DEG is highly undesirable, since for a HEMT to work properly the GaN must be insulating enough to restrict current flow to the 2DEG layer and not allow conduction in parallel through the bulk GaN. However, if the semi-insulating GaN is excessively resistive, the occurrence of traps in the GaN is more probable.\textsuperscript{47}
Bulk GaN substrates could reduce or ideally eliminate the influence of trapping type defects on HEMT performance, especially traps associated with dislocations. However, the operating junction temperatures of HEMTs are greater than 200 °C, which can still lead to device breakdown and loss of linearity. This suggests that active cooling of the devices is potentially as important as reducing the influence of traps. Because SiC has a high thermal conductivity and is closely lattice-matched to GaN (3.5% difference) and AlN (< 1% difference), SiC is the best substrate for GaN HEMTs. The GaN HEMTs with the best power performance to date have been grown on SiC.

1.2.8 Doping

Historically, epitaxially grown GaN layers have been characterized by an unintentional, background $n$-type doping. This unintentional doping was originally attributed to N vacancies which contributed a shallow donor level in GaN (and InN). Until recently, the degree of background $n$-type doping effectively precluded the realization of $p$-type doping in GaN. An ab initio study by Mattila and Nieminen (1996) predicted that O point defects in GaN would create a shallow donor level that could also explain the $n$-type background.48

A prerequisite for the majority of electronic devices is a semi-insulating layer upon which the active layers can be epitaxially grown using the techniques previously mentioned. This has been a problem for GaN due to the lack of a native substrate. Because the substrate—here defined as the layer upon which the GaN is grown, but not necessarily the wafer substrate—does not share the
stoichiometry of the GaN layer, the GaN may be subject to autodoping: the incorporation of substrate elements as dopants, particularly during high temperature processing. Depth profile Hall measurements of the carrier densities in unintentionally doped GaN\textsuperscript{49} provide evidence that the unintentional \textit{n}-type conductivity appears predominantly in the region near the interface of the GaN with, in that case, the sapphire substrate. More recently, scanning capacitance microscopy (SCM) analyses of similar GaN/sapphire interfaces confirmed that the unintentional \textit{n}-type conductivity occurs primarily in the near-interface region, while secondary ion mass spectrometry of comparable samples identified oxygen incorporation as responsible for the background \textit{n}-type conductivity\textsuperscript{50} The SCM results were independently corroborated for nonpolar \textit{a}-plane (11\overline{2}0) GaN grown on \textit{r}-plane (\overline{1}0\overline{2}) sapphire [Zhu et al., 2010]. Typical MOCVD growth of GaN on sapphire proceeds by three-dimensional island growth followed by coalescence into a two-dimensional layer (3D-2D growth).\textsuperscript{51} The extent of unintentionally incorporated O can be significantly reduced by instead manipulating the process conditions to maintain 2D layer growth. However, the penalty to be paid is increased dislocation density.\textsuperscript{52} Measured carrier concentrations for unintentional \textit{n}-type doping in these studies were on the order of 10\textsuperscript{18} cm\textsuperscript{-3}.

1.3 HEMT Devices

The defining feature of a HEMT is the 2DEG that is formed on one side of the heterointerface. The terminology for electronic devices has evolved over time
as new materials are (re)introduced, novel structures attempted, etc. and this is certainly applicable to HEMTs. The HEMT belongs to the general class of field effect transistor (FET). Because it takes advantage of the juxtaposition of different epitaxial material layers, the HEMT is also a member of the heterojunction FET (HFET) subclass of FETs and is sometimes referred to by this more general term. There is a further division of HEMT into modulation-doped FET (MODFET) and undoped channel HEMT; the distinction will be explained further in the next section.

1.3.1 Device Structure

Transistors, whether of the bipolar or field effect variety, are three-terminal devices and the HEMT is no exception. The HEMT is characterized by a heterojunction which enables the formation of a 2DEG conduction channel. The terminals on either end of this channel—the source and drain—are formed with ohmic metal systems, while the contact in proximity to but not in contact with the channel, is termed the gate and is formed using metal systems that produce a Schottky contact.

The earliest example of a HEMT, known as a MODFET, or modulation-doped FET, was demonstrated in 1978. This device was based on a modulation-doped AlGaAs/GaAs superlattice. One year later, a MODFET comprising a single AlGaAs/GaAs heterojunction was reported. In each of these devices, the higher bandgap material—the AlGaAs—was doped and carriers derived from the dopants transferred to the heterointerface, where they formed a high mobility
conduction channel, undegraded by impurity scattering. For Group III/As- and Group III/P-based HEMTs, this channel is formed by doping the wider bandgap material (e.g., AlGaAs for GaAs or GaAs/AlGaAs for InGaAs) in order to provide carriers that diffuse to the unintentionally doped narrow bandgap material. In contrast, the wurtzite Group III-nitrides possess an inherently large spontaneous polarization field which, in combination with piezoelectric effects due to lattice mismatch strain, induces an interfacial sheet carrier density—the 2DEG—in HEMT devices on the order of $10^{13} \text{ cm}^{-2}$.[Ref. 29]

1.3.2 Device Fabrication

The prototypical Group III-nitride HEMT device incorporates an AlGaN barrier with a GaN buffer. First, GaN is epitaxially grown on a suitable substrate using techniques described in the preceding section; buffer and transition layers are often grown as preliminary steps to accommodate lattice mismatch or to otherwise improve the quality of the GaN. Next, an $\text{Al}_x\text{Ga}_{1-x}\text{N}$ layer is grown, with $x$ typically in the range 0.2 to 0.3. The active area is defined using conventional lithography techniques such as mesa etching. Ohmic contacts are formed over the source and drain regions, most commonly using a Ti/Al/Ni/Au metal stack but other materials for the diffusion barrier (e.g., Ta, V) and high conductivity layers (e.g., Ag, Pt) are also being evaluated for improving both contact resistance and device reliability.55,56 The gate, which is most often composed of a Ni/Au bilayer, is defined using a liftoff process. Generally, non-stoichiometric $\text{SiN}_x$ is then deposited over the entire device to provide a
passivation layer. However, if a field plate structure is desired then this metal layer stack will be deposited and patterned and an additional SiNx deposition performed. The passivation layer plays a critical role in mitigating the effects of RF-DC dispersion of the HEMT.\textsuperscript{56}

1.3.3 Applications

Group III-nitride materials offer material properties that are highly desirable for high power RF electronics and these provide a strong driver for their development. GaN-based devices in particular have undergone considerable evolution over the past two decades. As recently as 2005, silicon laterally diffused metal oxide semiconductor (LDMOS) FET devices accounted for 90\% of market share for high power RF amplifier application above 2 GHz, with the remainder being covered by GaAs pseudomorphic HEMTs.\textsuperscript{57}

From the amplifier point of view, GaN-based HEMTs have many advantages over existing production technologies (e.g., GaAs).\textsuperscript{56} The high output power density allows the fabrication of much smaller size devices with the same output power. Higher impedance due to the smaller size allows for easier and lower loss matching in amplifiers. The operation at high voltage due to its high breakdown electric field not only reduces the need for voltage conversion, but also provides the possibility to obtain high efficiency, which is a critical parameter for amplifiers. The wide bandgap also enables operation at high temperatures. At the same time, the HEMT offers better noise performance than that of MESFETs. These attractive features in amplifier applications enabled by
the superior semiconductor properties make the GaN-based HEMT a very promising candidate for microwave power applications.

1.4 Overview of this Dissertation

In this dissertation, the microstructure and defectivity of Group III-nitride HEMT device structures are characterized using TEM imaging, including related microanalytical techniques, and off-axis electron holography. Research results are presented for the following five subject areas: (i) electrically-stressed AlGaN/GaN HEMTs; (ii) the consequence of inadvertent amorphous layers at the gate metal/barrier interface of AlN/GaN HEMTs; and (iii) the impact of laser liftoff processing to separate GaN-based HEMTs from sapphire substrates. Substrate materials and engineering are excluded from the scope of this dissertation research but both metal contacts and electrical performance are treated, with the intent being to characterize and further understand failure mechanisms in Group III-nitride HEMTs.

In Chapter 2, experimental details are presented for TEM sample preparation using focused ion beam and for the TEM imaging, microanalysis, and electron holography techniques and data analysis performed in this research.

In Chapter 3, the results of a TEM investigation of electrically stressed AlGaN/GaN HEMT devices are presented. The relationship between degradation in electrical performance and observations of defects near the gate edges and gate metal diffusion into the barrier layer is described.
In Chapter 4, an unintentional amorphous layer beneath the gate metal contact of an AlN/GaN HEMT is identified and characterized and its presence correlated to improved device performance, including values of transconductance and cutoff frequency-gate length product which exceed all other values so far reported.

In Chapter 5, a process using an excimer laser to lift off AlGaN/GaN and InAlN/GaN from their sapphire substrates is discussed. Samples prepared for and analyzed by TEM are compared with similar reference samples and the impact on crystalline and specifically interfacial quality at the delaminated surface are characterized. The results are discussed in the context of related strain measurements.

In Chapter 6, the findings of chapters 3, 4, and 5 are summarized and recommendations for further research related to characterization of GaN-Based devices and understanding of their reliability are presented.
REFERENCES


36. CRC 79th Handbook of Chemistry and Physics, 1998-1999]


CHAPTER 2

EXPERIMENTAL DETAILS

This chapter presents the procedures and methods that were used for preparation of samples compatible with TEM study as well as brief descriptions of relevant imaging, microanalytical, and off-axis electron holography techniques. Special considerations for the preparation of samples suitable for electron holography are also discussed.

2.1 Sample Preparation

Many techniques have been developed for preparing samples for TEM analysis. However, the only technique which can reliably provide site-selective samples is focused-ion-beam (FIB) milling.\(^1\) This capability is essential for the great majority of samples extracted from processed semiconductor devices and it becomes even more critical in the context of ever-shrinking device dimensions that are currently prevalent in the semiconductor industry.

The original FIB systems were single-beam systems with a metal ion source, such as Ga, Au, or Ir. More recently, dual-beam systems similar to that shown in Fig. 2.1 have become the norm.\(^2\) Such systems comprise an electron source and ion source mounted at some fixed angle relative to each other, typically in the range 45° to 60°. This setup represents a significant improvement over single-beam systems since the electron beam can be used for secondary electron imaging of the sample, minimizing the extent of undesired interaction of
the ion beam with the specimen. Moreover, the dual-beam configuration enables concurrent imaging and milling of the sample, thus allowing real-time monitoring of the milling process. This capability contributes greatly to the superior throughput of FIB sample preparation relative to other techniques for which the sample typically must be repeatedly measured, often with a light microscope, to ensure that the sample region of interest is maintained in the appropriate orientation and that it is not overthinned.

Fig. 2.1. Schematic of a dual-beam FIB system used for TEM sample preparation,
showing the principal components: electron and ion columns, and gas injection system (GIS).

For TEM analyses of HEMT devices, as with most microelectronic devices, site specificity is a prerequisite. Thus, FIB milling is the preparation technique of choice. However, as with any sample preparation technique, there are disadvantages, notably the potential for introducing artifacts. Awareness of these disadvantages allows appropriate measures to be taken to mitigate their effects.

In most commercial FIB systems, a liquid metal Ga source is used as the ion source, with the Ga\(^+\) ions accelerated to energies that are typically in the range from 5 keV to 50 keV. Apertures allow control of the ion current density with corresponding sample currents typically in the range of 1 pA to 30 nA. The kinetic energy of the Ga\(^+\) ions drives the sputtering action which removes material in a controlled fashion via momentum and energy transfer. However, this milling action is also the impetus for the two most significant sample preparation artifacts of this technique: ion implantation and amorphization (and related material modification processes). Implantation may occur any time atomic (or molecular) species are incident on the surface of the material.

Figure 2.2 shows plots of particle trajectories in a 50 nm layer of GaN for 30 keV, 5 keV, and 1 keV Ga\(^+\) ions impinging normal (the surface of incidence is at the left edge of the diagrams) to the GaN surface. Based on the difference in penetration depth and lateral straggle, it is clear that a lower energy ion beam will introduce a lesser degree of artifacts, albeit at the expense of processing (milling)
time. It is standard practice to perform all milling at 30 keV except for the final ~100 nm removal that is done at the lowest energy available.

Fig. 2.2. SRIM Monte Carlo simulations of Ga\textsuperscript{+} trajectories in 50 nm GaN for incident ion energies of (a) 30 keV, (b) 5 keV, and (c) 1 keV.\textsuperscript{5}

Two additional techniques for reducing artifacts originating with ion implantation and ion beam-induced amorphization are Ar\textsuperscript{+} milling and plasma thinning (reactive ion etching). Ar\textsuperscript{+} milling offers some benefits over Ga\textsuperscript{+} milling. Commercial Ar\textsuperscript{+} milling systems typically allow milling at energies lower than those that have been available for ion beams in commercial FIB systems. However, that situation is changing as FIB systems capable of ion energies as low as 500 eV are becoming available. Another advantage is the nature of Ar itself: it is an inert element and it is not generally (intentionally) introduced into microelectronics structures (Ar sputtered films will incorporate some Ar). Its inertness precludes most chemical interactions of implanted Ar. Plasma thinning is essentially the application of reactive-ion-etching techniques, as commonly used in the semiconductor industry and elsewhere, to samples to be analyzed in an electron microscope. In the current context, it applies to a final thinning step for
the TEM sample by placing it in fixturing to incorporate it into the active electrode of an Ar rf plasma chamber. The rf plasma induces a dc bias at the sample which in turn creates a potential distribution which is only weakly conformal to the shape of the sample. Due to geometric enhancement effects, the electric field magnitude increases with decreasing sample radius of curvature. Accordingly, the ion flux and etching is amplified in regions of relatively small radius of curvature. This is not necessarily desirable since, for a typical “pluck-and-weld” (described in the following text) TEM sample lamella that is attached at one end, there will be an etch gradient from the base of the sample to its free end (longitudinal axis). In the direction orthogonal to the longitudinal axis and the normal to the sample faces, there will also be an edge-to-center etch gradient. These shortcomings may be overcome by the inclusion of O in the plasma to create a reactive, chemical component in addition to the kinetic component provided by impact of the Ar\(^+\) (and O\(^+\)). In this case, chemical etch selectivity should be taken into account.

The FIB system used in support of this dissertation research is an FEI Nova 200 NanoLab dual-beam system. A Schottky field emission gun (FEG) provides a high brightness, high coherence source of electrons. In immersion mode, the image resolution approaches 1 nm under the best practically attainable conditions. The ion beam is produced by a Ga liquid-metal ion source (LMIS). To facilitate sample preparation, it is also equipped with two gas injector systems (GIS) and a probe for sample extraction. The function of a GIS module is precise metering
and delivery of a precursor gas to the desired location, which is typically the eucentric point for the two beams coincident with the area of interest on the wafer sample. Some fraction of the incoming precursor species are adsorbed at the sample surface. The area of the sample scanned by the electron (or ion) beam transfers energy to the adsorbed species and consequent chemical reactions result in either deposition of material (bonding to the sample surface) or material removal selectivity, depending on the nature of the precursor. In the case of ion-beam-induced deposition, sputtering and deposition proceed as competitive processes, but precursor chemistry and beam (and surface conditions) are controlled to ensure the deposition rate exceeds the removal rate. The Nova 200 of this study has two GIS modules that enable electron-beam- or ion-beam-induced deposition of amorphous carbon or Pt using the precursors phenanthrene (C_{14}H_{10}) or trimethyl platinum (C_{9}H_{17}Pt, TMP), respectively.

The majority of TEM samples analyzed for this dissertation were cross-sections prepared using an in situ FIB liftout technique commonly referred to as “pluck-and-weld”. The following is a brief description of this technique.

1. A wafer sample is cut with a wafering saw to a size compatible with mounting on a SEM sample stub. The sample is imaged in SEM mode and the area of interest is located.

2. The wafer surface including and in close proximity to the area of interest must be protected to prevent ion-beam damage to the underlying material. Pt deposition may be performed using either the electron beam
or the ion beam. While the ion beam provides faster deposition rates due
to generally higher secondary electron yields, the electron beam enables
deposition without milling and other ion-related damage effects.
Therefore, the first step is to perform an electron-beam-induced
deposition of Pt until a layer thickness of 100-200 nm is achieved.\(^5\) Next,
an ion-beam-induced Pt layer of \(\sim 2 \mu m\) is deposited. These layers will
provide protection for the underlying area of interest as surrounding
areas are subsequently milled away.

3. The areas to either side of the Pt are milled in a terrace of steps at
relatively high (7-20 nA) ion-beam current, starting at \(\sim 9 \mu m\) from the Pt
edges and increasing to a maximum depth of \(\sim 5 \mu m\) at a distance of \(\sim 3\)
\(\mu m\) from the Pt. This step provides line-of-sight access to the sample
lamella for subsequent steps.

4. “Cleaning cross-section” milling, i.e., milling in sequential slices is
performed, alternating from one side of the lamella to the other.
Typically, the current is stepped down in consecutive operations, e.g., 5
nA, 3 nA, 1 nA, 0.5 nA until the lamella is 1 \(\mu m\) thick.

5. The stage is tilted to the value that places the ion beam as close as
possible to perpendicular to the lamella face. For the Nova 200, this
value is \(-10^\circ\). Release cuts are milled at the periphery of the lamella,
leaving a small “ear” connecting the lamella to the bulk of the wafer
sample.
6. A probe needle is maneuvered into place with the tip making contact (minimal overdrive to prevent mechanically stressing the lamella) with the lamella at the edge opposite the “ear”. The probe needle is attached to the lamella using e-beam induced Pt deposition. Once the needle is secured to the lamella, the “ear” is milled away, freeing the lamella from the bulk.

7. The needle and sample are lifted free from the SEM stage. The chamber is vented, the bulk sample removed and replaced with a liftout grid, and the chamber pumped down once again.

8. The probe needle is again maneuvered to place the lamella in proper orientation and proximity to the liftout grid and attached with ion-beam induced Pt deposition. Then the needle tip is milled to sever it from the lamella.

9. The lamella is now in position for final cleaning cross-section milling using 0.3 nA and then 0.1 nA ion beam currents to bring the final lamella thickness to within 100 nm of the desired final thickness.

10. The ion beam accelerating voltage and current are reduced to 5 kV and ~29 pA, respectively, and focus and astigmatism are again adjusted. The lamella is tilted to introduce a slight (3°-5°) angle between the ion beam and the lamella face. Milling is then performed in a raster pattern across the lamella face with a target removal of 50 nA. The same procedure is repeated for the opposite lamella face.
A phenomenon commonly known as “curtaining” is a sample preparation artifact which is produced when ion milling samples, especially when the beam is incident parallel or nearly parallel to the sample surface. It occurs when ion milling rates vary across the sample as a function of material or structural inhomogeneity. In the case of semiconductor devices, the “top” or processed side of the sample generally is subject to both sources of variation as different materials are used to obtain different properties and topography is created in the process of building up the integrated device structure. Because the substrate side of the sample is necessarily planar and homogeneous in composition, the manifestation of this type of sample preparation artifact can largely be mitigated by performing backside milling whereby the sample is manipulated in the FIB to allow the ion beam to be incident from the substrate side.

2.2 Imaging and Analysis Techniques

Transmission electron microscopy (TEM) plays the central role in the research presented in this dissertation. TEM encompasses a wide variety of imaging, diffraction, and analytical techniques and it is the only technique which enables direct imaging at the atomic scale. In all TEM techniques, a beam of electrons is directed to impinge on the sample of interest which has been prepared to be “electron-transparent,” i.e., it is sufficiently thin in the direction parallel to the incident beam that most electrons that enter the first surface—after interacting with the sample—are transmitted, emerging from the opposite surface to continue
through vacuum to be detected in various ways. Similar to light-optical microscopes, the TEM resolution depends on the de Broglie wavelength of the fast electrons (e.g., the relativistic wavelength for 200 keV electrons is 0.025 Å). Other factors, most notably aberrations in the electron optics, degrade the practical resolution, but with the newest aberration corrected instruments, resolution at the sub-Å scale is now possible. Most modern TEMs are operated at acceleration voltages in the range 50-300 kV.

2.2.1 Conventional Transmission Electron Microscopy

Although there are numerous practical TEM configurations, all instruments share a few common elements: electron source, condenser lens(es), specimen holder and stage, objective lens, post-sample lenses, and image viewing/recording apparatus.

The electron source may incorporate a thermionic emitter (e.g., W hairpin or LaB₆ crystal) but field emitters are now more commonly used due to their higher brightness (current density per unit solid angle), lower energy spread (greater temporal coherency), and superior spatial coherency (smaller apparent source size). In addition to extraction of electrons from the thermionic or field emission material, the electron source or “gun” accelerates the electrons to the desired final energy for the electrons (e.g., 200 keV).

Most TEM systems use two or sometimes three condenser lenses. The condenser lens nearer the electron source formed by the electron source optics provides several settings for demagnification of the electron crossover formed by
the electron source optics (“spot size” control). The second or final condenser lens transfers the electron crossover to the sample.

The specimen holder and stage provide the means for (a) securing the sample, (b) introducing the sample into the volume near the objective lens bore, and (c) providing translation along three axes. Holders are available which allow rotation about one or more of three principal axes. Mechanical and thermal stability, and accuracy and reproducibility of positioning are all critical properties for the specimen holder and stage.

The objective lens plays a crucial role in the electron microscope since it critically impacts performance. In particular, the spherical aberration of the objective lens is the ultimate limiting factor for TEM resolution. The objective aperture (in the back focal plane of the objective lens) selects the electrons which are transmitted from the exit surface of the sample; if the direct beam is selected a bright field (BF) image is formed, while if any of the scattered electrons are selected, a dark field image results.

Additional lenses are included for controlling image magnification and for viewing the electron diffraction pattern. The final lens in the main TEM column is a projector lens which transfers the image onto (a) a fluorescent screen for direct viewing, (b) a charge coupled device (CCD) camera, or (c) a TV monitor.

2.2.2 Scanning Transmission Electron Microscopy

In contrast to CTEM, for which the condenser lenses are adjusted to provide nearly parallel illumination onto the sample, in scanning transmission electron
microscopy (STEM) mode, the condenser lenses form a focused probe which is raster scanned over the sample area of interest (AoI). An image is not formed directly; instead various signals may be detected as the probe is scanned across the sample and the image is built up incrementally. The direct-beam electrons impact on the central detector enabling formation of BF STEM images while the annular detectors intercept scattered electrons enabling formation of DF STEM images.

2.2.3 Microanalytical Techniques

There are a number of analytical techniques available to complement imaging and diffraction modes in CTEM and STEM systems. Three of these techniques are energy-dispersive x-ray spectroscopy (EDXS), electron-energy-loss spectroscopy (EELS), and energy-filtered TEM (EFTEM).

When high energy electrons in a TEM impinge on the specimen, some electrons are subject to Coulombic interactions with the positive atomic nuclei as well as the negative bound electrons and will be decelerated and lose energy. Energy lost in this way is converted to a photon of the same energy $E_{\text{photon}} = h \nu$, where $h$ is Planck’s constant and $\nu$ is the frequency of the electromagnetic radiation. Since the beam electron may lose energy anywhere in the range from no loss (elastic scattering) to the full kinetic energy possessed before the interaction, the photons so created produce a continuum of radiation—*bremsstrahlung*, or “braking radiation”—in that energy range. In some cases, the beam electron may transfer sufficient energy directly to an electron in a constituent atom of the
sample and excite it into a vacant level at a higher energy. This in turn leaves a vacancy in an inner shell and renders the atom ionized. When an electron from an outer shell transitions to this lower energy vacancy, a photon is created, similar to bremsstrahlung, but in this case the energy is characteristic of the elemental identity of the atom from which it originated. Thus, for a particular sample under analysis in the TEM, peaks are superimposed on the bremsstrahlung continuum and these provide the means for identifying the elemental constituents of the sample. This forms the basis of EDXS. These characteristic energies superimposed on the bremsstrahlung continuum in an EDXS spectrum enable elemental identification of constituents of the sample under analysis. Characteristic energies for the atomic transitions just described fall in the x-ray portion of the electromagnetic spectrum.

In a sense, the physics of EELS is complementary to EDXS since the former uses characteristic electron-energy losses, some of which are the result of the characteristic x-ray emission used in the latter. When electrons in a TEM traverse the sample, inelastic scattering occurs to varying degrees. The electron sources used in TEMs are virtually monochromatic; if an energy analyzer is employed post-specimen then energy losses characteristic of the materials involved may be detected and interpreted in order to make elemental identifications and in some cases obtain chemical information. This analytical technique is known as electron-energy-loss spectroscopy (EELS). These inelastic interactions may be due to plasmon excitations, inner shell ionizations, phonon
excitations, and inter- and intra-band transitions. Inner shell ionization is particularly useful for making elemental identification. However, whereas EDXS detects the x-ray generated due to the inner-shell ionization, EELS measures the energy loss of the electron responsible for causing the ionization. In addition to chemical information, EELS may also be used to determine sample thickness, $t$, from an EELS spectrum through the relation

$$ t = \lambda_{IMFP} \ln\left(\frac{I_0}{I_{tot}}\right), $$

where $\lambda$ is the (averaged) inelastic mean free path of the sample material, $I_0$ is the integrated intensity of the zero loss peak, and $I_{tot}$ is the integrated intensity of the entire spectrum.\(^6\)

In addition to acquiring EELS spectra, the spectrometer may also be used to selectively image electrons from a narrow energy band. This capability enables energy-filtered imaging and diffraction and it may be realized using either an in-column filter or a post-column filter. In this research, energy filtering was used primarily for elemental mapping.

2.2.4 Off-Axis Electron Holography

Electron holography was originally proposed by Gabor (1948) as a means for correcting the spherical aberration ($C_s$) of the TEM objective lens and thus improving the eventual resolution. Its practical implementation was not possible until field emission electron sources became commercially available, thus enabling a highly coherent electron beam which is a prerequisite for the
technique, just as a highly coherent light source—a laser—is necessary for optical holography. In conventional CTEM and STEM imaging, all information manifests in the final image intensities and phase information is lost. In contrast, electron holography is a phase- (and amplitude-) imaging technique. Access to phase information offers many possibilities, but one of the most powerful applications is mapping and quantification of electrostatic potential profiles, a capability which is of particular interest for semiconductor devices, and specifically for heterointerfaces, p-n junctions, and dopant profiles.7,8

There are many ways to implement electron holography in a TEM,9 but all incarnations rely on the interference of two or more coherent electron waves to produce an interferogram, or hologram. One of the most common implementations is the off-axis electron holography mode which was used in this work. Fig. 2.3 shows a cross-section of the FEI/Philips CM200-FEG used for these studies, together with a schematic diagram illustrating the technique. An essential addition to the TEM column for the electron holography technique is an electrostatic biprism which is a conductive wire of diameter typically less than 1 μm. The electrostatic biprism is typically introduced as a replacement for one of the selected-area-diffraction apertures. The biprism is biased with respect to the microscope column, typically in the range of 50-300 V for a 200 keV electron beam. The field produced by the biprism deflects the electrons incident from the electron gun such that the electron waves from one side overlap and interfere with the electron waves from the other side. A TEM sample which is intended for off-
axis electron holography is prepared such that the area of interest is in close 
proximity to vacuum. The sample and electron optics (including the electrostatic 
biprism) may then be adjusted to allow one wave to pass through the area of 
interest while the wave—the reference wave—passes through only vacuum as 
shown in Fig. 2.3. The following sections provide a brief theoretical description 
of off-axis electron holography. In order to study HEMT devices, which have 
active areas on the order of one to a few microns in the direction of the gate 
length, it is necessary to have a commensurate field of view. In the case of 
electron holography this is achieved using a Lorentz lens in place of the 
instrument’s objective lens (current for that lens is zero for such experiments).

Wave-particle duality is manifested in many aspects of TEM and it 
plays a prominent role in electron holography. According to de Broglie 
(1924), a particle of momentum $p$ is characterized by a wavelength 
$\lambda = \frac{h}{p}$, where $h$ is Planck’s constant. The behavior of electrons in the presence of 
electromagnetic fields, such as those present in electron microscopes, may be 
described in terms of particles or waves. A treatment of the information 
transfer characteristics of the electron optics in a TEM in terms of the wave 
properties of the electrons allows application of the formalism developed by 
Abbe for image formation using coherent (visible light) illumination in a 
microscope.
An electron wave incident on the sample will interact with the sample during transit and as a result will have experienced some change in phase. This phase change in one dimension is given by

$$\varphi(x) = C_E \int V_0(x, z) \, dz - \frac{e}{\hbar} \iint B_\perp(x, z) \, dx \, dz,$$  \hspace{1cm} (2)

Where the $x$ axis lies in the sample plane, $z$ is the incident beam direction, $V_0$ is the mean inner potential (MIP), and $B_\perp$ is the magnetic induction component perpendicular to $x$ and $z$. The interaction constant $C_E$ is a term that depends on the incident electron wavelength $\lambda$, the kinetic energy $E$, and rest mass energy $E_0$, according to the expression

$$C_E = \frac{2\pi}{\lambda} \frac{E+2E_0}{E+E_0}. \hspace{1cm} (3)$$

For the samples analyzed in this research, the magnetic component may be disregarded. Furthermore, because the samples are prepared in cross-section, they may be assumed to be compositionally homogeneous in the direction normal to the sample surface. For the purposes of this research, the most advantageous application of electron holography is the identification and quantification of electrostatic fields in the active layers of AlGaN/GaN HEMTs.

To this end, the two most important material properties are the mean inner potential (MIP) and the inelastic mean free path (IMFP). The MIP is the volume-average electrostatic potential of a solid that manifests due to
incomplete screening of the atomic cores.\textsuperscript{4} MIP values for Group III nitrides are shown in Table 2.1.

\begin{table}
\centering
\begin{tabular}{|l|c|c|c|}
\hline
Material & Schowalter & Tanaka & McCartney \\
\hline
AlN & 15.88 & 13.1 & \\
GaN & 16.89 & 13.8 & 13.5 \\
InN & 18.9 & & \\
\hline
\end{tabular}
\caption{Table 2.1. Mean inner potential values for Group III-nitrides from \textit{ab initio} calculations.\textsuperscript{11-13}}
\end{table}
Fig. 2.3. (a) Schematic diagram of off-axis electron holography. (b) the FEI/Philips CM 200 TEM used for this work, and (c) a cross-sectional line drawing of the CM 200 electron optical column.
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CHAPTER 3

ELECTRICALLY STRESSED AlGaN/GaN HEMTs

This chapter describes an investigation of a set of AlGaN/GaN high electron mobility (HEMT) devices that had been subjected to electrical step-stress testing. This study was carried out in collaboration with Profs. F. Ren and S. J. Pearton at the University of Florida, whose groups were responsible for device fabrication and electrical testing. My contribution to this joint effort has been the microstructural and microanalytical characterization of related samples using electron microscopy. Results from this study have been accepted for publication elsewhere.¹

3.1 Introduction

As noted earlier, the HEMT is a specific type of heterostructure field effect transistor (HFET) that is particularly suitable for high power and high frequency applications.²,³ The first heterostructures developed for HEMT applications were based on AlGaAs/GaAs,⁴ but AlGaN/GaN and other III-nitride HEMTs are increasingly being studied due to their superior high power density and high frequency performance (> 5 W/mm and > 5 GHz, respectively), as well as higher input and output impedances which result in improved bandwidth.⁵ Since ensuring long-term reliability has become a serious consideration for many possible device applications, AlGaN/GaN HEMT research has recently been more closely focused on identifying and understanding failure mechanisms.²,⁶,⁷
The predominant mechanism(s) responsible for device breakdown in the AlGaN/GaN system are not yet well established. The traditional approach to lifetime testing is based on the three-temperature Arrhenius accelerated-life-test under DC or RF operating modes. However, the failure mechanisms activated by the extreme temperatures used in temperature-accelerated experiments do not necessarily have statistical relevance for normal operation. Recent reliability testing has focused on electric-field and current-driven failure modes arising from hot carrier degradation and defect formation caused by the inverse piezoelectric effect. For example, hot carriers could lead to device degradation through the formation of oxide traps and gate leakage current. High electric fields at the gate edge due to geometric enhancement, combined with the piezoelectric nature of the barrier material could result in very high, localized stress near the gate edge, possibly also leading to defect formation and loss of crystallinity.

Several TEM studies have reported physical evidence indicating that breakdown has occurred near the gate edge. In one case, samples were stressed at channel temperatures ranging from 250 °C to 320 °C with 40 V bias applied to the drain. Post-stress electrical measurements showed increases in threshold voltage and even more significant decreases in drain current. TEM observations at the drain side of the gate edge showed the presence of pit-shaped defects and cracks. The formation of these defects was again attributed to an inverse piezoelectric effect resulting from high electric fields localized at the drain-side edge of the gate.
In this current work, a set of nominally identical AlGaN/GaN HEMT samples was subjected to step-stress testing, and representative devices were then analyzed using electron microscopy techniques, including conventional transmission electron microscopy (CTEM), scanning transmission electron microscopy (STEM), electron energy-loss spectroscopy (EELS), energy-dispersive x-ray spectroscopy (EDXS), and energy-filtered imaging. The results provide interesting insights into possible failure mechanisms.

3.2 Experimental Details

The AlGaN/GaN HEMT devices examined here were fabricated on high-resistivity silicon substrates at the University of Florida. Epitaxial layers were grown with metal-organic chemical vapor deposition (MOCVD) using typical precursors in a cold-wall, rotating-disc reactor designed from flow dynamics simulations. Because of the large lattice mismatch between GaN and Si, a relatively thick stress-buffering layer was required in order to transition to the GaN channel deposition. First, an AlN nucleation layer was deposited, followed by a proprietary AlGaN transition layer.\textsuperscript{12,13} After this transition layer, a $\sim\text{1-\textmu m}$-thick GaN channel layer was deposited, then a 16-nm-thick Al$_x$Ga$_{1-x}$N ($x = 0.26$) barrier, and finally a 2-nm-thick GaN capping layer. The epitaxial barrier and buffer layers were grown at a nominal substrate temperature of 1030$^\circ$C.

After deposition of the epitaxial layers, Ti/Al/Ni/Au Ohmic contacts were deposited, followed by rapid thermal annealing at 825$^\circ$C in nitrogen ambient.
Finally, Ni/Au gate metal layers were deposited. Contact resistance, specific contact resistivity, and specific on-resistance were $0.45 \, \Omega \cdot \text{mm}$, $5 \times 10^{-6} \, \Omega \cdot \text{cm}^2$, and $2.2 \, \Omega \cdot \text{mm}$, respectively. Inter-device isolation was achieved via multiple-energy $\text{N}^+$ implantation in order to induce lattice damage throughout the GaN buffer layer. Ion-implantation processing was selected over mesa isolation in order to maintain planar device geometry and to reduce parasitic leakage paths. A 70-nm-thick non-stoichiometric silicon nitride ($\text{SiN}_x$) passivation layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) with the PECVD reactor baseplate maintained at 300 °C. The Schottky gate and windows for the Ohmic contacts were formed by selectively etching the SiN$_x$ passivation layer. A second SiN$_x$ deposition, and a pattern-and-etch step, further opened the gate and the Ohmic contact windows reopened. A Ni/Au metallization stack was concurrently deposited on the gate and Ohmic contact areas. The wafers were then passivated with another 400-nm-thick layer of PECVD SiN$_x$ at 300 °C. The contact windows were opened by dry etching. An additional metal deposition step formed the source field plate. The field plate was patterned to connect to the source contact and to extend $\sim 1 \, \mu\text{m}$ over the gate towards the gate-to-drain region. The source to gate distance, and the channel length of the HEMTs with and without the source field plate, were kept constant at $1 \, \mu\text{m}$ and $4.7 \, \mu\text{m}$, respectively. A schematic diagram of the HEMT geometry, together with the source field plate, is depicted in Fig. 3.1 (a).
Fig. 3.1. (a) Schematic diagram showing HEMT device geometry in cross section. Dimensions are as-designed, not necessarily as-processed. (b) SEM image showing entire HEMT device cross-section during TEM sample preparation using FIB milling.¹

Samples suitable for TEM observation were prepared by selective-area milling and subsequent liftout using the FEI Nova 200 NanoLab dual-beam focused-ion-beam (FIB) milling system at Arizona State University. Cross-sectional samples were taken from along the conventional gate length and were mounted on Omniprobe liftout grids for final thinning. Figure 3.1 (b) is a scanning electron micrograph showing an entire HEMT device during FIB milling in the Nova 200. Specimens were observed by high-resolution bright-field (BF)
imaging in a JEOL JEM 4000EX operated at 400 keV. A JEOL 2010F scanning TEM operated at 200 keV was used to obtain electron-energy-loss spectroscopy (EELS) linescans using a 0.5-nm STEM probe and 10-sec dwell time. Energy-filtered images for elemental mapping purposes were obtained using a Philips-FEI CM200 FEG equipped with a Gatan Imaging Filter (GIF). EDXS linescans were also performed using a 20 keV SEM probe in the Nova NanoLab instrument.

3.3 Electrical Characterization

Figure 3.2 shows step-stress leakage current results that are typical of the thirty or so HEMTs which were step-stressed in this study: (a) no degradation observed, (b) degradation occurring on the source-side gate edge, and (c) degradation occurring on the drain-side gate edge. With the source grounded and with +5 V applied to the drain, the gate bias voltage was swept from -5 V to a final value near -60 V, stepping in -1 V increments. The devices were stressed for 60 seconds at each gate voltage step. The total gate leakage current, $I_g$, is the sum of the gate-to-source leakage current, $I_{gs}$, and the gate-to-drain leakage current, $I_{gd}$. During the step-stress, $I_g$, $I_{gs}$, and $I_{gd}$ were measured. The drain I-V characteristic, transfer characteristic, gate forward current biased from 0 V to 1.5 V and gate reverse current biased from 0 V to -5 V were recorded between each step. Drain-to-source currents were held at low values such that self-heating effects were negligible, as supported by thermal simulations.
Fig. 3.2. (a) Off-state total gate current, gate-to-source current and gate-to-drain current for undegraded HEMT, as a function of gate voltage. (b) Off-state total gate current, gate-to-source current and gate-to-drain current for the source-side-degraded HEMT, as a function of gate voltage. (c) Off-state total gate current,
gate-to-source current and gate-to-drain current for the drain-side-degraded HEMT, as a function of gate voltage.\(^1\)

For the majority of the tested devices, the onset of the sudden increase of \(I_g\) was found to correlate with the onset of a sudden increase in either \(I_{gd}\) or \(I_{gs}\). The critical voltage of the off-state step-stress was thus defined as the onset of a sudden \(I_g\) increase (discontinuity in \(d|I_g|/dV_{gs}\)) during the stress testing. Most devices clearly showed this critical voltage during the stress-testing, as illustrated in Figs. 3.2 (b) and (c). Typically, additional increases of \(I_g\) were observed for stressed gate bias voltages above the critical voltage, as also visible in Figs. 3.2 (b) and (c). There were only two devices that did not exhibit a critical voltage during the stress testing measurements: no degradation was observed for the drain I-V characteristic, transfer characteristic (and derived extrinsic transconductance), and gate I-V characteristics after stress, as illustrated in Fig. 3.3.

These stressed devices exhibited depressed drain current and extrinsic transconductance \((g_{m,ext})\) as well as increased forward and reverse gate leakage currents, as illustrated in Fig. 3.4. Several authors have previously reported the coincidence of electrical degradation, as described here, with the appearance of pit-like structural defects along the exposed gate edges and the occurrence of gate metal diffusion at the gate-barrier/cap interface.\(^{10,11,14}\) Thus, it was inferred from these step-stress test results that physical degradation in the devices had most likely occurred on or near the gate edge closest to either the source side or the drain side, corresponding to increased \(I_{gs}\) or \(I_{gd}\), respectively.
Fig. 3.3. (a) Drain I-V characteristics; (b) extrinsic transconductance and drain current; and (c) forward and reverse gate IV characteristics, for HEMT not showing critical voltage during gate step-stress testing.¹
Fig. 3.4. (a) Drain I-V characteristic; (b) extrinsic transconductance and drain current; and (c) forward and reverse gate I-V characteristics, showing critical voltage in $I_{gs}$ during gate-voltage ramping. (d) Drain I-V characteristic, (e) extrinsic transconductance and drain current, and (f) forward and reverse gate I-V characteristics, showing critical voltage in $I_{gd}$ during gate-voltage ramping.$^1$
3.4 TEM Examination

Figure 5 shows a series of BF-TEM images of an unstressed device which did not undergo any form of electrical stress-testing. The low magnification image in Fig. 3.5 (a) shows the presence of threading dislocations, both under and away from the gate. Figure 3.5 (b) is an enlargement showing the gate-edge region on the source side where there is a prominent threading dislocation. Figure 3.5 (c) is an enlarged image which shows the edge of the gate on the drain side of the device, and suggests that the Ni layer of the gate metal has been modified.

Moreover, there is evidence for metal diffusion at the top of the threading dislocation (arrowed), as described in more detail below. Finally, Fig. 3.5(d)
shows a region beneath the gate where metal diffusion into the underlying AlGaN already appears to have occurred in several places (arrowed). Overall, these representative micrographs of an unstressed HEMT device indicate that the standard procedures commonly used for growth and fabrication can easily result in several different types of structural and/or chemical modifications, which could then possibly serve as preferential sites for subsequent device failure during later stress-testing experiments.

Figure 3.6 shows several BF-TEM images of a source-side-degraded HEMT device. The low magnification image in Fig. 3.6 (a) reveals the absence of any threading dislocations in the region beneath the gate contact, unlike the case for the unstressed sample. Moreover, the enlarged image in Fig. 3.6 (b) shows no apparent lattice disruption or structural defects near the gate-edge region on the drain side, but there is considerable metal diffusion into the AlGaN layer at one location (arrowed). Figure 3.6 (c) shows the source-side region of the gate contact, where a small pit in the AlGaN layer is evident.
Fig. 3.6. Source-side-degraded device: (a) low magnification image showing gate contact, (b) enlarged image showing source side of gate edge with no apparent defects visible, and (c) enlarged image showing a pit defect at the drain side of gate edge.
Results for the drain-side-degraded HEMT device have been published in a previous study that investigated the effect of the source field plate on HEMT reliability under off-state stress conditions, and Fig. 3.7 (a) shows a BF-TEM image of this device. In this case, several threading dislocations (as well as “curtaining artifacts” (see section 2.1) due to FIB milling) are visible under the gate contact. Figure 3.7 (b) reveals a small pit under the silicon nitride passivation layer just beyond the gate edge on the drain side, and some apparent gate metal diffusion is again also visible (arrowed). Finally, Fig. 3.7 (c) reveals another pit in the AlGaN layer but on the source side of the gate contact: the location of this defect would normally be considered as unexpected given that this particular device had exhibited drain-side-degraded electrical behavior. It is noteworthy that observations of another cross-section of the exact same drain-side-degraded HEMT device did not show any evidence for surface pits on either source or drain side of the device.

Figure 3.8 shows an area under the gate contact of a drain-side-degraded device where small-probe microanalysis was used to analyze several regions. Two scan lines, labeled 1 and 2, are indicated in Fig. 3.8 (a), and the corresponding EELS elemental profiles are shown in Figs. 3.8 (b) and 3.8 (c). The vertical dashed lines indicate the point along each linescan corresponding to the intersection of a line drawn across the apparent interface in the BF TEM micrograph of Fig. 8 (a). The linescan 1 clearly shows diffusion of a considerable volume of Ni penetrating several nanometers into the AlGaN layer, as well as
Fig. 3.7. Drain-side-degraded-device: (a) low magnification BF-TEM image showing gate contact; (b) enlarged image showing drain side of gate edge with small ‘pit’ defect visible in AlGaN layer just beyond the gate edge; and (c) enlarged image showing source side of gate edge with small ‘pit’ defect visible in AlGaN layer just beyond the edge of gate.¹,¹⁵
small traces of oxygen in the region of the interface. In contrast, linescan 2 shows a much more abrupt Ni signal, as well as a considerable oxygen signal occurring right at the interface. This oxygen signal coincides with the location of the very thin amorphous layer (0.5 nm to 1.5 nm) that was observed at the gate/nitride interface of most samples that were examined.

As mentioned previously, several devices did not show any indication of degradation in electrical performance after being subjected to stress-testing at voltages equal to or greater than those applied to other devices which exhibited electrical failure. Figure 3.9 (a) shows a BF-TEM image of the gate region of one of these electrically undegraded devices that in this case did not show any degradation even after stress at -90 V. No threading dislocations are observed beneath the gate nor are there any signs of pitting in the AlGaN layer close to the gate on either the source or drain side. Figure 3.9 (b) shows an enlarged view of an area under the gate, and Fig. 3.9 (c) shows results from a STEM-EELS linescan along the path indicated. Both the N and Ni signals indicate that the interface is relatively abrupt but a thin oxide layer is clearly again present at the interface.
Fig. 3.8. Drain-side-degraded device. (a) STEM image under the gate; (b) EELS elemental profile along line labeled ‘1’ in (a) showing unexpected presence of oxygen and evidence for considerable Ni diffusion into AlGaN layer; and (c) EELS elemental profile along line labeled ‘2’ in (a) showing sharp interface and evidence for considerable oxygen.\textsuperscript{1,15}
Fig. 3.9. Undegraded device: (a) low magnification image showing entire width of gate contact; (b) STEM image from region under the gate; and (c) corresponding EELS elemental profile indicating considerable oxygen at gate/AlGaN interface.

3.5 Discussion

Consistent with previous studies of AlGaN/GaN HEMT devices,\textsuperscript{10,15} we have found direct evidence linking electrical degradation with the appearance of structural defects. For electrically stressed devices which exhibited a sudden increase in $I_{gs}$ or $I_{gd}$, defects on the source- or drain-side of the gate, respectively, were observed. In the case of a stressed device which showed no evidence of electrical degradation, no gate-edge defects were observed. However, in the case
of the device that was electrically degraded on its drain side, a similar, albeit smaller, defect was visible at the source side of the gate edge, in addition to the defect observed on the drain side.

In a recent study, Chowdhury et al. reported a correlation between the severity of electrical degradation and the extent of structural defectivity at the gate edge.\textsuperscript{10} However, there was no clear causal relationship between the typical “v”-shaped pit defects located in the epitaxial layer(s) near the gate edges and the associated degradation of electrical performance, as manifested by the occurrence of a critical gate voltage at which the leakage current catastrophically increased. Another recent study has shown that the microstructural defects may occur discontinuously along the gate width.\textsuperscript{16} Thus, when preparing cross-section samples along the gate length via FIB liftout, such a defect may very well not be observed, since the probability of intersecting the defect during sample preparation is a function of the defect density.

Electric field effects have been cited as a significant factor contributing to HEMT degradation during electrical stressing, and have been attributed to an inverse piezoelectric effect present at the AlGaN barrier.\textsuperscript{17,18} The piezoelectric properties contribute advantageously to the formation of the 2DEG present at the AlGaN/GaN interface. However, at high bias (with associated high electric fields) the inverse piezoelectric effect provides a local environment that is conducive to defect formation. The presence of pre-existing crystallographic defects in
proximity to the high field regions in the barrier layer (namely, both gate edges) may then act as a trigger for the formation of pit defects.

Gate-edge pit defects are predominantly observed in the vicinity of threading dislocations, which is consistent with the observations of this study, particularly the absence of threading dislocations under the gate for the electrically stressed but undegraded sample. Although threading dislocations propagate from identifiable defects at the underlying epitaxial interface(s), their disposition in the vicinity of the gate will effectively follow a stochastic process for nominally identical processing conditions. For samples grown by MOCVD, the dislocation density for GaN is on the order of $10^7 \text{ cm}^{-2}$ to $10^8 \text{ cm}^{-2}$, corresponding to an average lateral separation of $\sim 1 \mu\text{m}$ so that the probability of dislocations occurring near the gate edges, particularly for the large gate widths used in power HEMTs, is quite high. Thus, it would be highly worthwhile to compare the behavior of devices fabricated with identical processing steps, but using substrates of higher quality, i.e., having reduced defect densities.

For almost all samples analyzed, a thin and unexpected amorphous layer was observed at the gate/barrier interface; this layer was identified as an oxide layer. Moreover, Ni gate-metal diffusion into the AlGaN barrier layer was observed at several locations, suggesting that gate-metal diffusion should be considered along with gate-edge pitting of the barrier layer when addressing electrical degradation mechanisms.
Despite some correlation between device breakdown with high gate leakage current and the development of gate-edge defects, the current evidence remains circumstantial and further work is required to establish a direct connection. In this regard, it would be instructive to carry out \textit{in situ} device biasing and stress-testing concurrently with TEM observation and analysis, although this might be a challenging task to realize in practice.

In summary, electrically step-stressed AlGaN/GaN HEMTs and characteristics of I-V and gate leakage curves correlated to specific microstructural defects in the gate region of each device. Inverse piezoelectric effects are often cited as the driving force for the evolution of gate-edge “pit” or “V”-shaped defects which are associated with dramatically increased leakage current but we find evidence that gate metal diffusion into the barrier layer may also play a significant role. The role of the thin and irregular oxide layer also remains to be determined.
REFERENCES


CHAPTER 4

OBSERVATIONS OF OXIDATION AT THE GATE/BUFFER INTERFACE
OF AlN/GaN HEMTs

This chapter describes an investigation of AlN/GaN high electron mobility
transistor (HEMT) devices, focusing on oxidation at the interface between the
gate contact and the ultrathin AlN barrier layer. This work was a collaborative
effort with the group of Capt. K. Chabak at Wright-Patterson Air Force Base who
fabricated and electrically tested the devices used in this study. My role was to
provide microstructural and microanalytical analysis of tested devices. Some of
these results have been published elsewhere.¹

4.1 Introduction

HEMT technology—in particular the III-nitride (III-N) HEMT—is highly
suited to millimeter-wave power and low-noise amplifier (LNA) device
applications. Of the group III-N heterostructures, the AlN/GaN interface offers
the highest theoretical two-dimensional electron gas (2DEG) sheet charge
density.² As discussed previously, this 2DEG results from a combination of
spontaneous and piezoelectric polarization.³ The growth of high quality AlN/GaN
epitaxial heterostructures using sapphire substrates, which achieve high mobility
and 2DEG sheet charge density while concomitantly maintaining low sheet
resistance (< 200 Ω/□), have recently been reported.⁴⁻⁶ A key capability in this
regard is the growth of an ultrathin (< 6 nm) AlN barrier with high
transconductance and reduced short-channel effects for dc and RF operation. In combination, these features enable performance surpassing that of HEMTs based on AlGaN/GaN and AlInN/GaN heterostructures.\textsuperscript{5,7} For low noise amplifier applications, relatively lower power requirements render the thermal management advantage of SiC substrates less important and AlN/GaN HEMTs on sapphire substrates emerge as a more affordable alternative.\textsuperscript{8}

Development of AlN/GaN HEMTs has been hindered by fabrication challenges such as tensile lattice strain, strain relaxation, and surface effects of the AlN barrier layer.\textsuperscript{9} To address these problems, the integration of atomic layer deposition gate dielectrics and novel surface passivation\textsuperscript{5,10-13} are now being implemented to suppress gate leakage, reduce gate capacitance, and maintain the integrity of the ultrathin barrier. Superior dc and RF performance has been demonstrated for sapphire substrates with the highest-to-date $I_{DS,max} = 2.9$ A/mm (Cao et al., 2007) and $f_t > 100$ GHz.\textsuperscript{10,11} Improved transconductance and high frequency performance has been reported for enhancement-mode AlN/GaN HEMTs on SiC substrates.\textsuperscript{11} AlN/GaN HEMTs fabricated with relatively thick AlN barriers (~6 nm) on 4-in silicon substrates have demonstrated record GaN-on-silicon dc results due to recessing metal contacts into the silicon nitride ($\text{Si}_x\text{N}_y$) passivation cap grown \textit{in situ}.\textsuperscript{7} However, in general, the available literature indicates that AlN/GaN technology remains immature as the $f_t \cdot L_G$ figure of merit is relatively low (< 6.5 GHz $\mu$m) for $L_G < 0.1$ $\mu$m, when targeting high frequency performance.\textsuperscript{10,14}
RF and dc measurements and TEM results are presented here for AlN/GaN HEMTs grown on sapphire substrates with an ultrathin ∼3.5-nm barrier and gate lengths, $L_G = 80–180$ nm. These data show that an amorphous oxide can be formed under the gate contact as a result of standard T-gate processing, yielding low gate leakage while maintaining excellent dc/RF performance with improved $f_T \cdot L_G$ product.\(^b\)

4.2 Experimental Details

The AlN/GaN HEMTs were grown by RF plasma-assisted molecular beam epitaxy on 2-inch c-plane sapphire substrates. After surface nitridation, a thin AlN nucleation layer was grown followed by ∼3-μm GaN buffer/channel layer. Next, a 3.5-nm fully strained AlN layer was grown at ∼700 °C. The tensile strain engendered in the AlN grown on Ga-polar GaN produces a piezoelectric polarization which, when combined with the spontaneous polarization present in each of the wurtzite components of the heterostructure, results in a 2DEG on the GaN side of the interface. Finally, the AlN surface was capped with a 1-nm GaN layer. AlN/GaN HEMTs were then fabricated beginning with chlorine-based dry etching to achieve device isolation and using an evaporation deposition/liftoff process for metal contacts. The ohmic (source and drain) and Schottky (gate) contacts were composed of Ti/Al/Ni/Au and Ni/Au metal layers, respectively. The

\(^b\) The current-gain cutoff frequency-gate length product is a figure of merit which via charge control theory provides an estimate for the saturation electron velocity.
ohmic metal was annealed for 30 s at 850 °C in nitrogen ambient. The contact resistance, $R_C$, measured across the wafer using the linear transmission line method (TLM) structures was $0.57 \pm 0.11 \, \Omega \cdot \text{mm}$, which closely approaches the best reported value, $0.4 \, \Omega \cdot \text{mm}$. The Schottky T-gate was centered between the source–drain contacts, and was formed using a bilayer poly(methyl methacrylate)/methyl methacrylate photoresist with a brief oxygen plasma and HCl:H$_2$O (1:1) wet etch pre-metallization treatment.

Samples for TEM observation were prepared by selective-area milling and subsequent liftout using the FEI Nova 200 NanoLab dual-beam focused-ion-beam (FIB) milling system. Cross-sectional samples were extracted from along the conventional direction of the HEMT gate length and then mounted on Omniprobe liftout grids for final thinning. Figure 4.1 is an SEM micrograph showing the entire active area of one of the HEMT devices, near the completion of FIB processing in the Nova 200. High-resolution bright-field (BF) imaging of the specimens was performed in a JEOL JEM 4000EX operated at 400 keV. A JEOL 2010F scanning TEM operated at 200 keV was used to obtain energy-dispersive x-ray spectroscopy (EDXS) linescans using a 0.5-nm STEM probe and 10-sec dwell time. Energy-filtered images for elemental mapping purposes were obtained using a Philips- FEI CM200 FEG equipped with a Gatan Imaging Filter (GIF).
Fig. 4.5. SEM micrograph of a completed FIB-milled cross-section of a T-gate structure AlN/GaN HEMT.

4.3 TEM and Electrical Testing Results

Results from static and pulsed $I_{DS}(V_{DS})$ measurements are shown in Fig. 4.2 (a) for a passivated 80-nm T-gate device with $2 \times 100$-$\mu$m gate width. A maximum drain current density of $\sim 1.25$ A/mm was recorded near the knee voltage at $V_{GS} = +2$ V. Thereafter, the drain current was significantly reduced due to local Joule heating which could not be adequately accommodated by the relatively low thermal conductivity of the sapphire substrate. Minor short-channel effects are attributed to the combined barrier/α-oxide thickness (effective $t_{bar}$), yielding an aspect ratio $L_G/t_{bar} \sim 14$ in addition to buffer leakage.\textsuperscript{15} Pulsed data are also superimposed on the $V_{GS} = +2$ V curve in Fig. 4.2(a) for 200 ns pulses with 1 ms period. The zero-bias condition ($V_{GSO}/V_{DSO} = 0/0$ V) suppresses both thermal and trapping effects to produce an ideal 1.75-A/mm output current density. Drain and current lag refer to transient current drops normally associated with buffer and
surface trapping states, respectively. The two additional pulse conditions $(V_{GSO}/V_{DSO} = -4/0 \text{ V}, \ V_{GSO}/V_{DSO} = -4/10 \text{ V})$ indicate that surface state trapping is present creating a small gate-and-drain current lag. Figs. 4.2 (b) and (c) present the gate leakage current induced by gate-and-drain bias stress. In Fig. 4.2(b), the gate leakage is suppressed to less than $10^{-4} \text{ A/mm}$ with the 2DEG channel fully open for maximum drain current. Beyond the knee voltage, an excellent gate leakage value—less than $10^{-6} \text{ A/mm}$—is measured for $V_{GS} < +2 \text{ V}$.

This value is sufficiently lower than the output current density, which verifies that any drain current degradation is not related to gate leakage. Additionally, Fig. 4.2(b) shows the OFF-state drain-induced gate leakage, which is less than $10^{-6} \text{ A/mm}$ up to $V_{GD} = -14 \text{ V}$. The gate diode of Fig. 4.2(b) indicates a Schottky behavior with $\sim 10 \text{ mA/mm}$ or less gate current for high reverse bias of up to $V_{GS} = -30 \text{ V}$. For $L_G = 180 \text{ nm}$, an order of magnitude lower gate leakage current was recorded. The overall higher reverse gate bias leakage can likely be attributed to the low-quality a-oxide interface and the ultrathin AlN barrier.

The $I_{DS}(V_{GS})$ transfer characteristics are shown in Fig. 4.2(c) from $V_{GS} = -4 \text{ V}$ to $V_{GS} = +2.5 \text{ V}$ at $V_{DS} = +4 \text{ V}$. The 80-nm device is compared with a 180-nm-gated device, which shows extrinsic transconductance values of 475 and 500 mS/mm, respectively. To our knowledge, this is the highest extrinsic transconductance performance demonstrated with AlN/GaN HEMTs on sapphire substrates.\(^5\) The difference in transconductance for each gate length can be
explained by high variations of source access resistance, i.e., \( R_S = 1.23 \pm 0.35 \ \Omega \cdot \text{mm} \), across the wafer. By de-embedding \( R_S \) from each device and using the expression \( g_{m,\text{ext}} = g_{m,\text{int}}(1 + g_{m,\text{int}}R_S)^{-1} \); where \( g_{m,\text{ext}} \) and \( g_{m,\text{int}} \) are the extrinsic and intrinsic transconductances, respectively; intrinsic transconductance values are calculated to be greater than 1.5 S/mm (\( R_S \sim 1.4 \ \Omega \cdot \text{mm} \)) and 0.9 S/mm (\( R_S \sim 1 \ \Omega \cdot \text{mm} \)) for the 80- and 180-nm devices, respectively. The high intrinsic
transconductance is directly related to the superior channel modulation advantage obtained by using an ultrathin AlN barrier. The sub-threshold slope was found to be in the range of 0.4-0.6 V/dec. Under channel pinch-off conditions, the drain–source current was relatively high because of buffer leakage resulting in a poor $I_{ON}/I_{OFF}$ ratio. This buffer leakage was validated using mesa isolation structures separated by 5 µm of GaN buffer. The average buffer leakage was determined to be $2.1 \pm 1.2$ mA/mm. The three-terminal breakdown voltage was, therefore, quite low using an $I_{DS} \sim 1-2$ mA/mm current compliance; however, it increased to approximately 20 V for $I_{DS} \sim 50$ mA/mm.

The small-signal RF gain for each gate length is shown in Fig. 4.3 using peak $g_m$ conditions as the gate bias and a constant drain bias of +4 V. Unity current gain cutoff frequency $f_t$ and maximum frequency (using Mason’s unilateral power gain) $f_{maxU}$ are plotted and extracted using a conservative $-20$ dB/dec slope methodology. The gate-and-drain pad capacitance was calculated to be $\sim 20 \mu F$, which was de-embedded from the measured y-parameters for intrinsic $|h_{21}|$ gain. The $f_t/f_{maxU}$ values for the 80- and 180-nm gated devices were 101/100 GHz and 57/73 GHz, respectively. These values correspond to a $f_t \cdot L_G \sim 8.1 \text{GHz} \cdot \mu \text{m}$ ($L_G = 80$ nm), which is superior to comparable AlN/GaN-on-sapphire values so far reported in the literature,$^{10,11}$ and near the best for SiC,$^{11}$ with $L_G < 0.1$ µm. Relatively low $f_{maxU}$ is related to the larger unit gate width and high $C_{gd}$ as a result of low drain bias. As the source–drain distance is scaled down.
to \( \sim 1 \ \mu m \) or less, even higher \( f_t \cdot L_G \) product values can be expected due to reduced access resistance.

After initial electrical testing revealed excellent gate leakage results, the samples were provided for TEM analysis, with particular emphasis on the interface between the gate metal and the underlying epitaxial layers. Samples

Fig. 4.3. Small-signal RF performance for passivated 2 x 100 \( \mu m \) AlN/GaN T-gate HEMTs with 80 nm (solid symbol) and 180 nm (open symbol) gate lengths. (a) Unity current gain, and (b) unilateral power gain.\(^1\)

After initial electrical testing revealed excellent gate leakage results, the samples were provided for TEM analysis, with particular emphasis on the interface between the gate metal and the underlying epitaxial layers. Samples
suitable for TEM examination were prepared by FIB liftout. During initial examination of the gate region it was immediately clear that an unintended layer was present between the gate metallization and the underlying epitaxial layers, as illustrated in the BF images shown in Fig. 4.4. Figure 4.4 (a) shows most of the T-gate structure, as well as the epitaxial AlN barrier and GaN buffer layers.

Fig. 4.4 (b) shows the relatively high intensity of the unintended layer that indicates low-Z (low atomic number) constituent materials. Lattice fringes are apparent in Fig. 4.4 (c) in both the epitaxial layers and the gate metal bilayer stack. However, the absence of lattice fringes in the unidentified layer is indicative of an amorphous material. The low-Z, amorphous character and the potential for exposure to oxidizing processes during processing made the presence of an oxide layer possible but confirmation was still needed.

A sample was examined in the JEOL 2010 using EDXS linescans for analysis purposes. The linescans were acquired across the interface between the gate metal and the epitaxial AlN barrier layer as shown in Fig.4.5. The thin GaN capping layer is not resolved in this image. The various layers labeled in Fig. 4.5 are identified in Fig. 4.6, with the Ga and Ni signals clearly straddling the central Al signal. An oxygen signal appears at the interface between the AlN and Ni.
Fig. 4.4. Cross-sectional TEM BF images of the region under the stem of the Ni/Au bilayer T-gate. In the images, the gate is the center top structure (darker contrast), the epilayers appear below the gate structure (lighter contrast). (a) Image showing full gate structure. (b) A thin amorphous layer with bright contrast is arrowed. (c) Higher resolution image of this layer (arrowed) at the edge of the gate stem. (d) High magnification image of mid-gate region, again showing a conspicuous amorphous region.
Fig. 4.7. BF TEM image of area subsequently analyzed with EDXS. The area interrogated by the linescan is indicated by the arrow.
Fig. 4.8. EDXS linescan data with GaN, AlN, and Ni layers delineated. A small but distinct oxygen signal appears in close proximity to the AlN/Ni interface. An integrated intensity profile indicates the relative positions of the gate Ni, AlN barrier, and GaN buffer layers.

To obtain better spatial resolution and positive identification of the location of the oxide layer, energy-filtered TEM (EFTEM) was performed using the Philips CM 200 TEM equipped with a Gatan imaging filter (GIF). EFTEM images were acquired for electron-energy-loss edges characteristic of several stack are clearly defined in Figs. 4.7 (d) and (f) for the Ni L₃ (855 eV) and Au
Fig. 4.9. EFTEM maps of the gate interface region.
elements of interest, as shown in Fig. 4.7. The Ni and Au of the gate metal bilayer M4,5 (2206 eV) edges, respectively. The map of the N K edge (401 eV) indicates the nitride epilayers as well as the Si₃Nₓ passivation layer. Of particular interest is the O K edge (532 eV) map which not only clearly delineates the oxide layer of interest but also provides evidence for oxygen at the interface between the gate Ni and the passivation dielectric layers. TEM micrographs also showed that the total distance from the gate to the 2DEG was slightly larger in this region when compared to the gate-source and gate-drain access regions. It is hypothesized that this oxide layer is related to the aluminum/gallium semiconductor and/or nickel metal layers absorbing oxygen as a result of the standard T-gate processing. The processing details required to control this oxidation method remain under investigation.

4.4 Summary

AlN/GaN HEMTs grown on sapphire substrates exhibit excellent dc and RF performance. The high performance is attributed to the high-quality, ultrathin AlN barrier layer, and robust ohmic and gate contact processes. Oxidation at the semiconductor/metal interface of the T-gate that formed a thin a-oxide gate insulator was identified via TEM microstructural and microanalytical characterization. Attributed to this previously unidentified layer, high reverse gate bias up to −30 V was demonstrated and drain-induced gate leakage was suppressed to impressive values of less than 1 μA/mm. In addition, g_m,ext ≃ 500 mS/mm and f_t · L_G ≃ 8.1 GHz·μm were achieved, which are the highest known
reported values for AlN/GaN HEMTs fabricated on a sapphire substrate despite having high access resistance.
REFERENCES


CHAPTER 5

FURTHER INVESTIGATIONS OF GaN-BASED DEVICES

This chapter describes additional studies related to GaN-based HEMT devices. This work was conducted in collaboration with the research groups of Professors Fan Ren and Stephen Pearton at the University of Florida, which were responsible for processing the semiconductor devices and for subsequent electrical testing. My role was to provide microstructural and microanalytical analysis of tested devices. Two sets of GaN-based HEMT devices were investigated and some of the results for the laser liftoff studies have been published elsewhere.¹

5.1 Laser Liftoff of AlGaN/GaN HEMTs

AlGaN/GaN high electron mobility transistors (HEMTs) with high electron mobility and saturation drift velocities are promising for high power and high frequency applications.²⁻⁹ Although sapphire is widely used as a substrate for producing HEMT structures, GaN-based devices grown on sapphire suffer from two major drawbacks: 1) the poor thermal conductivity of sapphire, and 2) the large mismatch between the coefficients of thermal expansion (CTE) for sapphire and GaN. Taken in combination, these two deficiencies have a significant negative impact on the thermal management of GaN-based devices grown on sapphire substrates, i.e., the heat generated during normal device operation cannot be dissipated effectively, consequently limiting device performance. SiC is an
alternative substrate for GaN growth with high thermal conductivity and improved CTE compatibility, but the high cost of SiC substrates limits their applicability.

Laser liftoff (LLO) technology\textsuperscript{10–12} has recently been developed and widely used for GaN-based light-emitting diodes to improve thermal dissipation, operating current, and light extraction ratio.\textsuperscript{10,13–15} Typically, a 248-nm laser is used to decompose a thin layer of GaN at the GaN/sapphire interface, which then enables separation of the GaN film from the sapphire substrate. Once separated, the GaN film can then be transferred onto substrates having superior thermal characteristics, lower cost, and higher quality. Although liftoff of AlGaN/GaN HEMTs has been demonstrated, the film quality and device performance of the HEMTs reported in these studies have been inconsistent.\textsuperscript{16–22} It was shown that the film quality was directly impacted by the uniformity of the laser beam incident on the area to be lifted off, with the central region of the lifted-off sample exhibiting better quality than areas near the periphery.\textsuperscript{22} This difference was attributed to an intensity gradient at the edge of the laser beam spot causing crack generation and crystal structure degradation.\textsuperscript{22,23} A 10–15\% reduction of the drain current was reported for LLO HEMTs,\textsuperscript{17} but higher saturation drain current was also reported for LLO HEMTs.\textsuperscript{18} However, no explanation was provided for either device degradation or enhancement.\textsuperscript{17,18} The present study demonstrates the use of a 193-nm laser to lift-off HEMT structures from sapphire substrates. Transmission electron microscopy (TEM) was employed to examine the material.
quality of the LLO HEMTs. Drain and gate current-voltage (I-V) characteristics were used to evaluate the effects of the LLO processing on device performance. Both the Newton’s rings method and Raman spectroscopy were used to estimate the amount of strain relaxation of the LLO HEMTs.

5.1.1 Experimental Details

The AlGaN/GaN HEMT structures were grown on c-plane sapphire substrates by metal-organic chemical vapor deposition. The epilayers consisted of 2-μm-thick carbon-doped GaN buffer layers followed by a 55-nm-thick undoped GaN layer, 20 nm of Al0.25Ga0.75N, and a 2.5-nm-thick GaN capping layer. On-wafer Hall measurements showed sheet carrier concentration, sheet resistance, and mobility of $8.5 \times 10^{12}$ cm$^{-2}$, 550 Ω/□, and 1520 cm$^2$/V·s, respectively. Multiple energy and dose helium-ion implantation was used to electrically isolate adjacent devices. Ohmic source-drain contacts were formed using Ti/Al/Ni/Au metallization and annealing at 850 °C for 30 s, producing a specific contact resistance of 0.4 Ω·mm. The HEMTs employed a Ni/Au-based 1-μm gate length and 200-μm gate width, with source-to-gate and gate-to-drain distances of 1 μm and 1.5 μm, respectively. The devices were passivated with 200 nm of SiNx deposited by a Plasma-Therm 790 plasma-enhanced chemical vapor deposition (PECVD) system.

The laser-liftoff processing was performed using a JPSATM IX-260 ArF excimer laser system ($\lambda = 193$ nm). A convex/convex/convex tripler objective lens with a meniscus corrector was used to correct spherical aberration, and the
focal length of the tripler was 10 cm. A metal mask was installed in the light path and the openings on the mask were imaged onto the target surface. The laser pulse duration was fixed at 25 ns and the maximum repetition rate was 100 Hz. The sample stage was designed to accommodate 6-in. wafers. Two He–Ne lasers were used to guide the high-accuracy air-bearing x-y linear-motor sample stage, with stage movement resolution of 0.1 μm per step. The stage had an accuracy of ±3 μm over a full range of motion with a stage velocity of 6–8 in./s; the stage position could be programmed with a resolution of ±1 μm and stage movement repeatability of ±1 μm. The fluences used in this study were in the range 650-800 mJ/cm² for the LLO processing and 1.3 mJ/cm² for groove drilling. To mitigate micro-crack formation along the edges of the LLO samples during laser processing, 30-μm wide grooves were drilled through the entire AlGaN/GaN HEMT structure from the front side of wafers. Photoresist was first spin-coated on the wafer to protect the device from debris generated during laser drilling. The HEMT samples were mounted on AlN or Si wafers with the epitaxial side of the samples contacted to the mounting substrate using adhesive or wax. Figure 5.1 shows optical photographs of the HEMT sample before and after groove drilling. After the LLO processing, 5-min etching in a 1:1 HCl:H₂O solution was used to remove gallium droplets from the lifted-off GaN surface. Acetone was then used to remove the mounting wax to obtain the freestanding LLO HEMTs. The dc characteristics of the HEMTs were measured with an HP 4156 semiconductor parameter analyzer.
Figure 5.2 shows the Si-submounted LLO samples, the matrix of areas subjected to different laser fluences (as delineated by the laser-ablated grooves, and a top-down view of a sample during FIB trenching. Cross-sections of the HEMT structures before and after LLO processing were prepared for TEM examination by selective-area milling and subsequent liftout using the FEI Nova 200 NanoLab dual-beam focused-ion-beam (FIB) milling system. Cross-sectional samples were extracted from along the conventional direction of the HEMT gate length and then mounted on Omniprobe liftout grids for final thinning. Figure 5.3 is an SEM micrograph showing the entire active area of one of the HEMT devices, near the end of FIB processing in the Nova 200. High-resolution bright-
field (BF) imaging of the specimens was performed in a JEOL JEM 4000EX operated at 400 keV.

Fig. 5.2. (a) Samples submounted on Si were coated with ~10nm evaporated carbon to prevent charging of the sample surface in the FIB-SEM. (b) Singulated areas after liftoff and submount on Si substrate; laser-ablated grooves. (c) Sample after initial FIB milling; Pt bar is indicated.¹
5.1.2 Electrical Testing, Strain Measurement, and TEM Results

Figure 5.4 (a) shows a LLO HEMT placed on a flat glass lamella. Interference patterns are clearly visible in the middle of the sample, which indicates that the LLO HEMT samples are not flat. The bending of the freestanding LLO HEMT sample could be due to relaxation of the built-in strain from deposition of the SiN$_x$ film and metal contacts during the device fabrication, as well as strain resulting from the lattice mismatch between AlGaN and GaN during material growth.

Figure 5.4(b) shows an enlarged optical image of the edge of an LLO HEMT defined by laser drilling; the edge is very sharp and no micro-cracks are
evident. Without drilling grooves along the HEMT structure prior to the LLO process, the edges of the laser lift-off area would otherwise have developed cracks due to the impact of the shock wave created during the high fluence laser exposure, which would separate the laser-exposed area and the unexposed regions but result in the development of irregular edges and micro-cracks.

Figure 5.5(a) shows the drain I-V curves of a typical HEMT before and after LLO processing.\textsuperscript{1} Both curves exhibit good pinch-off characteristics, but a marked reduction in saturation drain currents is observed relative to the control sample values. About a dozen of the LLO HEMTs were examined and the saturation drain current of these HEMTs after LLO process ranged from 25-42% lower than for HEMTs before LLO processing. However, the threshold voltage of
the HEMT was only slightly shifted, as shown in Fig. 5.5(b). The threshold voltage was obtained from the intercept with the x-axis of the line fitted to the linear region of the square root of the drain current. Since no micro-cracks were identified on the LLO HEMT samples, the saturation current degradation is thought not to be due to micro-crack formation that is normally present on typical LLO samples.

Fig. 5.5. Comparison of drain current characteristics for an AlGaN/GaN HEMT pre- and post-LLO processing. (a) Source-drain I-V families of curves. (b) Square root of drain current versus gate voltage.¹

Schottky gate and drain punch-through characteristics were also examined to determine whether the AlGaN Schottky contact layer or GaN buffer were damaged during the LLO process. As shown in Fig. 5.6(a), gate I-V characteristics of a typical HEMT prior to and after the LLO process were very similar, and the gate I-V curves for some of the LLO HEMTs actually revealed slightly lower reverse leakage current and higher Schottky barrier height. These
improvements might be due to a piezoelectric effect from the Schottky contact to the AlGaN layer on the states of surface traps. However, this possibility needs to be confirmed with modeling. Based on the Schottky characteristics, there was no evidence that the AlGaN layer had been damaged during the LLO processing. Figure 5.6(b) illustrates the drain punch-through voltages of the HEMT before and after the LLO processing. The gate dimensions of the HEMT were 1 μm × 200 μm and the distance between the gate electrode and drain contact was 38 μm. The HEMT showed a 650 V drain punch-through voltage and there was no difference between the HEMT before and after the LLO processing. Thus, the electrical test results indicate that the quality of GaN buffer layer was not degraded.

![Graph showing leakage and punch-through for AlGaN/GaN HEMT pre- and post-LLO processing.](image)

Fig. 5.6. Leakage and punch-through for the AlGaN/GaN HEMT pre- and post-LLO processing. (a) Forward and reverse gate leakage currents. (b) Drain punch-through voltage at Vg = -7 V.¹

In order to separate the effects of the strain induced by the lattice-constant...
mismatch between AlGaN and GaN from the built-in strains of SiNₓ film and metal contacts deposited on the HEMT structure, circular samples of AlGaN/GaN HEMT structures without SiNx or metal contacts were also lifted-off to evaluate the partial relaxation of the strain induced by the lattice constant difference between AlGaN and GaN. Prior to the LLO processing, a 20-µm wide circular groove was drilled from the front side of the sample defining the radius of the circular sample, which was chosen to be 100 µm. When the LLO circular samples were placed on a Si wafer, circular optical diffraction patterns were observed, as illustrated in Fig. 5.7(a). These circular diffraction patterns are known as Newton’s rings. Thus, the LLO circular sample was warped due to partial relaxation of the strain between the AlGaN and GaN layers. The radius of the warped circular LLO HEMT sample, R, as shown in Fig. 5.7(b), was estimated based on the Newton’s rings method,

\[ R = \frac{r_k^2}{k \cdot \lambda}, \quad (1) \]

where \( R \) is the radius of the warped sample, \( k \) is the number of dark rings and \( k = 1, 2, 3, \ldots \), \( r_k \) is the radius of \( k^{th} \) dark ring, and \( \lambda \) is the wavelength of light. The partially relaxed strain induced deflection, \( d \), is calculated using

\[ d = R - \sqrt{R^2 - L^2} \cong \frac{L^2}{2R}, \quad \text{for } R \gg d, \quad (2) \]

where \( L \) is the radius of the circular LLO HEMT samples. The partially relaxed strain, \( \Delta \varepsilon \), of the circular LLO HEMT was estimated by treating the LLO sample
as a single structural beam. The tensile strain near the top surface of the structural beam is given by

\[ \Delta \varepsilon = \frac{t \cdot d}{L^2}, \]

where \( t \) is the sample thickness, \( d \) is the deflection, and \( L \) is the length of the structural beam.

Table 5.1 summarizes the calculated radius of the warped circular LLO HEMT sample, the deflection induced by the partially relaxed strain, and the partially relaxed strain for the circular LLO HEMT sample. To corroborate the partially relaxed strain calculated using the Newton’s rings method, micro-Raman
scattering measurements were also performed on the same sample before and after the LLO processing.

For GaN, the E\textsubscript{2} peak has been shown to be very sensitive to stress, specifically, the E\textsubscript{2} peak shift is proportional to the biaxial stress change

\[ \Delta \omega = 6.2 \Delta \sigma, \quad (4) \]

where \( \Delta \omega \) is the change of Raman shift (cm\textsuperscript{-1}) and \( \Delta \sigma \) is the biaxial stress change (GPa).\textsuperscript{25} As illustrated in Fig. 5.8, the wave number of the HEMT sample before and after the LLO processing is 569.01 cm\textsuperscript{-1} and 567.31 cm\textsuperscript{-1}, respectively. Thus, \( \Delta \omega = 1.697 \text{ cm}^{-1} \), and the corresponding relaxed stress, \( \Delta \sigma = 0.2737 \text{ GPa} \). The relaxed strain resulting from this stress relaxation is obtained from\textsuperscript{26}

\[ \Delta \sigma = \left[ E_{\text{GaN}}/(1 - \nu) \right] \Delta \varepsilon', \quad (5) \]

where \( E_{\text{GaN}} \) is the Young’s modulus of GaN (286 GPa) and \( \nu \) is the Poisson’s ratio (0.183).\textsuperscript{27,28} The partially relaxed strain estimated from the Raman spectrum E\textsubscript{2} peak shift method is \( 7.87 \times 10^{-4} \). This value is on the same order as the value

<table>
<thead>
<tr>
<th>Index of Newton ring, k</th>
<th>Radius of Newton ring, ( r_k ) (( \mu \text{m} ))</th>
<th>Radius of sample curvature, ( R ) (( \mu \text{m} ))</th>
<th>Sample warp, ( d ) (( \mu \text{m} ))</th>
<th>Strain</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>48.5</td>
<td>4163</td>
<td>1.2</td>
<td>2.4 \times 10^{-4}</td>
</tr>
<tr>
<td>2</td>
<td>68.5</td>
<td>4152</td>
<td>1.2</td>
<td>2.4 \times 10^{-4}</td>
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$\Delta \varepsilon$ of $2.4 \times 10^{-4}$ estimated by the Newton’s ring method. For the Al$_{0.25}$Ga$_{0.75}$N/GaN HEMT structures, the theoretical strain due to lattice mismatch is derived from a linear interpolation between the lattice constants of GaN and AlN$^{11}$

$$a(x) = (-0.077x + 3.189) \times 10^{-10} \text{ m},$$

where $a$ is the lattice constant of Al$_x$Ga$_{1-x}$N and $x$ is the atomic fraction of the Al in AlGaN. Thus, the partial relaxed strain obtained by both Newton’s rings and the HEMT sample before and after LLO processing.$^1$
Raman spectroscopy methods only accounted for 5–10% of the original strain.²⁹ As shown in Fig. 5.7(a), the interference patterns were observed in the middle of the sample, but not in the device active area. Hence, the bending of the sample around the device active area was too large to create interference patterns due to additional strain relaxation for the built-in strain caused by the SiNx and metal contact film layers. Multiple probes were also used to flatten the HEMT sample while measuring the drain current, and higher drain current was obtained. Use of three probes for the measurement resulted in reduction of the drain current to the original level. Thus, the drain current reduction of the LLO HEMT was mainly due to strain relaxation and no apparent damage was created during the LLO processing.

To obtain conclusive evidence that LLO processing did not adversely affect the epitaxial layers, TEM analysis was performed. Three sets of samples were analyzed: (1) a set which was not subjected to the LLO process and which served as a reference, (2) AlGaN/GaN LLO samples which were processed in a matrix of different laser fluences, and (3) InAlN/GaN LLO samples which were processed in a matrix of laser fluences in the range 700-1100 mJ·cm⁻². TEM imaging was used to confirm the quality of the constituent epilayers of the HEMTs before and after LLO processing, specifically concentrating on the region of the GaN/sapphire interfaces.

Of primary concern here is whether the lower GaN surface (LLO GaN surface), which is intentionally delaminated from the sapphire substrate during the
LLO processing, maintains structural integrity. If defects develop at this surface as a result of the LLO processing they may then propagate upwards into the channel and buffer layers and significantly degrade HEMT performance.

Figures 5.9 and 5.11 show bright-field (BF) TEM images of one of the AlGaN/GaN HEMT samples and one of the InAlN HEMT samples, respectively, before LLO processing. Threading dislocation density prior to LLO processing was on the order of $10^8 \text{ cm}^{-2}$ for all samples examined.

Fig. 5.9. BF TEM micrographs of an AlGaN/GaN HEMT prior to LLO processing. The sapphire substrate appears at the bottom in all images. (a) Entire epilayer stack comprised predominantly of 2 $\mu$m GaN with overlying 21 nm AlGaN buffer layer and 2.5 nm GaN cap. (b,c) Higher magnification images focusing on the region of the GaN/sapphire interface.
The micrographs for the AlGaN/GaN sample that was subjected to LLO processing with laser fluence of 800 mJ·cm$^{-2}$ appear in Fig. 5.10. Figure 5.10 (a) shows a wax layer (bright intensity due to its low average atomic mass) at the top of the image. This wax was used to adhere the sample to the Si submount. The active area of the HEMT is on this side. Opposite the side on which the wax appears can be seen the Pt used to protect the surface of the lifted-off GaN surface during FIB processing for TEM analysis. To prevent damage to this GaN surface, electron-beam-induced deposition was first used to deposit 200 nm of Pt. This was followed by 2 μm of Ga-ion-beam-induced Pt deposition. The dislocation density in the lower GaN layer estimated from these micrographs was also $\sim 10^8$ cm$^{-2}$ providing the first evidence that LLO processing had not damaged the GaN LLO surface. Closer examination of the lower GaN surface, as depicted in Fig. 5.10 (b), reveals the polycrystalline Pt layer in the bottom of the image but there appears to be no damage attributable to the LLO processing. Figs. 5.10 (c,d) are two HREM micrographs showing different areas of the same GaN surface. Again, the Pt layer is represented by the polycrystalline region at the bottom of the micrographs. It is now apparent that, although the GaN still exhibits good overall crystalline quality, with no substantial damage to the as-grown material, the LLO GaN lower surface now deviates slightly from the relative flatness it exhibited before LLO processing. Figure 5.12 shows micrographs for the InAlN/GaN sample that was subjected to LLO processing with laser fluence of 800 mJ·cm$^{-2}$. The results for this sample show no evidence of damage to the
epilayers which could be attributed to the LLO processing. While differences in electrical performance were more conceivable due to the different heterostructures, from the standpoint of the structural integrity of the LLO GaN

Fig. 5.10. BF TEM micrographs of the AlGaN/GaN HEMT shown in Fig. 5.9 following LLO processing with laser fluence of 800 mJ·cm⁻². (a) Entire epilayer stack, comparable to Fig. 5.9 (a); wax layer visible at top, Pt layer visible at the bottom. (b) Higher magnification image of the LLO GaN surface. (c,d) HREM images of the LLO GaN surface. Polycrystalline Pt layer appears at bottom edge of image.
surface, no significant difference would be expected, their both having the same GaN growth conditions on equivalent sapphire substrates.

Fig. 5.11. BF TEM images of an AlGaN/GaN HEMT prior to LLO processing. The sapphire substrate appears at the bottom in all images. (a) Entire epilayer stack comprised predominately of 1.9 µm GaN with overlying 10.2 nm InAlN buffer layer and 2.2 nm GaN cap. (b,c) Higher magnification images focusing on the GaN/sapphire interface.
5.1.3 Summary

AlGaN/GaN HEMT devices were successfully lifted-off using a 193-nm ArF excimer laser. Laser-drilled grooves on the front-side of the sample were employed to prevent the formation of micro-cracks during the LLO processing.
Other than a 25–43% reduction of the saturation drain current, no degradation of other dc characteristics was observed. The LLO HEMT was warped due to partial relaxation of the as-grown strain as well as strain arising from dielectric and metal depositions. Newton’s rings and Raman spectroscopy methods were used to estimate the partial relaxation of the strain due to the lattice mismatch between $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$ and GaN. The extent of partial relaxation for lattice mismatch accounted for only 5–10% of the drain current reduction. The majority of the drain current reduction was attributed to the relaxation of the strain caused by dielectric and metal deposition. In conjunction with establishing that the electrical performance was not adversely impacted by the LLO processing, the TEM evidence demonstrated that the LLO processing caused no detrimental effects on the quality of the epitaxial layers. Comparison of micrographs taken pre- and post-LLO processing showed no evidence of damage to the bulk of the epilayer. Specifically, no additional threading defects were identified to have been generated during LLO processing.
REFERENCES


6.1 Summary

Group-III nitride HEMTs have demonstrated several performance advantages over conventional semiconductors, especially for high power/high frequency applications. However, many device reliability questions still remain unclear or unanswered. The research presented in this dissertation addressed several critical issues associated with GaN-based HEMT reliability.

Gate-edge defects are conventionally identified as a leading cause of elevated gate leakage current in GaN-based devices. This research demonstrated that the correlation between the presence of such defects and elevated leakage current was only intermittently consistent within the AlGaN/GaN HEMT samples analyzed. Furthermore, interdiffusion at the gate metal/AlGaN buffer was identified and proposed as another possibly significant factor in device degradation.

AlN/GaN HEMTs grown on sapphire were demonstrated to have extrinsic transconductance, \( g_m \), and current gain cutoff frequency—gate length product, \( f_t \cdot L_G \), values that were higher than those reported to date for any other devices. The high performance was partially attributed to the high-quality, ultrathin AlN barrier layer, and robust ohmic and gate contact processes, but TEM analysis also identified the presence of oxidation at the gate metal/AlN buffer layer interface.
This thin $a$-oxide gate insulator was further characterized by energy-dispersive x-ray spectroscopy and energy-filtered TEM. Attributed to this previously unidentified layer, high reverse gate bias up to $-30\,\text{V}$ was demonstrated and drain-induced gate leakage was suppressed to values of less than $10^{-6}\,\text{A/mm}$.

A laser-liftoff (LLO) process was used to separate the active layers (epitaxially-grown, metal contact and interconnect, and passivation layers) from the sapphire substrate for several GaN-based HEMT devices, including each of AlGaN/GaN and InAlN/GaN heterostructure HEMTs. Warpage of the LLO samples resulted from relaxation of the as-grown strain as well as strain arising from dielectric and metal depositions, and this strain was quantified by both Newton’s rings and Raman spectroscopy methods. The quantity of partial relaxation for lattice mismatch only accounted for 5–10% of the drain current reduction. TEM analysis demonstrated that the LLO processing had produced no detrimental effects on the quality of the epitaxial layers. Comparison of electron FImicrographs taken pre- and post-LLO processing showed no evidence of damage to the $\sim2\,\mu\text{m}$ GaN epilayer although the lower GaN surface was partially modified. Moreover, no additional threading defects were identified to have been generated during LLO processing.
6.2 Future Work

6.2.1 Gate Metal/Buffer Layer Interdiffusion

Electron micrographs presented in Chapter 3 showed evidence for interdiffusion occurring at the gate contact/buffer layer interface. The presence of interdiffusion showed correlation to device degradation as manifested by increased gate leakage current. This result is a new finding which has not yet been methodically investigated. Limited work has been done assessing new metal layer systems for the gate Schottky contact so that further research in this area may yield useful results for mitigating interdiffusion. A better long-term approach would be to incorporate a diffusion barrier layer such as an aluminum or silicon oxide. The oxide layer examined in Chapter 4 may be serving this role of preventing interdiffusion. TEM microstructural and chemical analysis would be invaluable for characterizing the gate metal//buffer layer interdiffusion for these approaches and for assessing their relative success in its mitigation.

6.2.2 Device Performance Scalability between TEM Sample and Full-Scale Functional Devices

An assumption that is implicitly made when performing in situ biasing of active devices during TEM observation is that the device sample, after being thinned to electron transparency, presents the same device physics as the full-scale device. One possible source of divergence between the two is the possibility for strain relaxation as the sample is thinned. Of particular interest for GaN-based
HEMTs would be whether this strain relaxation affects the two-dimensional electron gas. Electron holography could be used to monitor HEMT potential profiles as a function of sample thickness.

6.2.3 FIB Liftout Grid for 3-Terminal Biasing Capability

Another problem with *in situ* biasing experiments is the restricted capabilities of commercially available biasing holders. Most biasing holders only allow two-terminal biasing: contact to one terminal is established when the TEM sample is mounted in the holder, a second contact is made with a translatable probe, and a third may be held at ground potential. This configuration enables a limited set of test conditions as well as limited facility for translating and tilting the sample. Companies such as NanoFactory™ now offer commercial solutions for biasing TEM samples but they are cost-prohibitive. An Omniprobe®-type FIB liftout grid could be designed and fabricated to incorporate electrical traces that could be connected to the device via beam-induced deposition in the FIB. A compatible biasing holder, designed to contact the other end of the grid traces would be required.
COMPREHENSIVE LIST OF REFERENCES


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